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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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# H8/38076R

## Transition to the Active (Medium-Speed) Mode

### Introduction

In this example a transition is made from the active (high-speed) mode to the active (medium-speed) mode, one of the power-down modes of the H8/38076R.

### Target Device

H8/38076R

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## 1. Specifications

After a reset is cleared the H8/38076R can transition to any of seven power-down modes, in which power consumption is reduced substantially, in addition to the normal active (high-speed) mode. In this sample task a transition is made from the active (high-speed) mode to the sleep (medium-speed) mode, one of the power-down modes.

## 2. Description of Functions

### 2.1 Functions Used

In this sample task a transition is made from the active (high-speed) mode to the active (medium-speed) mode, one of the power-down modes.

The state of the H8/38076R in the active (medium-speed) mode is shown in table 1, and the functions used as described below.

#### 1. System Clock ( $\phi$ )

This 10-MHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

#### 2. Subclock ( $\phi_w$ )

This 32.768-kHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

#### 3. Power-Down Mode (Active (Medium-Speed) Mode) Function

In the active (medium-speed) mode the system clock oscillator, subclock oscillator, CPU, and internal peripheral modules function.

The active (medium-speed) mode is cleared by the SLEEP instruction. When the active (medium-speed) mode is cleared, a transition is made to the standby mode according to the combination of bits SSBY, TMA3, and LSON in SYSCR1, to the watch mode according to the combination of bits SSBY and TMA3 in SYSCR1, or to the sleep mode according to the combination of bits SSBY and TMA3 in SYSCR1. Moreover, a transition to the active (high-speed) mode or the subactive mode can be made by a direct transition. The active (medium-speed) mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled in an interrupt enable register. When the  $\overline{\text{RES}}$  signal goes low in the active (medium-speed) mode, the active (medium-speed) mode is cleared and the H8/38076R enters the reset state.

The H8/38076R sometimes operates with half state early timing at the time of transition to the active (medium-speed) mode. In the active (medium-speed) mode the internal peripheral modules operate at the clock frequency set by the MA1 and MA0 bits in SYSCR1.

- System control register 1 (SYSCR1)

Together with SYSCR2, SYSCR1 controls the power-down modes.

- System control register 2 (SYSCR2)

Together with SYSCR1, SYSCR2 controls the power-down modes.

**Table 1 State of the H8/38076R in the Active (Medium-Speed) Mode**

<b>Function</b>		<b>Active (Medium-Speed) Mode</b>
System clock oscillator		Functioning
Subclock oscillator		Functioning
CPU	Instructions	Functioning
	RAM	Functioning
	Registers	Functioning
	I/O	Functioning
External interrupts	IRQ0	Functioning
	IRQ1	Functioning
	IRQ3	Functioning
	IRQ4	Functioning
	IRQAEC	Functioning
	WKP0 to WKP7	Functioning
Peripheral modules	Timer F	Functioning
	AEC (Asynchronous event counter)	Functioning
	RTC (realtime clock)	Functioning
	TPU (timer pulse unit)	Functioning
	WDT (watchdog timer)	Functioning
	SCI3/IrDA module	Functioning
	I <sup>2</sup> C2 module	Functioning
	PWM module	Functioning
	A/D converter	Functioning
	LCD controller/driver	Functioning

## 2.2 Assignment of Functions

Table 2 shows the assignment of functions in this sample task. A transition is made from the active (high-speed) mode to the active (medium-speed) mode, one of the power-down modes, using functions assigned as shown in table 2.

**Table 2 Assignment of Functions**

<b>Elements</b>	<b>Description</b>
SYSCR1	Together with SYSCR2, controls transition to the active (medium-speed) mode
SYSCR2	Together with SYSCR1, controls transition to the active (medium-speed) mode

## 3. Principles of Operation

The principles of operation of this sample task are described below. Using the procedure shown, a transition is made from the active (high-speed) mode to the active (medium-speed) mode, one of the power-down modes. The mode transitions in this sample task are illustrated in figure 1.

1. Transition to the active (medium-speed) mode
  - a. Clear the SSBY and LSON bits in SYSCR1 to 0.
  - b. Set the DTON and MSON bits in SYSCR2 to 1.
  - c. Execute the SLEEP instruction.
2. Clearing the active (medium-speed) mode (transition to the active (high-speed) mode)
  - a. Clear the SSBY and LSON bits in SYSCR1 to 0.
  - b. Set the DTON bit to 1 and clear the MSON bit to 0 in SYSCR2.
  - c. Execute the SLEEP instruction.

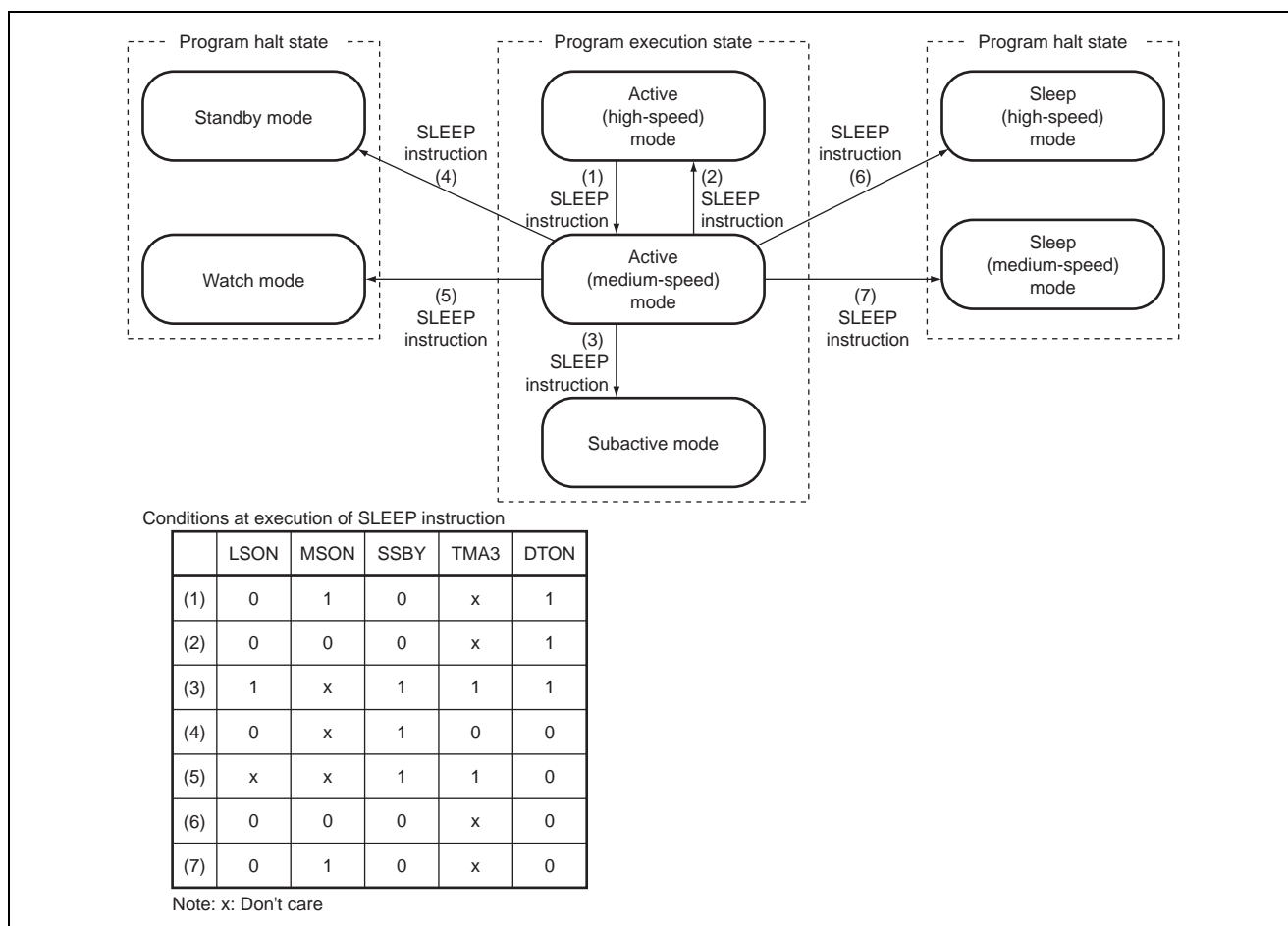


Figure 1 Mode Transition Diagram

#### 4. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SYSCR1                      System control register 1                      Address: H'FFF0

Bit	Bit Name	Set Value	R/W	Description
7	SSBY	0	R/W	Software standby Selects the mode to transition to after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode. 1: A transition is made to the standby mode or the watch mode.
3	LSON	0	R/W	Selects the system clock ( $\phi$ ) or subclock ( $\phi_{SUB}$ ) as the CPU operating clock when the watch mode is cleared. 0: The CPU operates on the system clock ( $\phi$ ) 1: The CPU operates on the subclock ( $\phi_{SUB}$ )
2	TMA3	User defined	R/W	In combination with SSBY and LSON in SYSCR1 and DTON and MSON in SYSCR2, selects the mode to which transition is made after the SLEEP instruction is executed.
1	MA1	User defined	R/W	Active mode clock selection 1 and 0
0	MA0	User defined	R/W	Selects the operating clock frequency in the active (medium-speed) sleep (medium-speed) modes. The MA1 and MA0 bits should be written to in the active (high-speed) mode or the subactive mode. 00: $\phi_{OSC}/8$ 01: $\phi_{OSC}/16$ 10: $\phi_{OSC}/32$ 11: $\phi_{OSC}/64$

- SYSCR2                      System control register 2                      Address: H'FFF1

Bit	Bit Name	Set Value	R/W	Description
3	DTON	1	R/W	Direct transfer on flag Selects the mode to transition to after the SLEEP instruction is executed with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
2	MSON	1	R/W	Medium speed on flag Selects whether operation continues in the active (high-speed) or the active (medium-speed) mode after the standby mode, the watch mode, or the sleep mode is cleared. 0: Active (high-speed) mode 1: Active (medium-speed) mode

## Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued



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