RAA604S00

Design data of two-layer Evaluation board with RF Switch

R01AN4567EJ0200
Rev.2.00
Dec 16, 2022

Introduction

This document describes the design data of the RAA604S00 Evaluation board. The design data includes schematics, BOM list, Gerber data and board layout diagram.

Target Device

RAA604S00

Contents

1. Overview 2
2. Configuration of Application Note 3
3. Substrate layer configuration of RAA604S00 Evaluation board 4

1. Overview

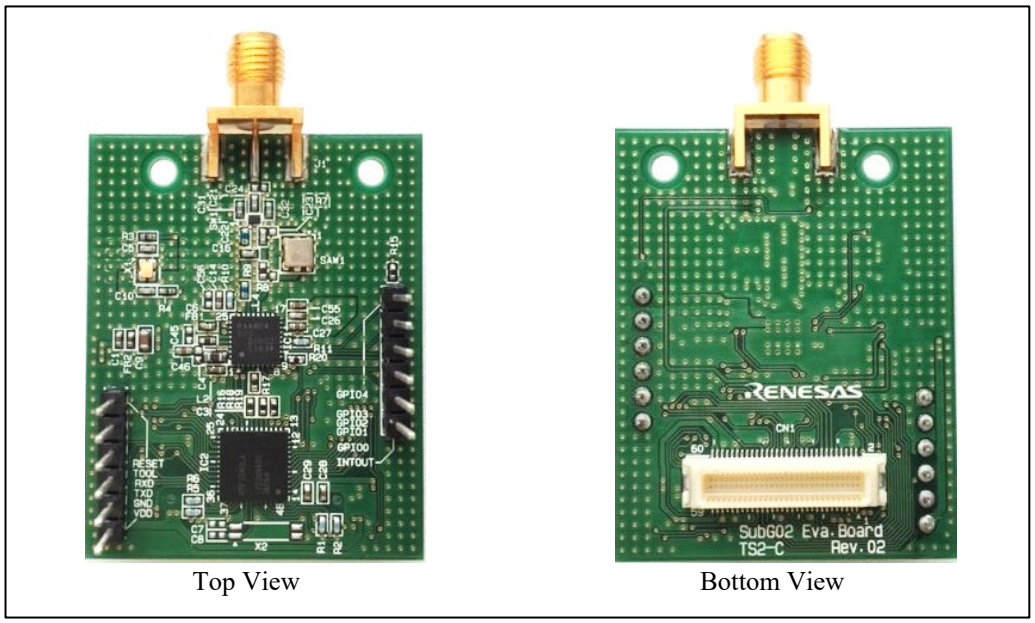
This document aim to deliver the design data of the RAA604S00 Evaluation board. The design data includes schematics, BOM list, Gerber data and board layout diagram.

1.1 Related documents

The following document is related to the application note. Also refer to this document when using this application note.

- Guidelines for the design of two-layer board in RF part (R01AN4426)

1.2 Appearance of Evaluation Board



Top View Bottom View

Figure 1 Appearance of Evaluation Board

2. Configuration of Application Note

This Application Note contains the following contents listed in table 1.

Table 1 Configuration of Application Note

File organization			Description
r01an4567ej0100-raa604s00.pdf			This application note
RAA604S00_Reference_Design_Data			
	01_Circuit_Diagram		
		RAA604S00_TS2-C_Circuit_Diagram.pdf	Circuit of RAA604S00 Evaluation board
	02_Parts_List		
		RAA604S00_TS2-C_Parts_List.pdf	BOM list of RAA604S00 Evaluation board
	03_Gerber_Data		
		SubG02_EVB_TS2-C_Rev2_GA.gbr	Dimensions
		SubG02_EVB_TS2-C_Rev2_LA.gbr	L1: Analog signal, Parts layer
		SubG02_EVB_TS2-C_Rev2_LB.gbr	L2: Digital signal, GND layer
		SubG02_EVB_TS2-C_Rev2_RA.gbr	L1: Resist
		SubG02_EVB_TS2-C_Rev2_RB.gbr	L2: Resist
		SubG02_EVB_TS2-C_Rev2_SA.gbr	L1: Silk
		SubG02_EVB_TS2-C_Rev2_SB.gbr	L2: Silk
		SubG02_EVB_TS2-C_Rev2_MA.gbr	L1: Solder Mask
		SubG02_EVB_TS2-C_Rev2_MB.gbr	L2: Solder Mask
		SubG02_EVB_TS2-C_Rev2_HO.gbr	Via hole
	04_Pattern Figure		
		RAA604S00_TS2-C_Pattern_Layout.pdf	Layout

3. Substrate layer configuration of RAA604S00 Evaluation board

The substrate layer configuration is shown in Figure 2 and Figure 3. This Evaluation board is composed by two substrate layers. Because the change of substrate layer configuration is an effect on RF characteristics, the substrate layer structure should be the same one if you want to get the same characteristics described in RAA604S00 data sheet.

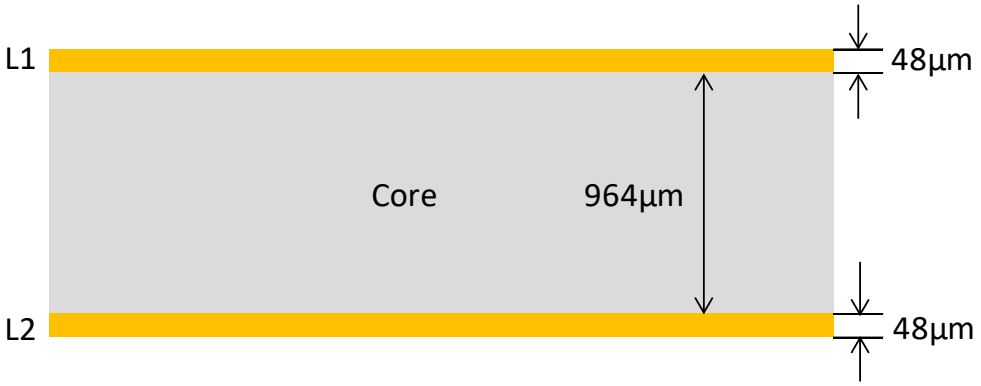


Figure 2 substrate layer configuration

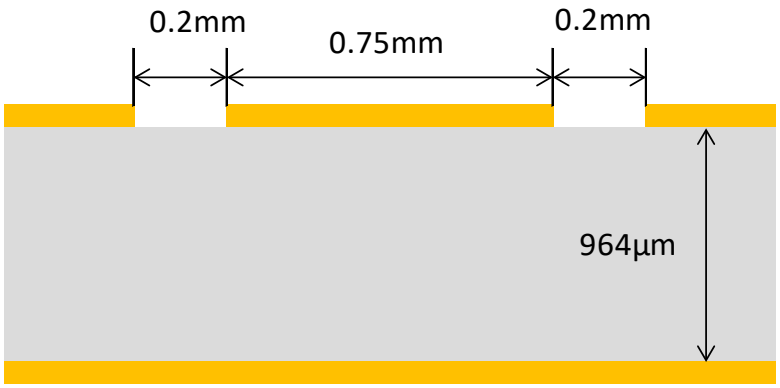


Figure 3 RF unit 50 Ohm impedance line

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Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Dec 12, 2018		First edition issued
2.00	Dec 16, 2022		Updated Circuit_Diagram and Parts_List

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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