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SH7000 Series

Multi-Bit Shift of 32-Bit Data (Arithmetic Right Shift)

| Label: | SHARN |
|-----------------|--|
| Functions Used: | SHLR2 Instruction SHLR8 Instruction SHLR16 Instruction |

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1. Function

Performs a multi-bit (0–31) arithmetic right shift of 32-bit data.

2. Arguments

| Description | | Storage Location | Data Length (Bytes) |
|-------------|-----------------------------|------------------|---------------------|
| Input | Number of shift bits (0–31) | R0 | 4 |
| | 32-bit data before shift | R1 | 4 |
| Output | 32-bit data after shift | R1 | 4 |

3. Internal Register Changes and Flag Changes

| | (Before Execution) \rightarrow (After Execution) |
|-------|--|
| R0 | Number of shift bits \rightarrow Change |
| R1 | 32-bit data before shift \rightarrow 32-bit data after shift |
| R2 | Work |
| R3 | Work |
| R4 | |
| R5 | |
| R6 | |
| R7 | |
| R8 | |
| R9 | |
| R10 | |
| R11 | |
| R12 | |
| R13 | |
| R14 | |
| R15 | (SP) |
| T bit | |
| | * : Change |
| | 0 : Fixed 0 |

1 : Fixed 1



4. Programming Specifications

| Program memory (bytes) |
|------------------------|
| 74 |
| Data memory (bytes) |
| 0 |
| Stack (bytes) |
| 8 |
| Number of states |
| 38 |
| Reentrant |
| Yes |
| Relocation |
| Yes |
| Intermediate interrupt |
| Yes |

5. Notes

The number of states indicated in the programming specifications is the value when a 31-bit shift is performed.



6. Description

(1) Function

Details of the arguments are as follows.

- R0: As the input argument, set the number of shift bits (0-31).
- R1: Set the 32-bit data before the shift as the input argument.

Holds the 32-bit data after the shift as the output argument.

Figure 1 shows a software SHARN execution example.

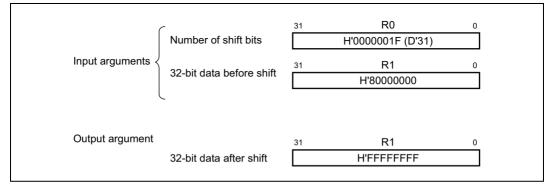


Figure 1 Software SHARN Execution Example

(2) Usage Notes

The contents of R1, which holds the 32-bit data before the shift, are destroyed after the shift when the 32-bit data after the shift is stored there. In addition, execution of the software SHARN instruction changes the setting of R0, which specified the number of shift bits.

If the values for the 32-bit data before the shift and the number of shift bits will be needed after the software SHARN instruction is executed, they should be saved beforehand.

(3) RAM Used

No RAM is used by the software SHARN instruction.

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(4) Usage Example

After the number of shift bits and the 32-bit data before the shift have been set in the input arguments, the software SHARN instruction is executed by a subroutine call.

```
MOV #H'05,R0 .... Sets number of shift bits in input argument (R0)
BSR SHARN .... Subroutine call to software SHARN
MOV.L DATA,R1 .... Sets 32-bit data before shift in input argument (R1)
....
.align 4
DATA .data.l H'80000000
```

(5) Operating Principle

(a) Bits 4 to 0 in R0, which is set to the number of shift bits, are tested. If any of them have a value of 1, a shift corresponding to the weighting of the bits in question is performed using the 16-bit logical right shift command (SHLR16), the 8-bit logical right shift command (SHLR8), the 2-bit logical right shift command (SHLR2), and the 1-bit logical right shift command (SHLR).

| Bit Number | Weighting | Instruction | |
|------------|---------------------|---------------|--|
| Bit 4 | 2 ⁴ = 16 | SHLR16 | |
| Bit 3 | $2^3 = 8$ | SHLR8 | |
| Bit 2 | $2^2 = 4$ | SHLR2 (twice) | |
| Bit 1 | $2^1 = 2$ | SHLR2 | |
| Bit 0 | $2^0 = 1$ | SHLR | |

Table 1 Number of Shift Bits and Instructions Used for Each Bit



(b) Since the 32-bit data before the shift is shifted 16 bits, 8 bits, 2 bits, and 1 bit by the logical right shift instructions, when the MSB of 32-bit data before shift is 1, the empty MSB following the shift becomes not 1 but 0.

Therefore, if R2 contains H'FFFFFFF, as shown in figure 2, and this data is shifted logically right by the same number of bits as the 32-bit data before the shift, and if the MSB before the shift is 1, after the shift the top bits of the shifted portion are set to 1 by a logical OR with the inverted R2 value.

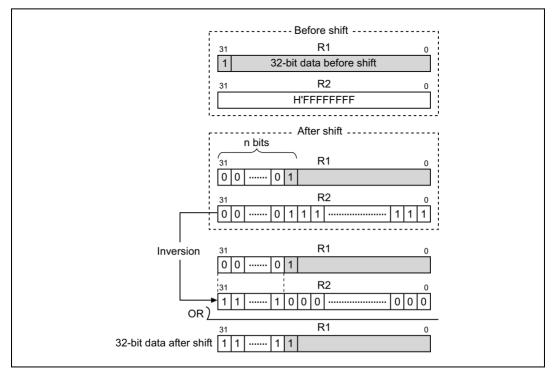
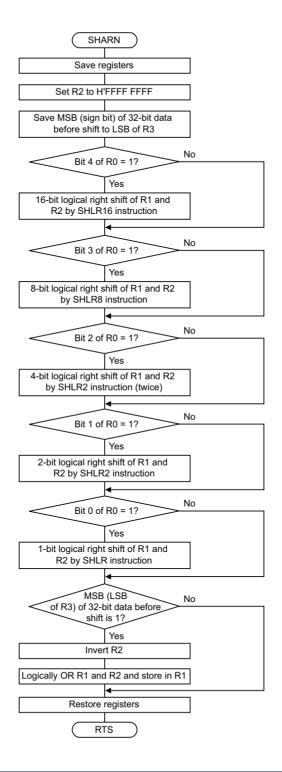


Figure 2 Multiple Bit Shift



7. Flowchart





8. Program Listing

| ENTRY: R0 (NUMER OF BIT SHITED) R1 (32 BIT DATA) RTURNS: R1 (32 BIT DATA) RTURNS: R1 (SHIT RESULT) 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 | NAME: n BITS SHIFT AF | RITHMET | IC RIGH | r (sharn |) | | |
|--|-----------------------------------|---------|---------|----------|----------------|---|--|
| NETURNS: R1 (SHIFT RESULT) 1 ; 1 1 ; 2 3 3 ; 3 3 3 ; 4 4 ; ; 5 . ; ; 6 . ; ; 7 . 7 ; ; 8 . ; ; 9 . . ; ; 10 . 10 ; ; 11 . 10 ; ; 12 0001000 13 SNARN .EQU \$ Recape register 13 0001000 14 MOV.L R2,e=R15 ; recape register 14 0001000 228 MOV.L R2,e2 ; Recape register 14 0001004 3228 17 MOV.L R2,e2 ; Recape register 15 0001004 3228 17 MOV.L R2,e2 ; Recape register 16 0001000 <td< td=""><td colspan="7">ENTRY: R0 (NUMBER OF BIT SHIFTED)</td></td<> | ENTRY: R0 (NUMBER OF BIT SHIFTED) | | | | | | |
| 1 1 , , 2 2 , , 3 3 , , 4 4 , , 5 , , , 6 , , , 7 , , , 8 .8 , , 9 .7 , , 10 .10 , , , 11 .11 , , , 12 00001000 13 SHARN .CODE .LOCATE-H'1000 , 13 00001000 13 SHARN .CODE .LOCATE-H'1000 ; 14 00001000 13 SHARN .CODE .LOCATE-H'1000 ; 15 00001000 14 SHARN .CODE .ROTE .ELOCATE-H'1000 ; 16 00001006 13 SHARN .CODE .ROTE .RI ; ; 16 00001006 140 SHARN .CODE .ROTE .RI ; ; 10 00001000 23 SHARN .CODE .SOTE; ; 2 | R1 (32 BIT DATA) | | | | | | |
| 2 2 ; 3 3 ; 4 3 ; 5 5 ; 5 5 ; 6 ; ; 7 7 ; 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 0001000 13 13 0001000 13 14 0001000 14 15 0001002 2P36 16 0001004 15 17 00001004 16 18 00001006 17 19 00001006 18 10 00001006 19 11 , R3C 12 0000100 103 10 00001006 19 11 , R3C 12 0000100 19 12 0000100 10 20 0000100 10 | | LT) | | | | | |
| 3 3 , ; 4 4 ; 5 5 ; 6 6 ; 7 7 ; 8 8 ; 9 9 ; 10 ; ; 11 10 ; 12 00001000 13 SHARN .EQU \$; 13 00001000 13 SHARN .EQU \$; Eacape register 14 00001002 2P26 14 MOV.L R3. e -R15 ; Eacape register 15 00001002 2P26 14 MOV.L R3. e -R15 ; 16 00001004 128 SHARN1 ; Eacape register 17 00001006 6227 18 NOT R2.R2 ; 10 00001006 228 ROT R1 ; 20 00001000 105 23 SHARN3 ; 22 0000100 201 ROT R1 ; No | | | | | | | |
| 4 4 ; 5 5 ; 6 ; ; 7 7 ; 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 00001000 13 SHARN JEQU \$ Retry point 14 00001002 2F26 14 MOV.L R3,e=R15 ; 15 00001004 16 SHARN JEQU \$ \$ Retry point 15 00001004 16 SHARN JEQU \$ \$ Retry point 16 00001004 16 SHARN JEQU \$ \$ Retry point 17 00001004 128 SHARN JEQU \$ \$ Retry point 18 00001006 6227 18 NOT R2,R2 ; R2 \leftarrow MSB of 32 bit data 21 00001005 19 SHARN3 ; S S 22 00001005 21 MOT R3 Bit 4 = 17 | 2 | 2 | | | | ; | |
| 5 5 ; 6 6 ; 7 7 ; 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 0001000 12 .SECTION A, CODE, LOCATE=H'1000 13 0001000 22 .SECTION A, CODE, LOCATE=H'1000 14 00001000 2726 14 MOV.L R2,e-R15 ; 16 0001002 2736 15 MOV.L R3,e-R15 ; 16 0000106 6227 18 NOT R2,R2 ; R3 ← MSB of 32 bit data 17 0001006 6227 18 NOT R2,R2 ; ; 18 00001006 4044 20 ROTL R1 ; ; 20 0000108 103 SHARN3 ; ; ; 21 00001006 123 SHARN4 ; N0 ; 22 00001010 132 SHARN5 ; N | 3 | 3 | | | | ; | |
| 6 6 ; 7 7 ; 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 00001000 12 .SECTION A, CODE, LOCATE=H'1000 13 00001000 13 SHARN .EQU \$: Entry point 14 00001002 2F26 14 MOV.L R2,e-R15 ; Eacape register 15 00001004 16 SHARN ; : : 17 00001004 16 SHARN ; : : 17 00001004 3228 17 SUB R2,R2 ; : 19 00001006 6227 18 NOT R3 ; : 20 00001008 19 SHARN3 ; : : : 21 00001008 329 21 MOVT R3 ; : 22 00001010 6901 25 SHARN3 ; : : | | | | | | ; | |
| 7 7 ; ; 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 00001000 13 SHARN .CQU \$? Entry point 14 0000100 13 SHARN .CQU \$? Excape register 15 0000102 2726 14 MOV.L R3.eR15 ? 16 0000104 3228 17 SUB R2.R2 ? R2 16 0000104 3228 17 SUB R2.R2 ? . 18 0000108 109 SHARN R0T R2.R2 ? . 19 0000108 109 SHARN R1 ? . 20 0000108 103 SHARN R0T R3 . 21 0000100 0329 21 MOVT R3 . 22 0000100 C810 24 SHARN3 . . 23 00001010 801 2 | | | | | | ; | |
| 8 8 ; 9 9 ; 10 10 ; 11 11 ; 12 0001000 13 SKARN .FQU \$ fntry point 14 00001002 2P36 14 MOV.L R2, e =R15 ; Excurpediate 15 0001002 2P36 15 MOV.L R3, e -R15 ; Intry point 16 0001004 3228 17 SUB R2,R2 ; R2 ← H'FFFFFFFF 18 0001006 6227 18 NOT R2,R2 ; R2 ← MSB of 32 bit data 20 0001008 109 SHARN2 ; ; SHARN3 ; 21 00001008 104 20 ROTR R1 ; R3 ← MSB of 32 bit data 21 00001002 4104 20 ROTR R1 ; R3 ← MSB of 32 bit data 22 00001002 4104 20 ROTR R1 ; R3 ← MSB of 32 bit data 23 0000102 510 SHARN3 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> | | | | | | | |
| 9 9 ; 10 | | | | | | | |
| 10 10 ; 11 11 ; 12 0000100 12 .SECTION A, CODE LOCATE=H'100 13 00001000 2726 14 MOV.L $R2, e-R15$; Entry point 15 00001002 2726 14 MOV.L $R3, e-R15$; 16 00001004 16 SHARN ; SUB $R2, R2$; $R2 \leftarrow H'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF$ | | | | | | | |
| 11 11 ; 12 00001000 13 SHARN .EQU \$; Entry point 14 00001000 2F36 14 MOV.L R2,0=R15 ; Escape register 15 0001004 3228 17 SUB R2,R2 ; R 16 0001006 6227 18 NOT R2,R2 ; R 19 0001008 104 20 ROTL R1 ; R3 ← MSB of 32 bit data 21 0001008 4104 20 ROTL R1 ; R3 ← MSB of 32 bit data 22 00001008 4104 20 ROTL R1 ; R3 ← MSB of 32 bit data 21 00001002 6329 21 MOVT R3 ; ; 23 00001002 6810 24 TST #B'0001000,R0 ; Bit 4 = 1? 25 0001010 8901 25 BT SHARN4 ; No 26 00001012 8101 15 SHARN5 ; Bit 4 = 1?< | | | | | | | |
| 12 0.0001000 12 SECTION A, CODE.JCCATE=H'1000 13 0.0001000 13 SHARN .EQU \$ Fectoperigiter 14 0.0001001 2P26 14 MOV.L R2.eR15 ; Escaperegister 15 0.0001002 2P26 15 MOV.L R2.eR15 ; Escaperegister 15 0.0001004 1228 15 MOV.L R2.eR2 ; R2 + H'FFFFFFF 18 0.001006 6227 18 NOT R2.R2 ; R3 + MSB of 32 bit data 19 0.001008 103 SHARN1 r ; R3 + MSB of 32 bit data 21 0.001008 103 Q2 ROTL R1 ; R3 + MSB of 32 bit data 21 0.001000 4105 22 ROTL R1 ; R3 + MSB of 32 bit data 22 0.001000 4105 23 SHARN3 ; No ; 23 0.001000 5 BT SHARN4 ; No 24 0.0001010 810 25 BT SHARN4 ; No 25 0.0001010 810 < | | | | | | | |
| 13 00001000 13 SHARN .EQU \$ Furty point 14 00001000 2F26 14 MOV.L R2.0=R15 ; Escape register 15 00001002 2F36 15 MOV.L R3.0=R15 ; 16 00001004 3228 17 SUB R2.R2 ; R2 \leftarrow H'FFFFFFFF 18 00001006 6227 18 NOT R2.R2 ; 19 0001008 4104 20 ROTL R1 ; 2 20 0001000 3228 22 ROTR R1 ; 2 20 0001000 4104 20 ROTL R1 ; 2 20 0001000 105 22 ROTR R1 ; 2 20 0001000 22 ROTR R1 ; 16 16 21 0001000 22 ROTR R1 ; 16 16 17 22 00001010 8001 25 SHARN3 ; N0 16 16 | | | | | | ; | |
| 14 0001000 2F26 14 MOV.L $R2, =R15$; Escape register 15 0001002 2F36 15 MOV.L $R3, =R15$; 16 0001004 3228 17 SUB $R2, R22$; $R2 \leftarrow$ H'FFFFFFFF 18 0001006 6227 18 NOT $R2, R22$; 19 0001008 19 SHARN2 ; ; $R3 \leftarrow$ MSB of 32 bit data 21 0001008 104 20 ROTL R1 ; R3 \leftarrow MSB of 32 bit data 21 0001006 0329 21 MOVT R3 ; 22 0001006 105 22 ROTR R1 ; 23 0001002 C810 24 TST #B'0001000,R0 ; Bit 4 = 1? 25 0001010 8901 25 BT SHARN4 ; No 26 00001012 4129 27 SHLR16 R1 ; Ib is is if 1 egical right 27 00001016 288 SHARN4 ; No ; ; | | | | | | | |
| 15 0001002 2F36 15 MOV.L $R3, \theta-R15$; 16 0001004 16 SHARN1 ; 17 0001006 6227 18 NOT R2, R2 ; $R2 \leftarrow H'FFFFFFFF$ 18 0001006 6227 18 NOT R2, R2 ; $R2 \leftarrow H'FFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFFF$ | | | | | | | |
| 16 0001004 328 17 SUB R2, R2 ; R2 \leftarrow H'FFFFFFF 18 0001006 5228 17 NOT R2, R2 ; R2 \leftarrow H'FFFFFFF 18 00001008 19 SHARN1 ; ; R3 ; 19 00001008 100 SHARN1 R1 ; R3 ; 20 00001008 0329 21 MOVT R3 ; 23 00001002 21 MOVT R3 ; 24 00001002 23 SHARN3 ; ; 25 00001002 SH0 24 TST #B'0001000,R0 ; Bit 4 = 1? 25 00001012 4129 27 SHLR16 R1 ; 16 bit shift logical right 27 00001014 4229 27 SHLR16 R1 ; 8 bit shift logical right 30 00001016 8901 30 SHLR16 R1 ; 8 bit shift logical right 31 00001016 8901 30 <t< td=""><td></td><td></td><td></td><td></td><td></td><td></td></t<> | | | | | | | |
| 1700001004 322817SUBR2,R2; R2 ← H'FFFFFFF18NOTR2,R2;19000100819SHARN2;2000001008 410420ROTLR1;21000100A 032921MOVTR3;220000100C 410522ROTR1;230000100E23SHARN3;240000100E C81024TST#B'0001000,R0;2500001012 412926SHLR16R1;2600001012 412926SHLR16R1;2700001014 422927SHLR16R1;280000101628SHARN4;NO290000101628SHARN4;NO3000001014411931SHLR8R1;3000001014411931SHLR8R1;310000101263SHARN5;NO3100001014411931SHLR8R1;320000101263SHLR1;Bit 2 = 1?33000010127SHLR2R1;Hit shift logical right34000010280335ST#B'0000100,R0;350001028410937SHLR2R1;36000102410936SHLR2R1;370001024410937SHLR2 | | | | | | | |
| 18 0001006 6227 18 NOT R2,R2 ; 19 0001008 104 20 ROTL R1 ; R3 \leftarrow MSB of 32 bit data 21 0001000 0329 21 MOV R3 ; 22 0001002 105 22 ROT R3 ; 23 0001002 210 ROT R3 ; 24 0001002 210 ROT R3 ; 24 0001002 210 24 TST #B'0001000,00 ; Bit 4 = 1? 25 0001010 8901 25 BT SHARN4 ; NO 26 0001014 4229 27 SHL16 R1 ; 16 bit shift logical right 27 00001016 28 SHARN5 ; Si j 30 00001016 8901 30 SHARN5 ; No 31 00001014 4119 31 SHARN5 ; No 31 00001012 8003 S | | | SHARN1 | | | | |
| 19000100819SHARN2;200001008410420ROTLR1;R3 \leftarrow MSB of 32 bit data21000100032921ROTRR1;22000100C410522ROTRR1;23000100E23SHARN3;;24000100EC81024TST $\#$ B'0001000,R0;bit 4 = 1?250001012412926SHARN4;No260001014422927SHL16R1;16 bit shift logical right2700001014422927SHL16R2;;2800001016C80829TST $\#$ B'0001000,R0;Bit 3 = 1?3000001018890130BTSHARN5; No3100001014411931SHARN5; No3300001012410932SHARN5;3400001012890335BT;SHARN6350000102890335SHARN2R1;3600001024410937SHAR2R1;370001024410937SHARN5;i38000102A420938SHARN2;;39000102A420936SHAR2R2;39000102A420936SHARN5;40000102A4209S | | | | | | | |
| 200001008410420ROTLR1; R3 \leftarrow MSB of 32 bit data21000100A032921MOVTR3;22000100C410522ROTRR1;23000100E23SHARN3;;24000100C 681024TST $\#$ 0001000,R0;Bit 4 = 1?2500001010890125BTSHARN4;No2600001012412926SHAR16R1;16 bit shift logical right2700001014422927SHLR16R2;;2800001016C80829TST $\#$ 00001000,R0;Bit 3 = 1?3000001018890130BTSHARN5; No3100001014411931SHARN5; 8 bit shift logical right3200001016C80829TST $\#$ 00000100,R0;3100001014411931SHARN5;330000101633SHARN5;;3400001012890335BTSHARN6; No350000102890335BTSHARN6; No3600001024410937SHLR2R1; 4 bit shift logical right370001024410937SHLR2R1;380001024410939SHLR2R2;39000102A40SHRR6 <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td></td<> | | | | | | | |
| 21000100A032921MOVTR3;22000100C410522ROTRR1;23000100EC81023SHARN3;;240000100EC81024TST#B'0001000,R0;Bit 4 = 1?250000101890125BTSHARN4;No2600001012412926SHR16R1;16 bit shift logical right270000101628SHARN4;SHARN5;280000101628SHARN5;Bit 3 = 1?3000001016890130STB'10001000,R0;3000001016890130SHARN5;No3100001014411931SHARN5;No3300001012421932SHARN5;SHARN53400001012680335BTSHARN6;350000102890335BTSHARN6;360000102410937SHAR2R1;4 bit shift logical right370000102420938SHARN6;No380000102420939SHARN6;No390000102A420SHARN6;SHAR1;410000102A40SHARN6;SHAR1;420000102A40SHARN6;SHAR1; <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> | | | | | | | |
| 22000100C 410522ROTRR1;23000100E23SHARN3;;24000100EC81024TST $\#$ B'0001000,R0;Bit 4 = 1?250000101890125BTSHARN4;No2600001012412926SHLR16R1;16 bit shift logical right2700001014422927SHLR16R2;2800001016C80829TST $\#$ B'0000100,R0;Bit 3 = 1?3000001018890130BTSHARN5;No3100001014411931SHLR8R1;8 bit shift logical right320000101628SHARN5;No3100001016411931SHLR8R1;8 bit shift logical right3200001016411931SHLR8R1;bit 2 = 1?3300001016890335BTSHARN6;3400001024410937SHLR2R1;4 bit shift logical right3700001024410937SHLR2R1;4 bit shift logical right3800001024420938SHLR2R2;;40000102A40SHAR06;Bit 1 = 1?410000102A40SHAR06;No430000102A41TST $\#$ 10000010,R0 <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> | | | | | | | |
| 23000100E23SHARN3;24000100E C81024TST#B'0001000,R0; Bit 4 = 1?250001010890125BTSHARN4; No260001012412926SHLR16R1; 16 bit shift logical right2700001014422927SHLR16R2;2800001016C80829TST#B'0000100,R0; Bit 3 = 1?3000001018890130ETSHARN5; No3100001014411931SHLR8R1; 8 bit shift logical right320000101C421932SHARN5;330000101E68034TST#B'0000100,R0; Bit 2 = 1?340000101E C80434TST#B'0000100,R0; bit 2 = 1?350000102410936SHLR2R1; A bit shift logical right360000102410936SHLR2R1; A bit shift logical right370001024410937SHLR2R1; A bit shift logical right3800001024420939SHLR2R2;41000102A40SHARN6; Bit 1 = 1?42000102A41TST#B'0000010,R0; Bit 1 = 1?43000102A41TST#B'0000010,R0; Dit 1 = 1?44000102A42FTSHARN7; No44000102A44SHLR2 | | | | | | | |
| 24 0000100E C810 24 TST #B'0001000,R0 ; Bit 4 = 1? 25 00001012 4129 25 BT SHARN4 ; No 26 00001012 4129 26 SHLR16 R1 ; 16 bit shift logical right 27 00001014 4229 27 SHLR16 R2 ; 28 00001016 28 SHARN4 ; Bit 3 = 1? 29 00001018 8901 30 BT SHARN5 ; No 31 00001012 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 00001012 4219 32 SHLR8 R2 ; 33 00001012 C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 0000102 8903 35 BT SHARN6 ; No 36 0000102 4109 36 SHLR2 R1 ; 4 bit shift logical right 38 0000102 4109 37 SHLR2 R1 ; 4 bit shift logical right 39 000102A 4209 38 SHLR2 R2 ; 40 00 | | | | | RI | | |
| 25 0001010 8901 25 BT SHARN4 ; No 26 0001012 4129 26 SHLR16 R1 ; 16 bit shift logical right 27 0001014 4229 27 SHLR16 R2 ; 28 0001016 C808 29 TST #B'0001000,R0 ; Bit 3 = 1? 30 0001018 8901 30 BT ; No 31 0001012 4119 31 SHLR8 R1 ; Bit 3 = 1? 32 0001012 4219 32 SHLR8 R1 ; Bit 3 = 1? 33 0001012 4219 32 SHLR8 R1 ; Bit 3 = 1? 34 0001012 8903 35 SHLR8 R1 ; No 35 000102 8903 35 SHLR2 R1 ; No 36 0001024 4109 37 SHLR2 R1 ; Abit shift logical right 38 0001024 109 38 SHLR2 R1 ; No 40 000102A 40 SHARN6 </td <td></td> <td></td> <td></td> <td></td> <td>#D100010000 D0</td> <td></td> | | | | | #D100010000 D0 | | |
| 26 0001012 4129 26 SHLR16 R1 ; 16 bit shift logical right 27 0001014 4229 27 SHLR16 R2 ; 28 0001016 C808 29 TST #B'0001000,R0 ; Bit 3 = 1? 30 0001018 8901 30 BT SHARN5 ; No 31 0001014 4119 31 SHARN5 ; Bit 3 = 1? 32 0001012 4219 32 SHAR R1 ; 8 bit shift logical right 32 0001012 4219 32 SHAR R1 ; 8 bit shift logical right 33 0001012 6209 33 SHAR R1 ; 8 bit shift logical right 34 0001012 6804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 0001020 8903 35 BT SHAR ; A bit shift logical right 36 0001024 4109 37 SHLR2 R1 ; A bit shift logical right 37 0001024 4109 38 SHLR2 R2 ; | | | | | | | |
| 27 00010114 4229 27 SHLR16 R2 ; 28 0001016 28 SHARN4 ; 29 00001016 C808 29 TST #B'00001000,R0 ; Bit 3 = 1? 30 00001018 8901 30 BT SHARN5 ; No 31 00001014 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 00001012 219 32 SHARN5 ; ; 33 00001012 33 SHARN5 ; ; Bit 2 = 1? 34 00001012 8903 35 BT SHARN6 ; No 34 0000102 8903 35 BT SHARN6 ; No 35 00001024 4109 37 SHLR2 R1 ; 4 bit shift logical right 37 00001024 4209 38 SHLR2 R2 ; ; 38 0000102A 420 SHARN6 ; Bit 1 = 1? 41 0000102A 420 | | | | | | | |
| 28 00001016 28 SHARN4 ; 29 00001016 C808 29 TST #B'000100,R0 ; Bit 3 = 1? 30 00001018 8901 30 BT SHARN5 ; No 31 00001014 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 00001012 4219 32 SHLR8 R1 ; 8 bit shift logical right 33 00001012 6804 34 SHLR8 R1 ; start 34 00001012 8903 35 BT #B'00000100,R0 ; Bit 2 = 1? 35 0001020 8903 35 BT SHARN6 ; No 36 0001024 4109 37 SHLR2 R1 ; 4 bit shift logical right 38 0001024 4109 37 SHARN6 ; No 40 0000102A 400 SHARN6 ; Bit 1 = 1? 41 0000102A 41 TST #B'00000010,R0 <td< td=""><td></td><td></td><td></td><td></td><td></td><td></td></td<> | | | | | | | |
| 29 00001016 C808 29 TST #B'0000100,R0 ; Bit 3 = 1? 30 00001018 8901 30 BT SHARN5 ; No 31 0000101A 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 0000101C 4219 32 SHLR8 R2 ; 33 0000101E C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 34 0000101E C804 34 TST #B'00000100,R0 ; Bit 2 = 1? 35 00001020 8903 35 BT SHARN6 ; No 36 0001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 38 0001024 4109 37 SHLR2 R1 ; ; 39 000102A 40 SHARN6 ; j ; ; 41 0000102A 40 SHARN6 ; j ; i 42 0000102A (8901 42 BT SHARN7 ; No <t< td=""><td></td><td></td><td></td><td></td><td>KZ</td><td></td></t<> | | | | | KZ | | |
| 30 00001018 8901 30 BT SHARN5 ; No 31 00001014 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 00001012 4219 32 SHLR8 R2 ; 33 0000101E CR04 34 SHARN5 ; Bit 2 = 1? 34 0000102 8903 35 BT #B'0000100,R0 ; Bit 2 = 1? 35 0000102 4109 36 SHLR2 R1 ; No 38 0001024 4109 37 SHLR2 R1 ; 4 bit shift logical right 39 0001024 4109 37 SHLR2 R1 ; 4 bit shift logical right 39 0001024 4109 37 SHLR2 R1 ; - 39 0001024 4209 38 SHLR2 R2 ; - 40 000102A 40 SHARN6 ; Bit 1 = 1? 41 0000102A 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102A 68901 42 BT SH | | | SHARNA | | #B'00001000 P0 | | |
| 31 0000101A 4119 31 SHLR8 R1 ; 8 bit shift logical right 32 0000101C 4219 32 SHLR8 R2 ; 33 0000101E 33 SHARN5 ; ; 34 0000101E C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 00001022 8903 35 BT SHARN6 ; No 36 00001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 00001024 4109 37 SHLR2 R1 ; 4 bit shift logical right 38 00001024 4209 38 SHLR2 R1 ; - 39 0001024 4209 39 SHLR2 R2 ; - 40 0000102A 40 SHARN6 ; - - 41 0000102A 41 TST #B'00000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 | | | | | | | |
| 32 0000101C 4219 32 SHLR8 R2 ; 33 0000101E 33 SHARN5 ; ; 34 0000101E C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 00001020 8903 35 BT SHARN6 ; No 36 00001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 00001024 4109 37 SHLR2 R1 ; . 38 00001024 4209 38 SHLR2 R2 ; . 40 000102A 400 SHARN6 ; . . 41 0000102A 40 SHARN6 ; . 42 0000102A 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102A 8901 42 BT SHARN7 ; No 43 0000102A 410 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4 | | | | | | | |
| 33 000101E 33 SHARN5 ; 34 000101E C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 00001020 8903 35 BT SHARN6 ; No 36 00001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 00001024 4109 37 SHLR2 R1 ; - 38 00001026 4209 38 SHLR2 R2 ; - 39 0000102A 420 39 SHARN6 ; Bit 1 = 1? 41 0000102A 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 0001030 420 SHLR2 R1 ; 2 bit shift logical right | | | | | | | |
| 34 0000101E C804 34 TST #B'0000100,R0 ; Bit 2 = 1? 35 00001020 8903 35 BT SHARN6 ; No 36 00001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 00001024 4109 37 SHLR2 R1 ; 38 00001026 4209 38 SHLR2 R2 ; 39 00001028 4209 39 SHLR2 R2 ; 40 0000102A 400 SHARN6 ; Bit 1 = 1? 41 0000102A C802 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; i stick if i i i i i i i i i i i i i i i i i i | | | SHARN5 | | | | |
| 35 0001020 8903 35 BT SHARN6 ; No 36 0001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 0001024 4109 37 SHLR2 R1 ; | | | | | | | |
| 36 0001022 4109 36 SHLR2 R1 ; 4 bit shift logical right 37 0001024 4109 37 SHLR2 R1 ; 38 0001026 4209 38 SHLR2 R2 ; 39 00001028 4209 39 SHLR2 R2 ; 40 000102A 400 SHARN6 ; ; 41 0000102A 6802 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| 37 00001024 4109 37 SHLR2 R1 ; 38 00001026 4209 38 SHLR2 R2 ; 39 00001028 4209 39 SHLR2 R2 ; 40 0000102A 40 SHARN6 ; ; 41 0000102A 6802 41 TST #B'00000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| 38 0001026 4209 38 SHLR2 R2 ; 39 0001028 4209 39 SHLR2 R2 ; 40 000102A 40 SHARN6 ; ; 41 0000102A C802 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 00001022 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; * | | | | | - 1 | | |
| 39 0001028 4209 39 SHLR2 R2 ; 40 000102A 40 SHARN6 ; ; 41 0000102A C802 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 00001022 410 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| 40 0000102A 40 SHARN6 ; 41 0000102A C802 41 TST #B'0000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| 41 0000102A C802 41 TST #B'00000010,R0 ; Bit 1 = 1? 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | SHARN6 | | | | |
| 42 0000102C 8901 42 BT SHARN7 ; No 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | - | | | | |
| 43 0000102E 4109 43 SHLR2 R1 ; 2 bit shift logical right 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| 44 00001030 4209 44 SHLR2 R2 ; | | | | | | | |
| | | | | | | | |
| | 45 00001032 | 45 | SHARN7 | | | | |



SH7000 Series Multi-Bit Shift of 32-Bit Data (Arithmetic Right Shift)

| 46 | 00001032 | C801 | 46 | | TST | #B'0000001,R0 | ; | Bit 0 = 1? |
|----|----------|------|----|---------|-------|----------------|---|---------------------------|
| 47 | 00001034 | 8901 | 47 | | BT | SHARN8 | ; | No |
| 48 | 00001036 | 4101 | 48 | | SHLR | Rl | ; | 1 bit shift logical right |
| 49 | 00001038 | 4201 | 49 | | SHLR | R2 | ; | |
| 50 | 0000103A | | 50 | SHARN8 | | | ; | |
| 51 | 0000103A | 6033 | 51 | | MOV | R3,R0 | ; | |
| 52 | 0000103C | C801 | 52 | | TST | #B'00000001;R0 | ; | MSB of 32 bit data = 1? |
| 53 | 0000103E | 8901 | 53 | | BT | SHARN_END | ; | No |
| 54 | 00001040 | 6227 | 54 | | NOT | R2,R2 | ; | |
| 55 | 00001042 | 212B | 55 | | OR | R2,R1 | ; | |
| 56 | 00001044 | | 56 | SHARN_E | ND | | ; | |
| 57 | 00001044 | 63F6 | 57 | | MOV.L | @R15+,R3 | ; | Return register |
| 58 | 00001046 | 000B | 58 | | RTS | | ; | |
| 59 | 00001048 | 62F6 | 59 | | MOV.L | @R15+,R2 | ; | |
| 60 | | | 60 | | .END | | | |
| | | | | | | | | |

*****TOTAL ERRORS 0

*****TOTAL WARNINGS 0



SH7000 Series Multi-Bit Shift of 32-Bit Data (Arithmetic Right Shift)

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Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

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