Notes on the Measured S-parameters for the F1240 Dual Intermediate Frequency Digital Variable Gain Amplifier

Introduction

The F1240 Dual Intermediate Frequency Digital Variable Gain Amplifier consists of two separate channels. Each channel has a differential digital step attenuator (DSA) and an differential amplifier. The DSA is a 6-bit device with a 0.5 dB step for a 31.5 dB attenuation range. The amplifier has a maximum differential gain of approximately 20 dB. When discussing the F1240 we talk about the gain state which will vary from 20 to -11.5 dB. The frequency range 10 to 500 MHz.

We have designed our evaluation board for single ended operation for ease of testing. This means we use a 4:1 transformer to transmit a signal into and out of the DVGA. Customers are requesting S-parameters to the individual ports on the package so that simulations can be done at the system level. This note is to explaining the calibration and testing methodology that has been performed to obtain the data.

Evaluation Board

In order to accomplish this, a new evaluation board was designed. Figure 1 shows the original evaluation board, while Figure 2 shows the special evaluation board.

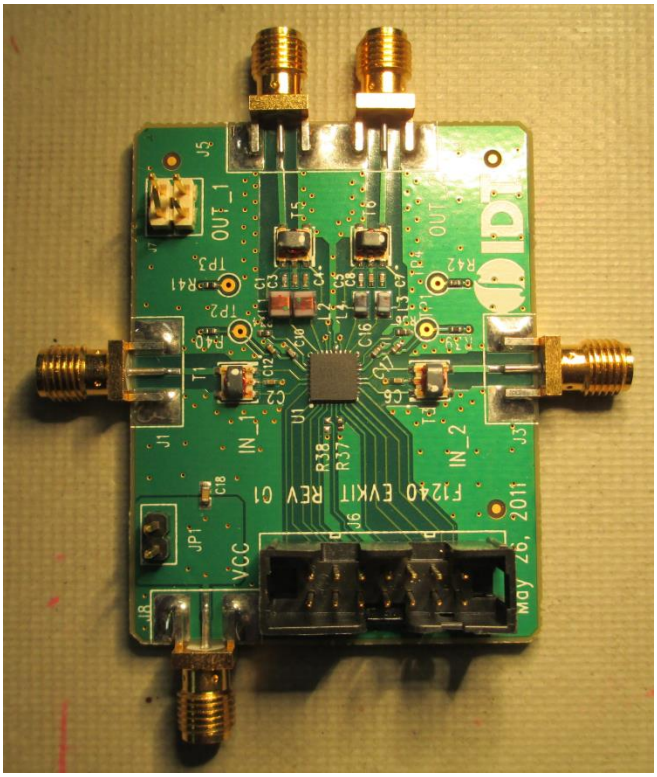

Figure 1 - Standard F1240 Evaluation Board

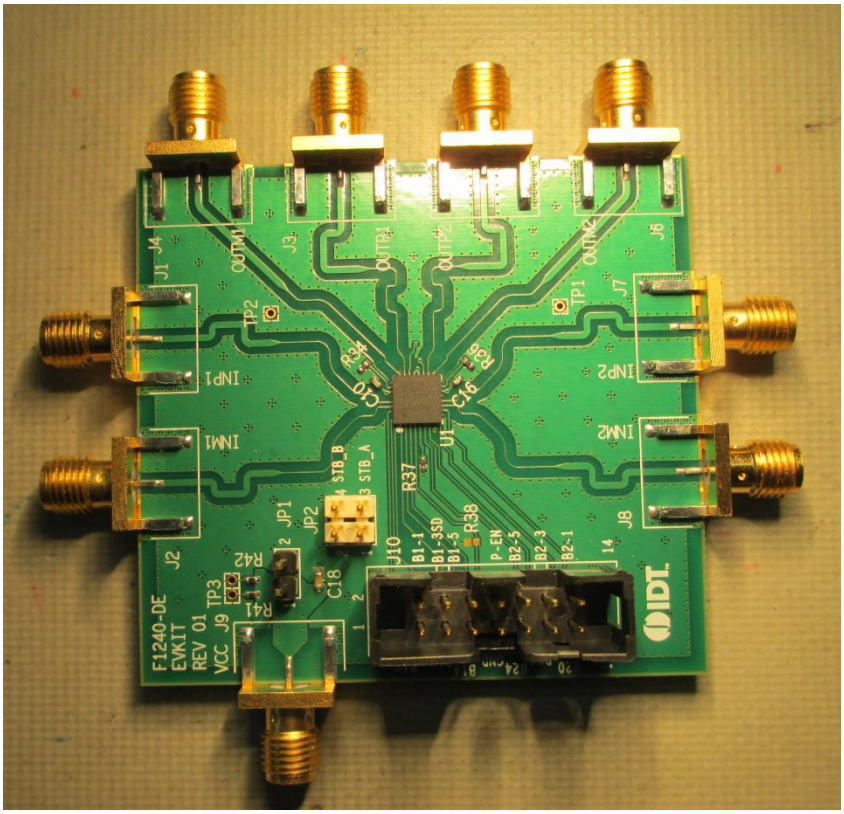

Figure 2 - Modified F1240 Evaluation Board for Individual Port Access

The new evaluation board has equal length lines. The miter bends were needed to create the proper length. The overall length were matched to within 10 mils or 1.3 degrees at 1.0 GHz. This error is attributed to not properly accounting for the miter bend effective length. But does not affect the overall calibration. We only need one board to make a complete measurement. This evaluation board was mislabeled for the input port names. “P” and “N” should be reversed. This has no effect on the measurements.

Calibration

The above board was designed so that a port de-embedding and port impedance can be preformed. Port de-embedding was done using the Automatic Fixture Removal (AFR) technique. Details of this technique can be found at Keysight Technologies (formerly Agilent Technologies) website in their application notes and forums. A simplified description is: a network analyzer is first calibrated to the connectors using standard calibration (mechanical or electronic) techniques to at least twice the frequency range you would like to use. We performed a measurement to 20 GHz. Each port of the evaluation board is connected to network analyzer with no device installed and a 1 port measurement is saved. Each of these files is analyzed using the AFR routine with the assumption there is a open circuit at the end. The AFR routine will then generate a 2 port file for each port so de-embdedding can be done. Each file is the used in the fixture 2-port de-embedding option.

Since the amplifier is a differential amplifier, there are four ports that need be measured., A four port calibration was performed from 0.0005 to 4.000 GHz using a segment sweep. The input power was set for -10 dBm to assure that the small signal operation of the amplifier was being used.

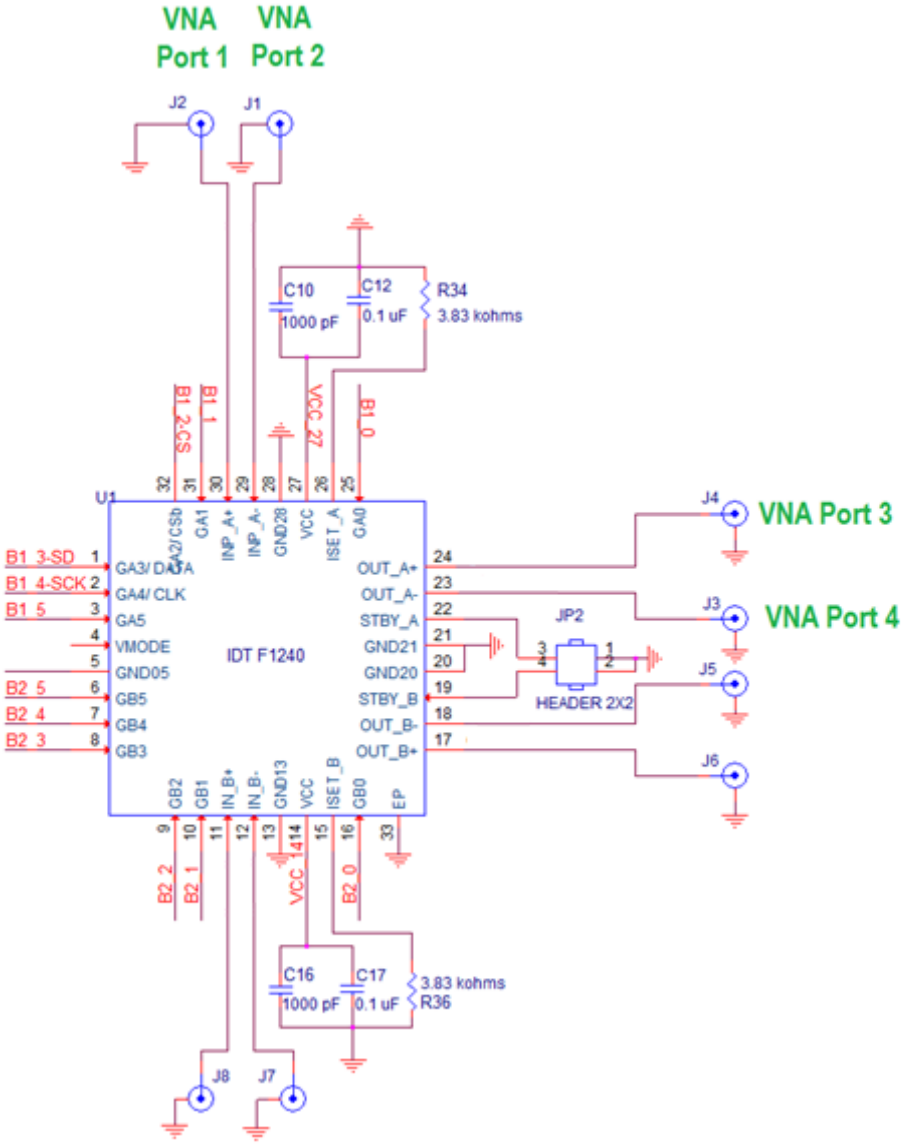

Figure 3 - Network Analyzer Port Connection and S-Parameter file designation

Data Collection

All gain states of the F1240 were measured. Only Channel 1 (or “A”) was measured. Figure 3 shows how the network analyzer was connected to the product. The port designations also represent the ports within the S-parameter files. The states were changed by using the Serial Programming Interface (SPI). Two 8-Bit words are sent to device. The first 8 Bit word tells which channel is being controlled, while the second 8-bit word will enable or disable the channel (D7) and set the gain setting. This second 8-Bit word is shown in Table.

The S-parameter data is single ended data and reference to 50 ohms. To evaluate differential or common mode gain, impedances, and other parameters the S-parameter files may be used in a linear simulator that will apply the correct signals to both ports 1 and 2 and ports 3 and 4.

Table 1 - F1240 States, Filenames, and Serial Data Word

State	Gain State	File Name	D7	D6	D5	D4	D3	D2	D1	D0
0	20.0	F1240_p20p0dB_SE.S4P	E	0	0	0	0	0	0	x
1	19.5	F1240_p19p5dB_SE.S4P	E	0	0	0	0	0	1	x
2	19.0	F1240_p19p0dB_SE.S4P	E	0	0	0	0	1	0	x
3	18.5	F1240_p18p5dB_SE.S4P	E	0	0	0	0	1	1	x
4	18.0	F1240_p18p0dB_SE.S4P	E	0	0	0	1	0	0	x
5	17.5	F1240_p17p5dB_SE.S4P	E	0	0	0	1	0	1	x
6	17.0	F1240_p17p0dB_SE.S4P	E	0	0	0	1	1	0	x
7	16.5	F1240_p16p5dB_SE.S4P	E	0	0	0	1	1	1	x
8	16.0	F1240_p16p0dB_SE.S4P	E	0	0	1	0	0	0	x
9	15.5	F1240_p15p5dB_SE.S4P	E	0	0	1	0	0	1	x
10	15.0	F1240_p15p0dB_SE.S4P	E	0	0	1	0	1	0	x
11	14.5	F1240_p14p5dB_SE.S4P	E	0	0	1	0	1	1	x
12	14.0	F1240_p14p0dB_SE.S4P	E	0	0	1	1	0	0	x
13	13.5	F1240_p13p5dB_SE.S4P	E	0	0	1	1	0	1	x
14	13.0	F1240_p13p0dB_SE.S4P	E	0	0	1	1	1	0	x
15	12.5	F1240_p12p5dB_SE.S4P	E	0	0	1	1	1	1	x
16	12.0	F1240_p12p0dB_SE.S4P	E	0	1	0	0	0	0	x
17	11.5	F1240_p11p5dB_SE.S4P	E	0	1	0	0	0	1	x
18	11.0	F1240_p11p0dB_SE.S4P	E	0	1	0	0	1	0	x
19	10.5	F1240_p10p5dB_SE.S4P	E	0	1	0	0	1	1	x
20	10.0	F1240_p10p0dB_SE.S4P	E	0	1	0	1	0	0	x
21	9.5	F1240_p09p5dB_SE.S4P	E	0	1	0	1	0	1	x
22	9.0	F1240_p09p0dB_SE.S4P	E	0	1	0	1	1	0	x
23	8.5	F1240_p08p5dB_SE.S4P	E	0	1	0	1	1	1	x
24	8.0	F1240_p08p0dB_SE.S4P	E	0	1	1	0	0	0	x
25	7.5	F1240_p07p5dB_SE.S4P	E	0	1	1	0	0	1	x
26	7.0	F1240_p07p0dB_SE.S4P	E	0	1	1	0	1	0	x
27	6.5	F1240_p06p5dB_SE.S4P	E	0	1	1	0	1	1	x
28	6.0	F1240_p06p0dB_SE.S4P	E	0	1	1	1	0	0	x
29	5.5	F1240_p05p5dB_SE.S4P	E	0	1	1	1	0	1	x
30	5.0	F1240_p05p0dB_SE.S4P	E	0	1	1	1	1	0	x
31	4.5	F1240_p04p5dB_SE.S4P	E	0	1	1	1	1	1	x
32	4.0	F1240_p04p0dB_SE.S4P	E	1	0	0	0	0	0	x
33	3.5	F1240_p03p5dB_SE.S4P	E	1	0	0	0	0	1	x
34	3.0	F1240_p03p0dB_SE.S4P	E	1	0	0	0	1	0	x
35	2.5	F1240_p02p5dB_SE.S4P	E	1	0	0	0	1	1	x
36	2.0	F1240_p02p0dB_SE.S4P	E	1	0	0	1	0	0	x
37	1.5	F1240_p01p5dB_SE.S4P	E	1	0	0	1	0	1	x
38	1.0	F1240_p01p0dB_SE.S4P	E	1	0	0	1	1	0	x
39	0.5	F1240_p00p5dB_SE.S4P	E	1	0	0	1	1	1	x
40	0.0	F1240_p00p0dB_SE.S4P	E	1	0	1	0	0	0	x
41	-0.5	F1240_m00p5dB_SE.S4P	E	1	0	1	0	0	1	x
42	-1.0	F1240_m01p0dB_SE.S4P	E	1	0	1	0	1	0	x
43	-1.5	F1240_m01p5dB_SE.S4P	E	1	0	1	0	1	1	x
44	-2.0	F1240_m02p0dB_SE.S4P	E	1	0	1	1	0	0	x
45	-2.5	F1240_m02p5dB_SE.S4P	E	1	0	1	1	0	1	x
46	-3.0	F1240_m03p0dB_SE.S4P	E	1	0	1	1	1	0	x
47	-3.5	F1240_m03p5dB_SE.S4P	E	1	0	1	1	1	1	x
48	-4.0	F1240_m04p0dB_SE.S4P	E	1	1	0	0	0	0	x
49	-4.5	F1240_m04p5dB_SE.S4P	E	1	1	0	0	0	1	x
50	-5.0	F1240_m05p0dB_SE.S4P	E	1	1	0	0	1	0	x
51	-5.5	F1240_m05p5dB_SE.S4P	E	1	1	0	0	1	1	x
52	-6.0	F1240_m06p0dB_SE.S4P	E	1	1	0	1	0	0	x
53	-6.5	F1240_m06p5dB_SE.S4P	E	1	1	0	1	0	1	x
54	-7.0	F1240_m07p0dB_SE.S4P	E	1	1	0	1	1	0	x
55	-7.5	F1240_m07p5dB_SE.S4P	E	1	1	0	1	1	1	x
56	-8.0	F1240_m08p0dB_SE.S4P	E	1	1	1	0	0	0	x
57	-8.5	F1240_m08p5dB_SE.S4P	E	1	1	1	0	0	1	x
58	-9.0	F1240_m09p0dB_SE.S4P	E	1	1	1	0	1	0	x
59	-9.5	F1240_m09p5dB_SE.S4P	E	1	1	1	0	1	1	x
60	-10.0	F1240_m10p0dB_SE.S4P	E	1	1	1	1	0	0	x
61	-10.5	F1240_m10p5dB_SE.S4P	E	1	1	1	1	0	1	x
62	-11.0	F1240_m11p0dB_SE.S4P	E	1	1	1	1	1	0	x
63	-11.5	F1240_m11p5dB_SE.S4P	E	1	1	1	1	1	1	x

Note: Bit D7 will Enable (E=1) or Disable (E=0) the channel selected