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1. Introduction

The P9221-R Wireless Power Receiver (Rx) is an integrated circuit (IC) consisting of multiple high-power blocks and noise-sensitive circuits controlled by a microprocessor. When implementing the application circuit on a printed circuit board (PCB), there are often tradeoffs associated with managing the critical current paths. In order to optimize the design, components should be placed on the circuit board based on circuit function to guarantee best performance. The thermal management of the P9221-R is also important to the product's performance and should be optimized when designing the PCB. The following guidance should be used in order to place the components in order of priority based on operation.

There are three main categories of circuitry:

- Power circuits
- Sensitive circuits
- Non-sensitive circuits

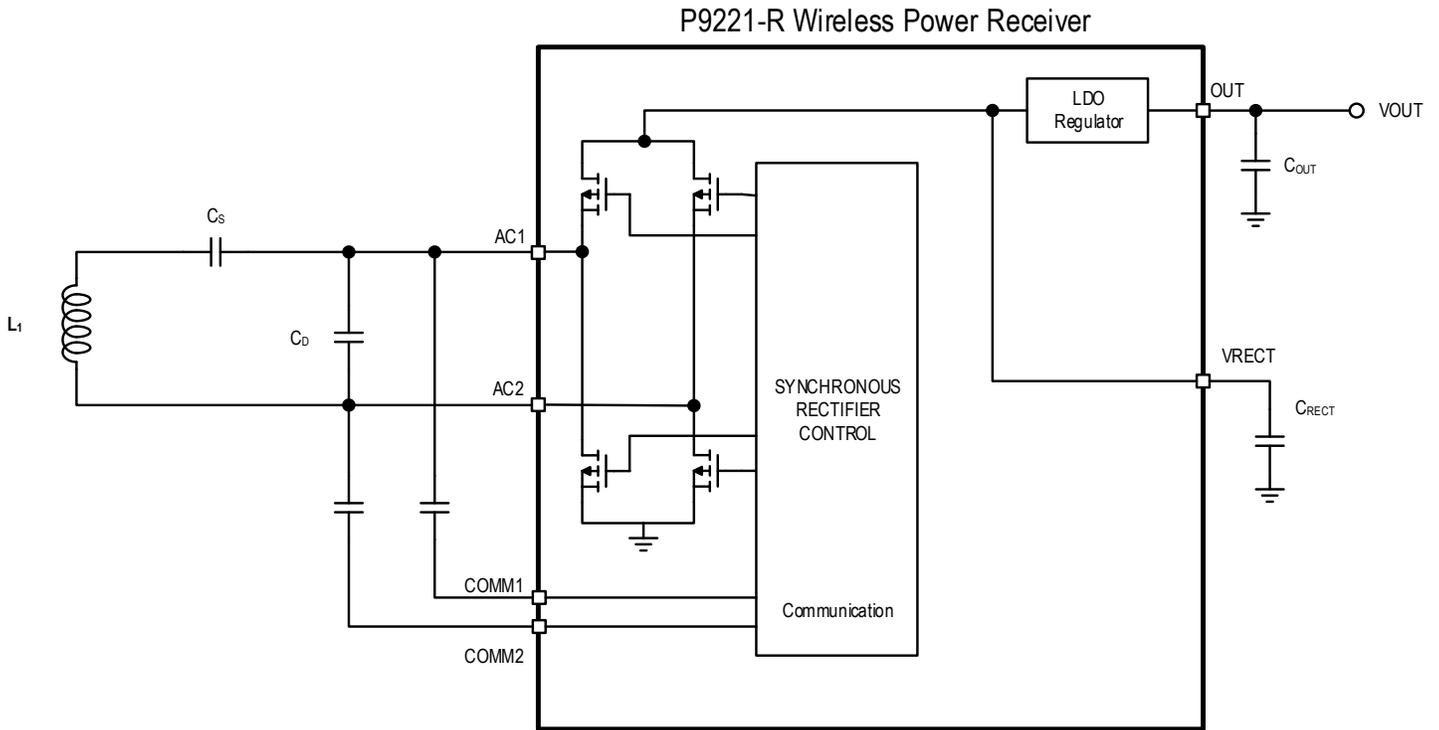
1.1 Key Points for Optimal Layout

- Route the power connections wide (≥ 100 mils) and on the same side of the PCB as the P9221-R.
- Use the layer under the P9221-R side of the board as a solid ground plane.
- Connect all 8 GND pins to the ground plane(s) using via-in-pads. Add a thermal tab for the J-row GND pins (see pin layout in the *P9221-R Datasheet*).
- Avoid unnecessary layer transitions for the AC power connections (LC node and the VRECT, AC1, AC2, and GND pins).
- Place the P9221-R as close as possible to the center of the board. Avoid placing it along the PCB edge.
- Connect as much copper as possible to every pin of the P9221-R, including pins that do not carry high current.
- Place components in the following order: resonance capacitors (C_S and C_D as shown in Figure 1), VRECT pin capacitors, BST pin capacitors, OUT pin capacitors, communication capacitors, VDD18 pin capacitors, and VDD5V pin capacitors.
- Use minimal trace-to-trace separation for all traces and planes connected to and within 10mm of the P9221-R.
- Use low-ESR resonance capacitors (C_S , C_D) to decrease losses in the LC and AC1 current path (C0G preferred).
- Follow the placement and routing suggestions outlined in the remainder of this document for the specific types of circuits. Refer to the schematics in section 5 for the location of components.

2. Rx Power Circuits

The main power circuits of the IDTP9221-R device are the resonance tank, the synchronous bridge rectifier/inverter, and the low drop-out (LDO) linear regulator. Secondary power circuits are the VDD5V and VDD18 regulators.

Figure 1. P9221-R Power Block



Recommendation: Once the final shape of the production or development PCB has been determined and the connection points for the power transfer coil (L_{RX}) have been chosen, place the P9221-R on the board as close to the center of the PCB as possible, taking into consideration the mechanical requirements of the system under design. Its orientation should be determined based on the ability to route connections and place the required components in the order of priority given in section 1.1. The main power current path is considered to be the connection from the L_{RX} coil to the AC2 pin and the resonance capacitors to the AC1, GND, VRECT, and VOUT connections. The trace for the power connections should be wide and on the same side of the PCB as the P9221-R (see section 1.1 for requirements for the power connections). An example of the optimal P9221-R orientation relative to the L_{RX} coil and the optimal output connector physical locations is shown in Figure 3.

2.2 Thermal Management

The heat management of the P9221-R design is critical to performance, and from the thermal perspective, it is recommended that the main power connections be routed as directly as possible to the device. This allows optimal electrical and thermal performance. See the example layouts in Figure 3 through Figure 6 for a demonstration of the following principles of heat management.

The main power connections are VRECT, AC1, AC2, VOUT, the Rx coil node (LC node), and GND. These connections should be routed on the same side of the PCB as the P9221-R for maximum thermal benefit (excluding GND, which should be on the closest internal layer and the outer layer opposite to the P9221-R). These traces should avoid multiple layer changes in order to reduce voltage drops and thermal resistance induced by thin via walls. If these traces need to transfer to other layers, it should be accomplished using multiple vias that have enough spacing such that they do not block the current path leading up to the via.

The thermal tab, which is a copper shape with 22 thermal vias as shown in Figure 3, is an important connection and layout improvement because it assists with current conduction and dramatically improves the P9221-R thermal performance. Vias-in-pad for GND pins and the thermal tab are recommended for all layouts.

The outer layers of the PCB will be the most effective at transferring heat from the board to the ambient air or other objects. Spreading the heat into internal layers is also effective for lowering the operating temperature since the thickness of the PCB allows the thermal resistance of the FR-4 material to have a fairly small resistance to heat flow along the z-axis. Internal layers are able to effectively spread heat horizontally when they are not interrupted by traces and through-holes along their surface. An ideal layout will result in the entire PCB being approximately the same temperature; however, in order to obtain this result, all board layers should have planes that are fairly continuous and in direct contact with the P9221-R via-in-pads. A single internal layer should be selected for routing the majority of the inner row/column pins to the rest of the PCB. The third layer is preferred for this purpose. The required nodes for connecting heat spreading planes are GND, VRECT, AC1, AC2, and OUT. The other connections will spread heat due to natural thermodynamics, but the listed nodes contact the primary heat sources of the P9221-R.

Figure 3. P9221-R-EVK Evaluation Board V2.2 (Top Layer)

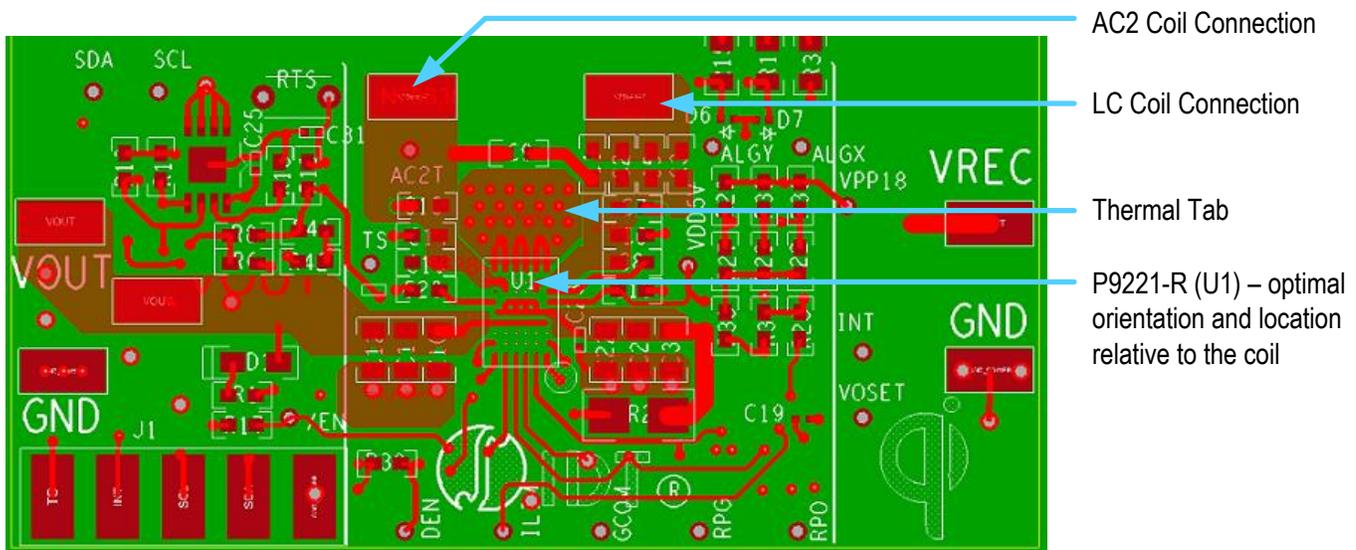


Figure 4. P9221-R-EVK Evaluation Board V2.2 (Second Layer)

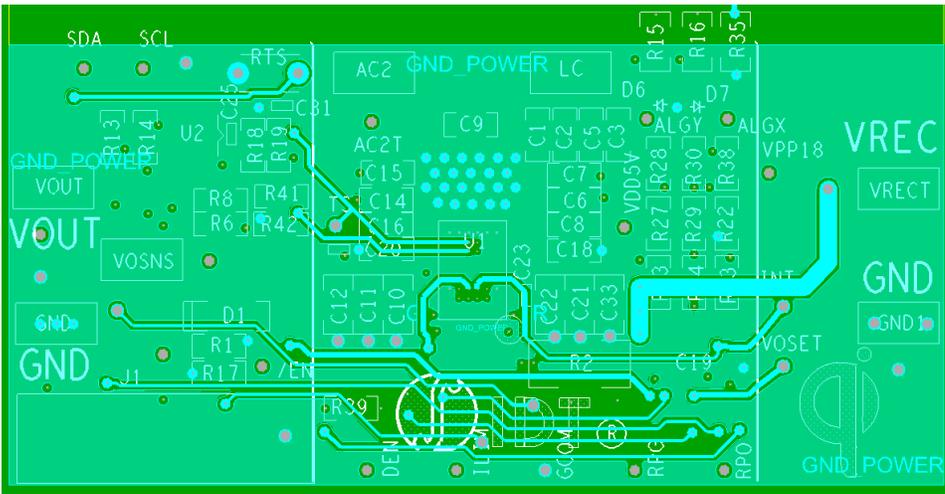


Figure 5. P9221-R-EVK Evaluation Board V2.2 (Third Layer)

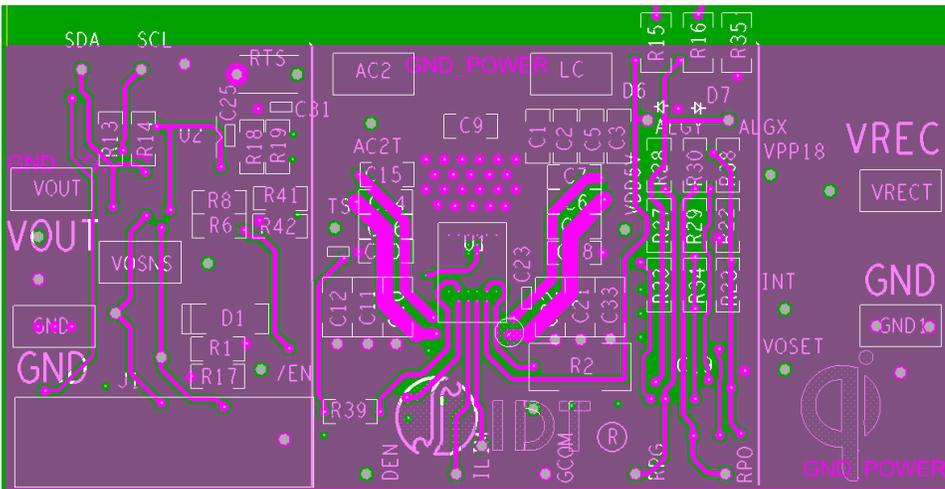
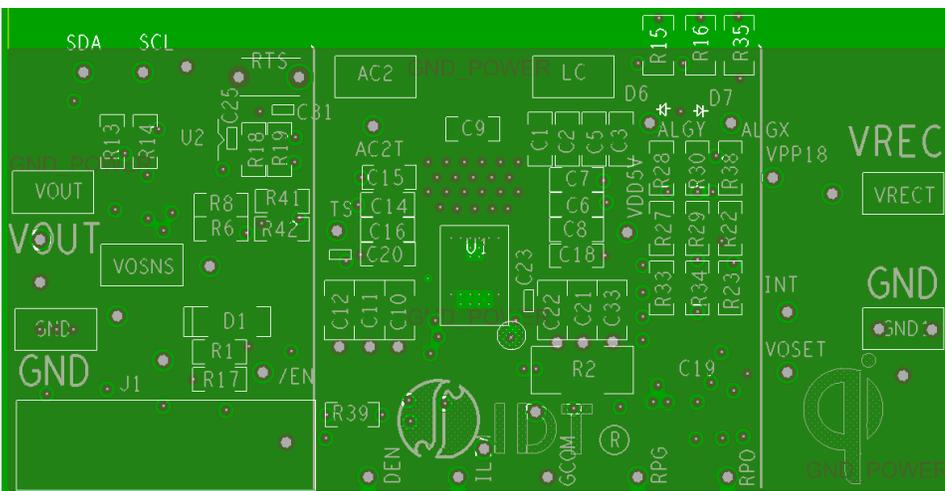


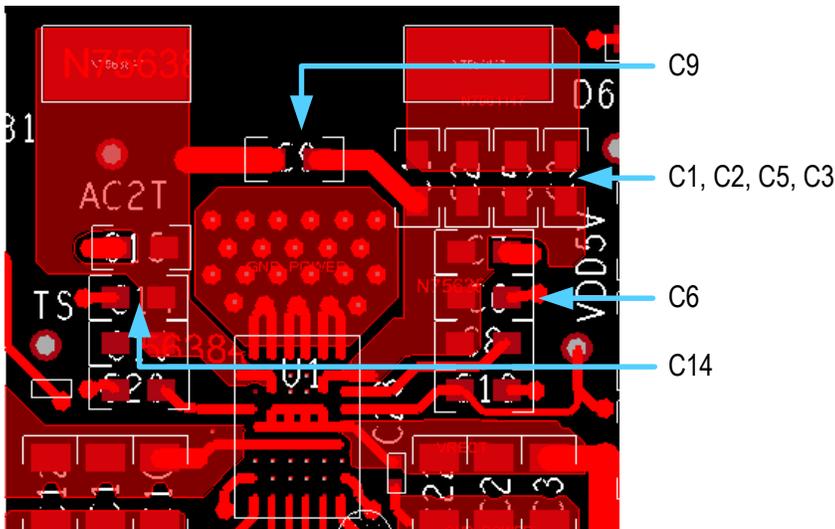
Figure 6. P9221-R-EVK Evaluation Board V2.2 (Bottom Layer)



2.3 Communication and Resonance Capacitors

The communication capacitors (C6 and C14) and resonance capacitors (C1, C2, C3, C5, and C9) should be placed on the same layer as the P9221-R. The resonance capacitors should be close to the P9221-R and have fairly direct connections to the respective pins (route 12 to 20 mils wide). The resonance capacitors should have wide copper planes connected to them (at least 50 mils) and be in-line from the P9221-R to the Rx coil. C0G-type capacitors will offer the highest performance and are highly recommended. The X7R and X5R type capacitors can be substituted. However, low-ESR capacitors should be utilized. Since all the load current and the current required to charge the VRECT/VOUT capacitors flows through the resonance capacitors, the heat developed within the resonance capacitors (Class II only) should be allowed to spread into large copper planes.

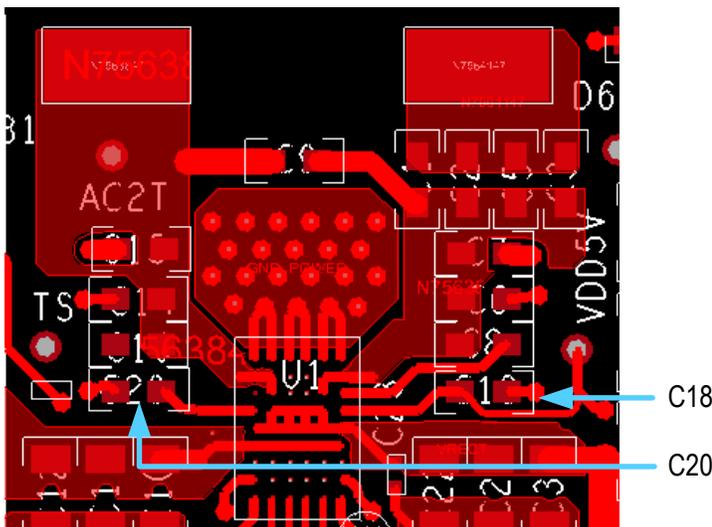
Figure 7. Communication and Resonance Capacitors



2.4 VDD18 and VDD5V Pin Capacitors

The VDD5V and VDD18 pin capacitors (C20 and C18) are used to stabilize the internal linear regulators. These capacitors must be located close to the P9221-R.

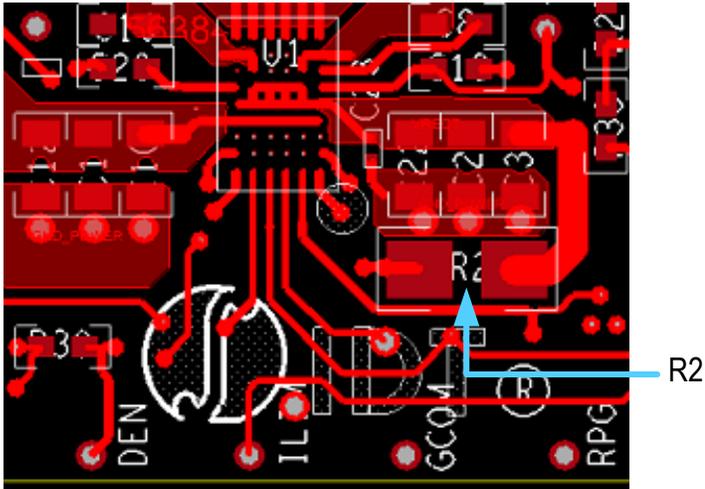
Figure 8. VDD18 and VDD5V Pin Capacitors



2.5 SINK

The SINK connection to the VRECT node is used to provide DC clamping of the rectifier output voltage during transient events. A 1/2W, 36Ω resistor (R2) must be located close to the P9221-R. Optimal placement is directly connected to the VRECT node and routed to the SINK pin using a trace width of at least 12 mils. This is the primary VRECT clamping mechanism and must be connected at all times.

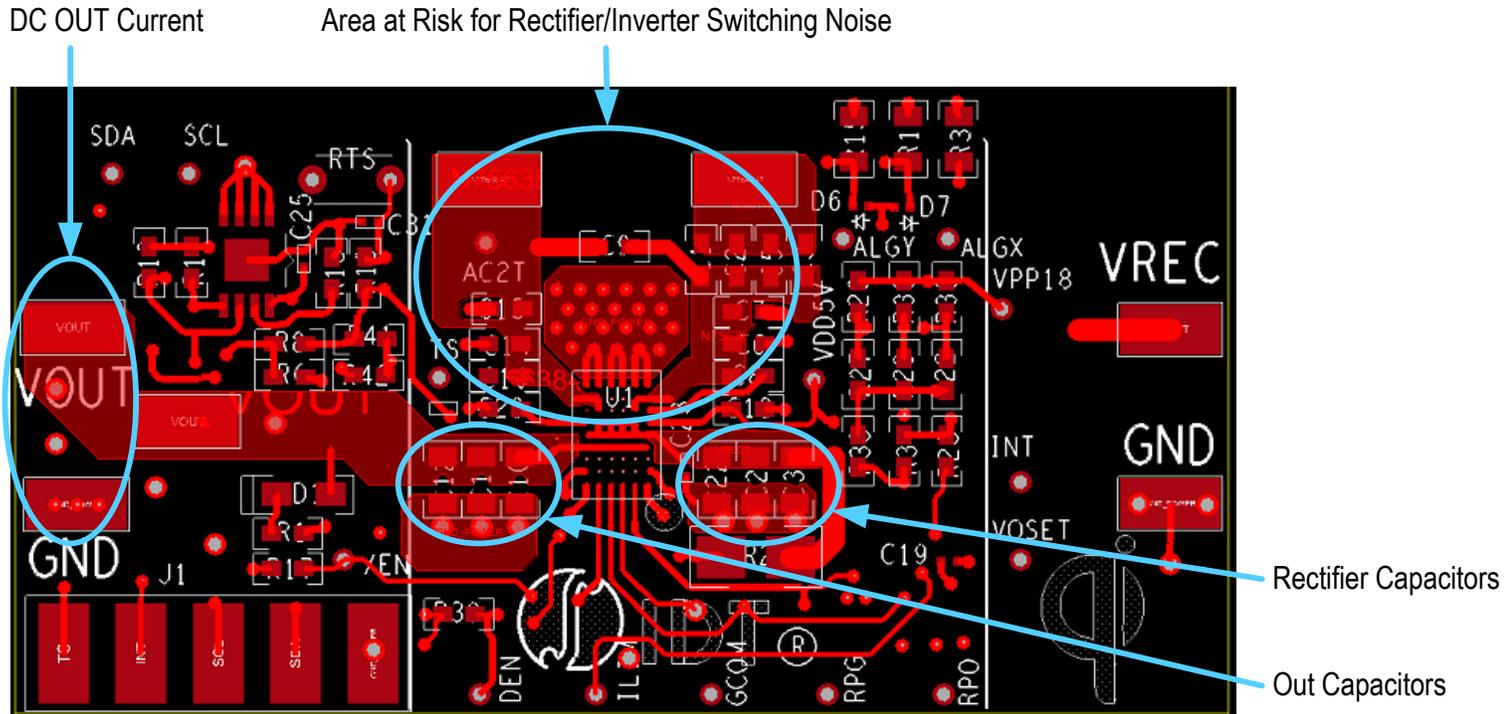
Figure 9. SINK Connection to VRECT



2.6 Sensitive Circuits

The term “sensitive circuits” refers to noise-sensitive circuits that should be referenced to GND in the “quiet” ground area; see Figure 10. AC coupling, the thermistor bypass capacitors, and other capacitors are for decoupling noise. In order to optimize the signal-to-noise performance, it is recommended that the OUT pin capacitors be placed on the side of the P9221-R closest to the OUTPUT/INPUT voltage connector and that the rectifier capacitors be placed on the opposite side of the P9221-R. The rectifier and resonance nodes generate the highest harmonic noise, which must be filtered with a decoupling capacitor.

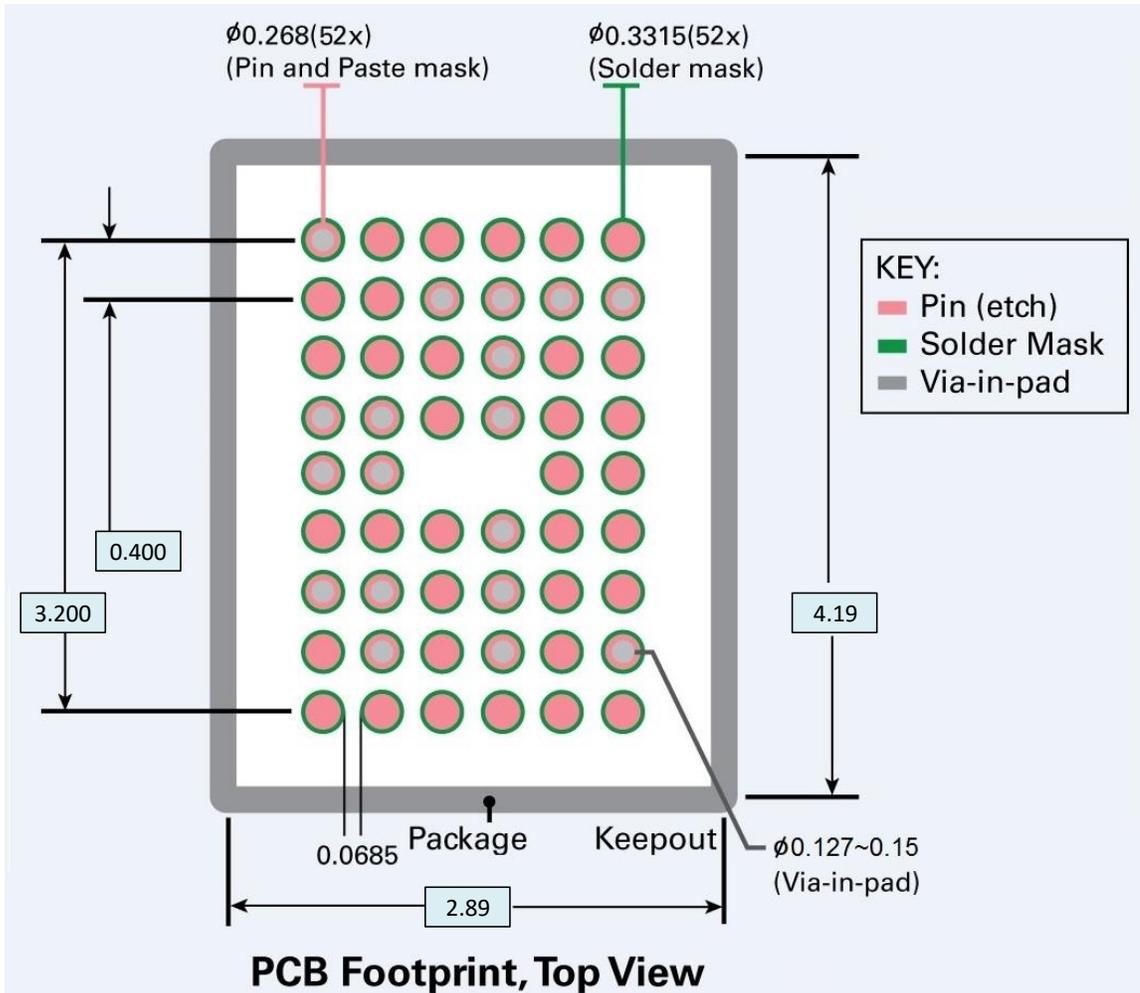
Figure 10. P9221 Typical GND Noise Areas



3. PCB Footprint Design

The P9221-R package is a fine-pitch WLCSP package. Improper footprint design can lead to solder shorts or open circuits. Poor PCB footprint design can also cause the performance to be degraded by limiting the robustness and diameter of the pin-to-board connections. To minimize the risk of such events, design the PCB pin pads and via-in-pads using the following guidance. Non-solder-mask defined pins are recommended, and solder paste should be applied with stencil openings of 0.127mm to 0.268mm (recommendation: 0.19mm typical) based on stencil thickness and solder paste selected. The pin diameter should be set to 0.268mm; the solder mask should be 0.3315mm; and via-in-pads should be 0.127mm to 0.15mm diameter holes.

Figure 11. P9221-R Recommended PCB Footprint Dimensions



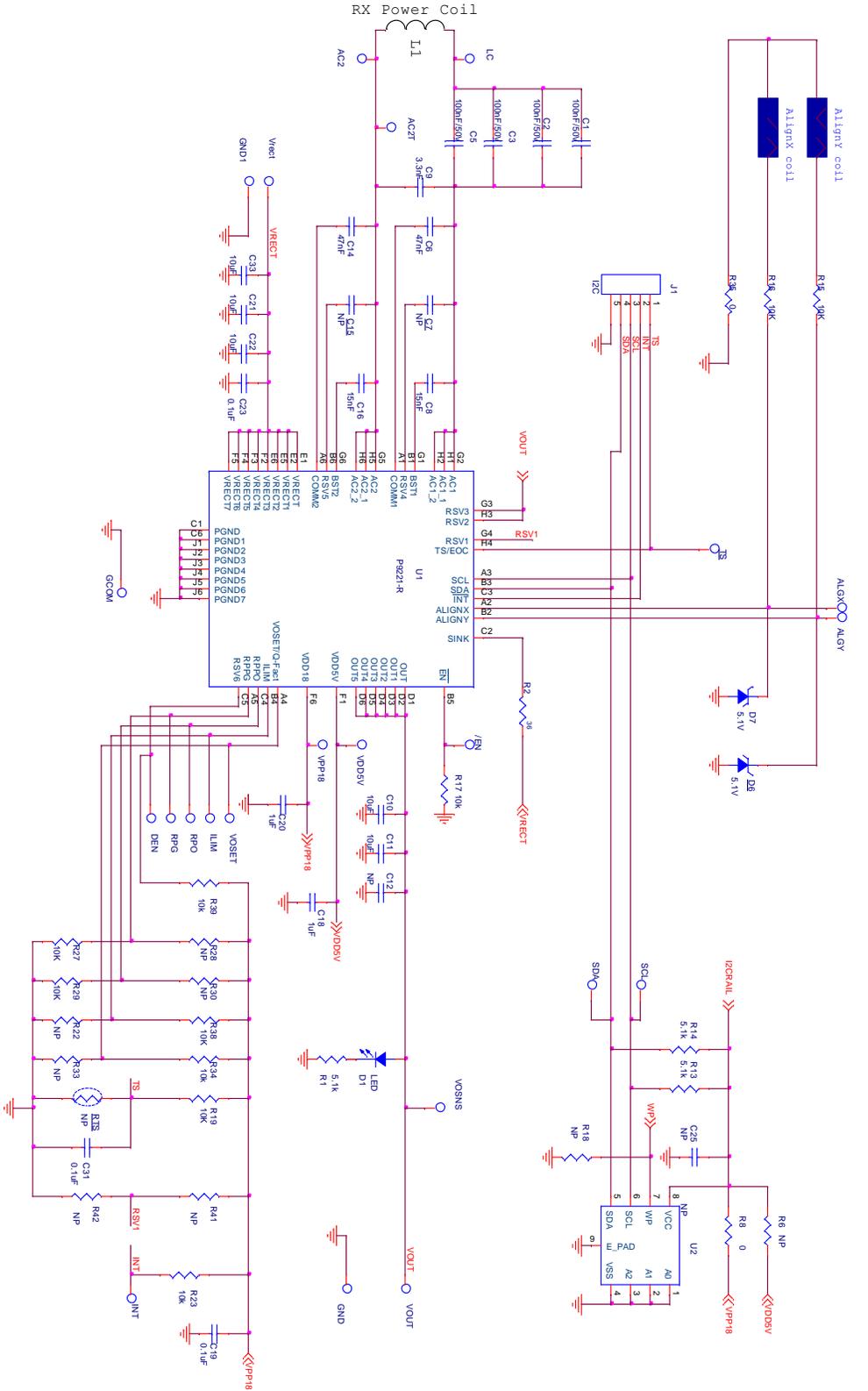
4. Audible Noise Suppression

Wireless power receiver solutions have been observed to produce audible noise. If sound is detected, there are several steps that can be taken to reduce or eliminate the noise. Some of the sources of the audible noise have been identified to be the following: the rectifier capacitors, the Rx coil ferrite, and the communication capacitors. Typically, the rectifier capacitors are the most significant cause of audible noise. This is due to the WPC communication signals being generating in the audible frequency range and the use of small-form factor ceramic capacitors. The noise occurs due to the piezoelectric effect of ceramic capacitors. The capacitors constrict and expand while providing the communication pulses, and this noise is amplified as it flexes the PCB. The primary solution to this issue is to use low-acoustic noise capacitors. Alternatively, higher voltage rated components can have superior piezoelectric properties that can reduce the audible noise. Additionally, placing the capacitors on both sides of the PCB (directly above and below each other) counters the piezoelectric forces applied to the PCB (cancels the force by each capacitor). Another method is to add slots through the PCB on both outer sides of the capacitors or directly under each capacitor. One additional approach is to place additional lower capacitance value components in parallel to reduce the mechanical force of the piezoelectric effect per component.

For any additional questions, contact IDT technical support (see the last page for contact information).

5. Application Schematics, Bill of Materials (BOM), and Board Layout

Figure 12. Application Schematics



P9221-R MM EV Board V2.2

Table 1. Application Board Bill of Materials (BOM) V2.2

Item	Reference	Quantity	Value	Description	Part number	PCB Footprint
1	AC2T, VDD5V, VPP18, VOSET, TS, SDA, SCL, RPO, RPG, INT, ILIM, GCOM, DEN, ALGY, ALGX, /EN	16	PTH_TP	Test Pad		10MIL_35PAD
2	AC2, LC	2	NP	TEST POINT		test_pt_sm_135x70
3	C1, C2, C3, C5	4	100nF	CAP CER 0.1μF 50V X5R 0402	GRM155R61H104KE19D	0402
4	C6, C14	2	47nF	CAP CER 0.047μF 50V X7R 0402	C1005X7R1H473K050BB	0402
5	C7, C15	2	NP	CAP CER 0.047μF 50V X7R 0402	C1005X7R1H473K050BB	0402
6	C8, C16	2	15nF	CAP CER 0.015μF 50V X7R 0402	GRM155R71H153KA12J	0402
7	C9	1	3.3nF	CAP CER 3300PF 50V X7R 0402	CL05B332KB5NNNC	0402
8	C10, C11, C21, C22, C33	5	10μF	CAP CER 10μF 25V X5R 0603	CL10A106MA8NRNC	0603
9	C12	1	NP	CAP CER 10μF 25V X5R 0603	CL10A106MA8NRNC	0603
10	C18,C20	2	1μF	CAP CER 1μF 10V X5R 0402	GRM155R61A105KE15D	0402
11	C19,C31	2	0.1μF	CAP CER 0.1μF 10V X5R 0201	C0603X5R1A104K030BC	0201
12	C23	1	0.1μF	CAP CER 0.1μF 25V X5R 0201	CL03A104KA3NNNC	0201
13	C25	1	NP	CAP CER 0.1μF 10V X5R 0201	C0603X5R1A104K030BC	0201
14	D1	1	LED	LED GREEN CLEAR 0603 SMD	150 060 GS7 500 0	0603_diode
15	D6,D7	2	5.1V	DIODE ZENER 5.1V 100MW 0201	CZRZ5V1B-HF	0201
16	GND1, VRECT, VOUT, VOSNS, GND	5	Test Point	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_135x70
17	J1	1	I ² C	HEADER_1X5_0P1PITCH60P42D	68002-205HLF	header_1x5_0p1Pit ch60p42d
18	RTS	1	NP			NTC2
19	R1, R13, R14	3	5.1kΩ	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	0402
20	R2	1	36Ω	RES SMD 36 OHM 5% 1/2W 0805	ERJ-P06J360V	0805
21	R6	1	NP	RES SMD 0.0OHM JUMPER	ERJ-2GE0R00X	0402
22	R8	1	0Ω	RES SMD 0.0OHM JUMPER 1/10W 0402	ERJ-2GE0R00X	0402
23	R15, R16	2	10KΩ	RES SMD 10K OHM 1% 1/10W 0603	RC0603FR-0710KL	0603
24	R17, R19, R23, R27, R29, R34, R38, R39	8	10kΩ	RES SMD 10K OHM 5% 1/16W 0402	CRCW040210K0JNEDIF	0402

Item	Reference	Quantity	Value	Description	Part number	PCB Footprint
25	R18, R22, R28, R30, R33, R41, R42	7	NP	RES SMD 10K OHM 5% 1/16W 0402	CRCW040210K0JNEDIF	0402
26	R35	1	0Ω	RES SMD 0.0OHM 1/10W 0603	MCR03EZPJ000	0603
27	U1	1	P9221-R	MP Wireless power receiver	P9221-R	csp52_2p64x3p94_0p4mm
28	U2	1	NP	IC EEPROM 128KBIT 400KHZ 8TDFN	24AA128T-I/MNY	TDFN08

Figure 13. Silkscreen – Top of Board

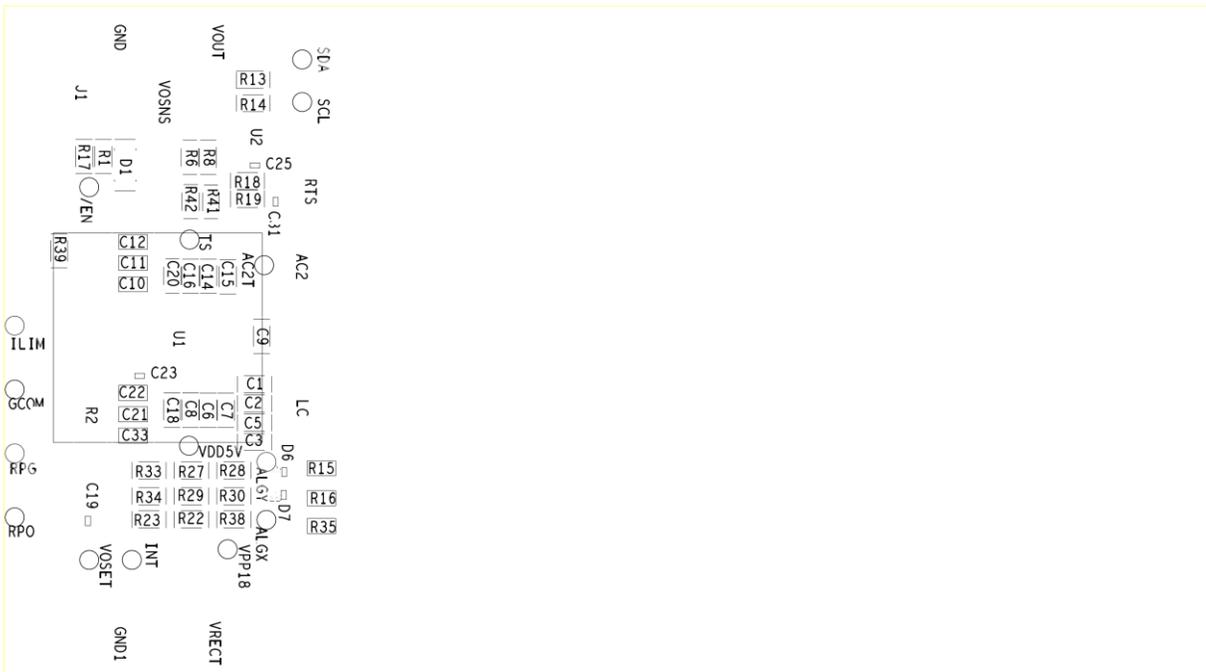


Figure 14. Silkscreen – Bottom of Board

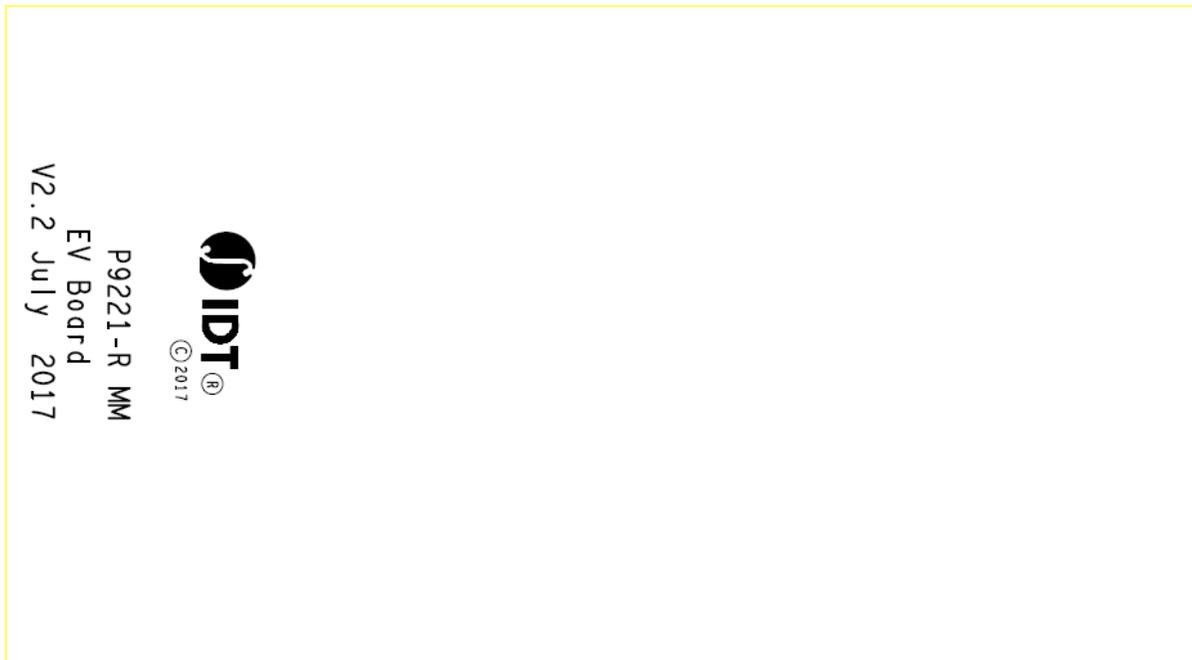


Figure 15. Top Copper Layer

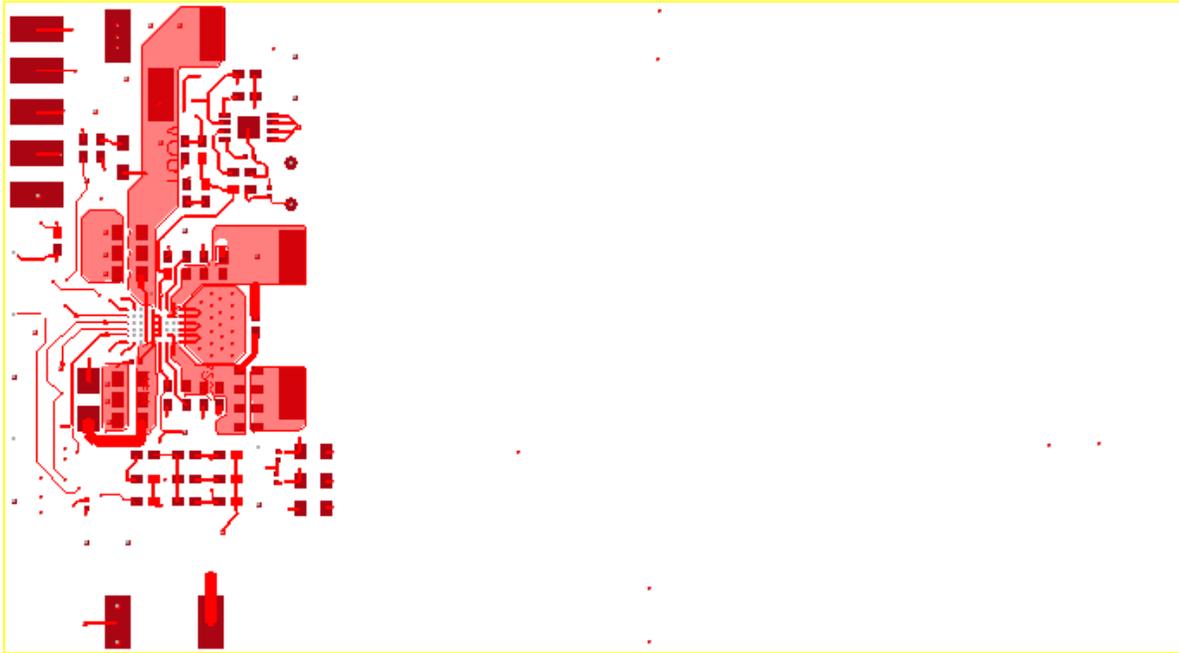


Figure 16. L2 Copper Layer

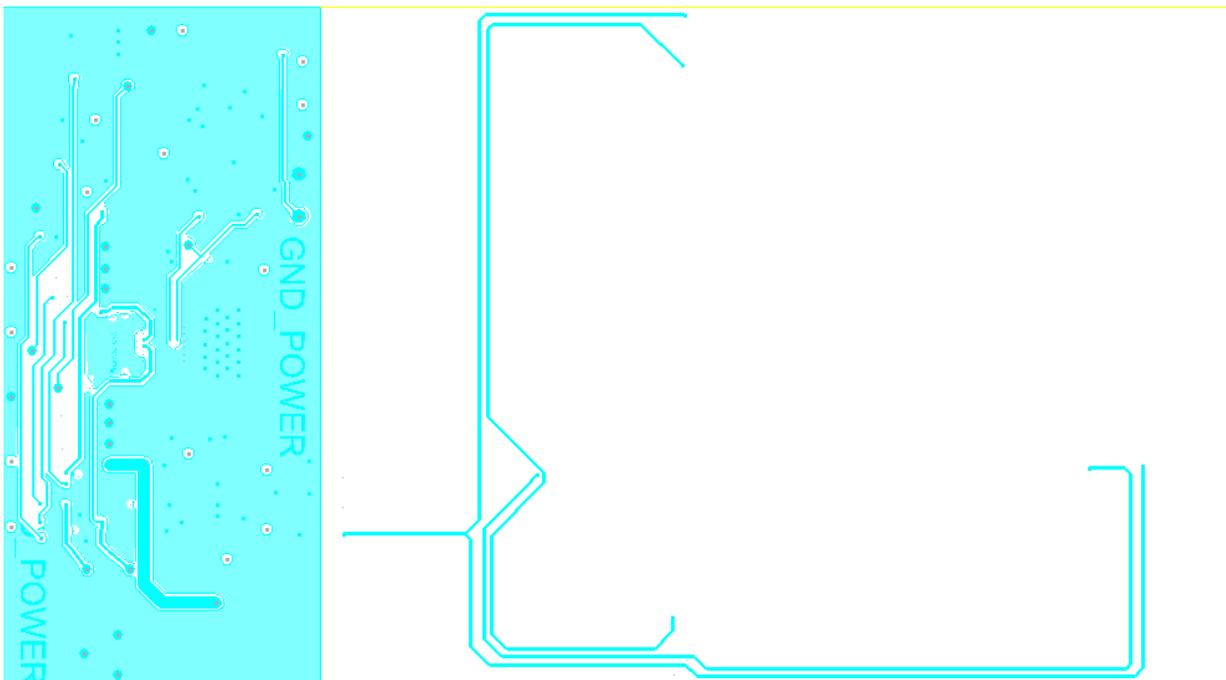


Figure 17. L3 Copper Layer

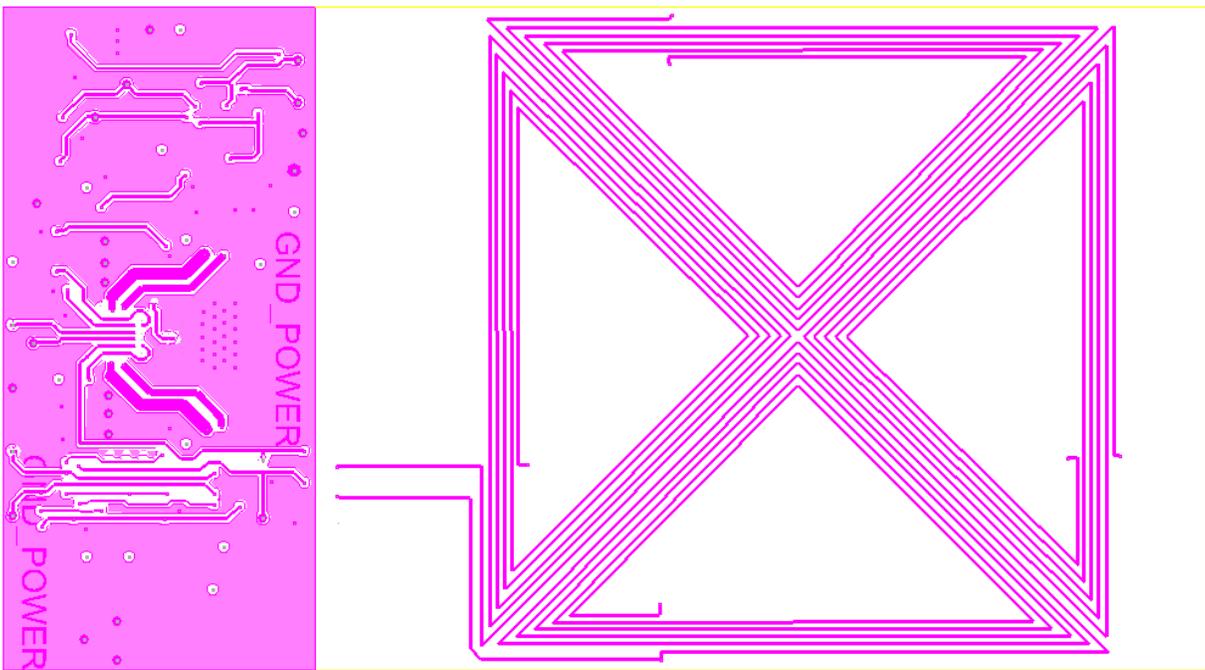
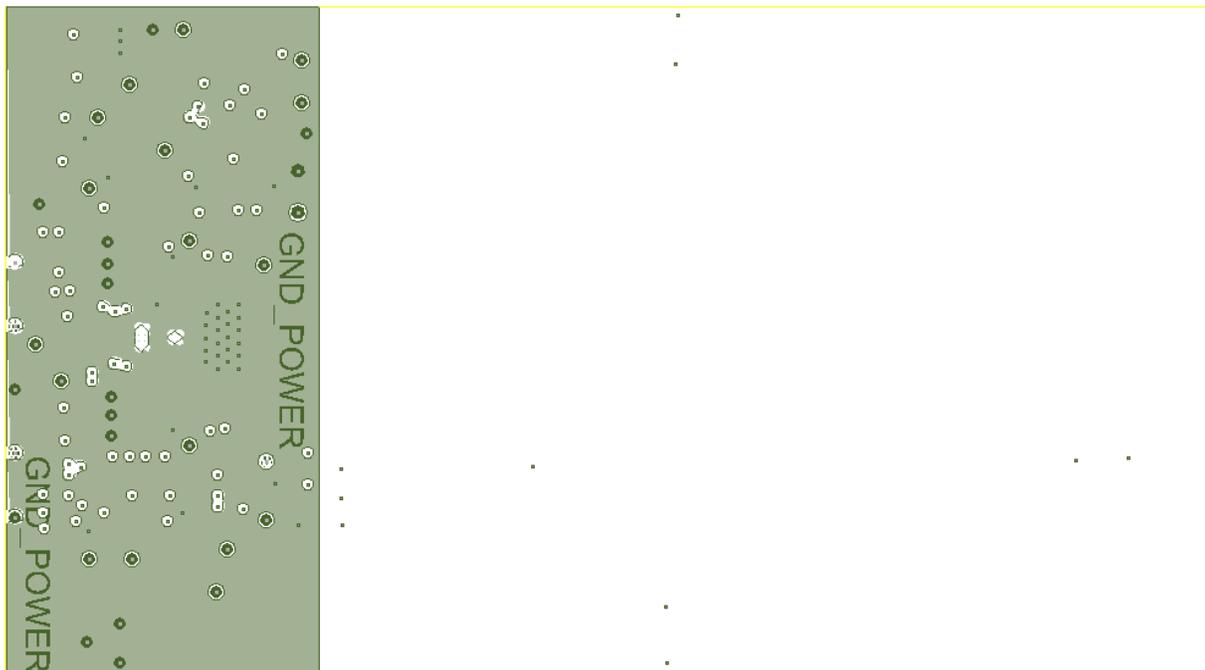


Figure 18. Bottom Copper Layer



6. Revision History

Revision Date	Description of Change
April 24, 2018	<ul style="list-style-type: none">▪ Updates for V2.2 of the P9221-R-EVK.▪ Minor edits.
December 22, 2016	Initial release of document.

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