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Renesas Electronics Corporation

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Introduction

The LCE-789177-EM is an emulation board or daughterboard for the LCE-K0S development system for NEC's 8-bit μ PD789177 subseries microcontrollers. Combining this board with the LCE-78K0S allows you to efficiently emulate any μ PD789177 subseries device. The LCE-789177-EM is shipped with the following contents:

- LCE-789177-EM daughterboard
- User's manual
- 50-pin ribbon cable
- CD-ROM containing debugger, compiler, assembler, and documentation

Figure 1. System Configuration

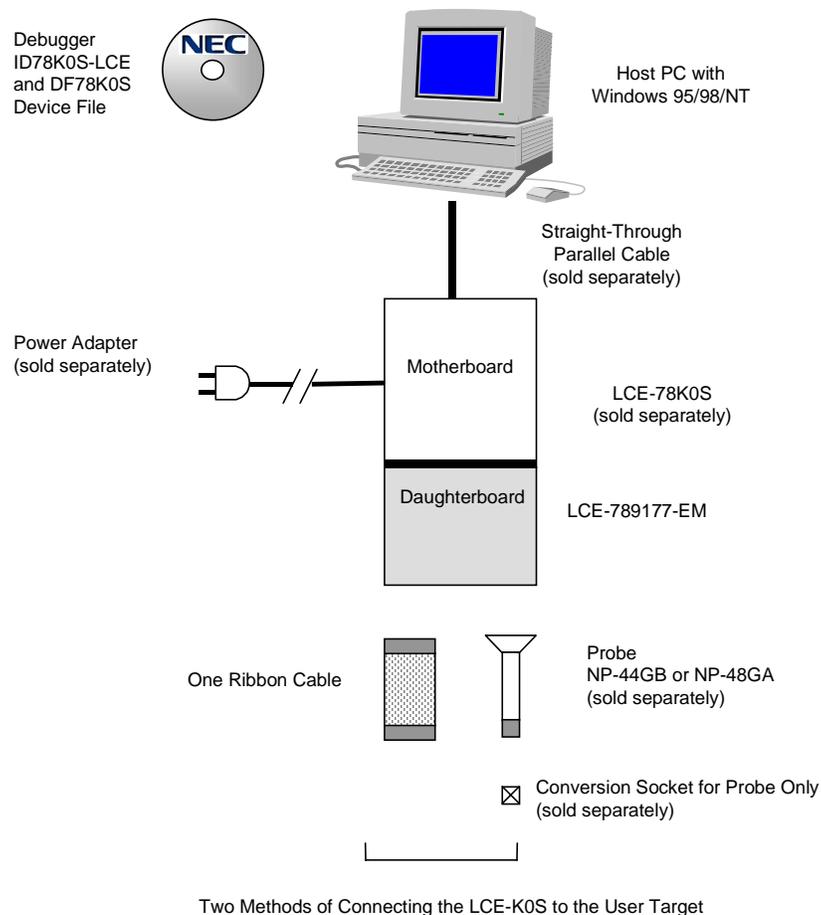


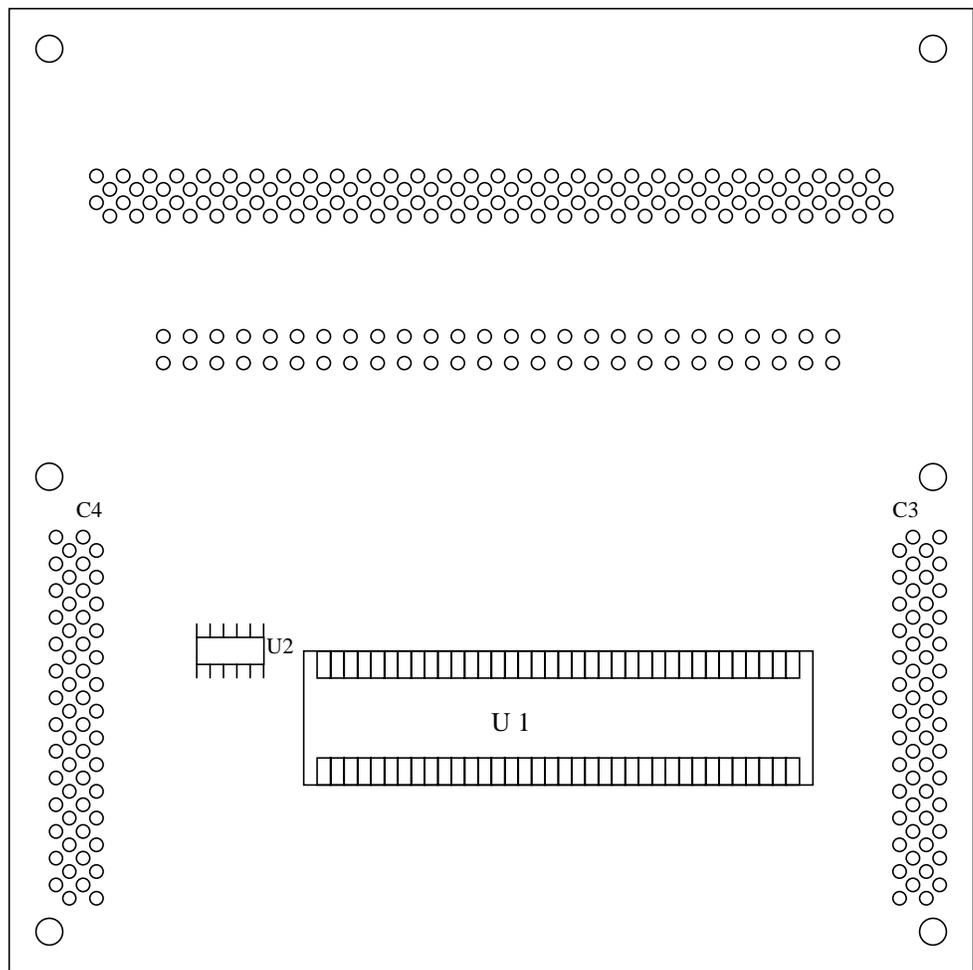
Table 1. Basic Specifications

| Parameter | Description |
|------------------------|--|
| Target device | μPD789166 |
| | μPD789167 |
| | μPD789176 |
| | μPD789177 |
| | μPD78F9177 |
| Clock supply | Internal: installed on the motherboard |
| | External: pulse input |
| Low-voltage compatible | 1.8 to 5.5 volts |

Components

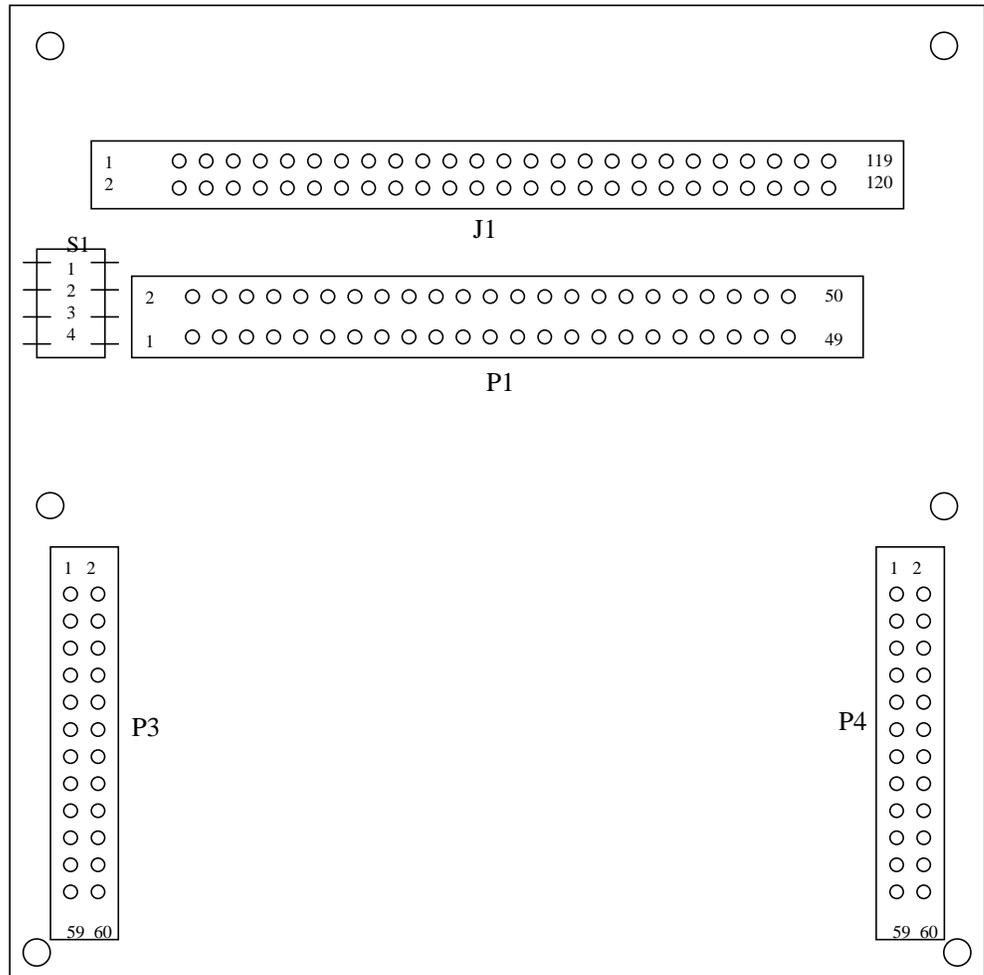
The LCE-789177-EM daughterboard mates with the LCE-78K0S motherboard. As shown in Figure 2, a bottom view of the daughterboard, U1 is the Realchip that provides peripherals unique to the μPD789177 devices.

Figure 2. Bottom View of Daughterboard



In the top view shown in Figure 3, J1 and P1 are connectors to the user target. These connectors contain all of the pins available on the device. J1 is a KEL connector for the probe, while P1 is a dual-row, male-shrouded header with latching levers for the ribbon cables. See Tables 2-4 for pin assignments. S1 is a DIP switch for enabling or disabling pull-up resistors on the input pins for mask ROM. P3 and P4 are connectors for the motherboard, which attaches to the top of the daughterboard.

Figure 3. Top View of Daughterboard



Ribbon Cable

The ribbon cable is a 50-pin female-to-female cable that connects the LCE-K0S to the user target. Alternatively, an emulation probe may be used. One end of the ribbon cable connects to the daughterboard and the other to the target. The side of the ribbon cable with a red stripe is pin 1.

Table 2. P1 Pin Assignments

| P1 Connector | 48-Pin TQFP Package | 44-Pin PQFP Package | Signal Name | Note |
|--------------|---------------------|---------------------|---------------------------|---|
| 1 | | | | GND on probe cable |
| 2 | 1 | 1 | P60/ANI0 | |
| 3 | 2 | 2 | P61/ANI1 | |
| 4 | 3 | 3 | P62/ANI3 | |
| 5 | 4 | 4 | P63/ANI3 | |
| 6 | 5 | 5 | P64/ANI4 | |
| 7 | 6 | 6 | P65/ANI5 | |
| 8 | 7 | 7 | P66/ANI6 | |
| 9 | 8 | 8 | P67/ANI7 | |
| 10 | 9 | 9 | AVSS | Connected to GND on emulation board and probe |
| 11 | 10 | 10 | P10 | |
| 12 | 11 | 11 | P11 | |
| 13 | 12 | --- | IC2 | Not connected on probe |
| 14 | 13 | 12 | P30/INTP0/T181/CPT90 | |
| 15 | 14 | 13 | P31/INTP1/TO81 | |
| 16 | 15 | 14 | P32/INTP2/TO90 | |
| 17 | 16 | 15 | P33/INTP3/TO82/BZO90 | |
| 18 | 17 | 16 | P20/SCK20/ASCK20 | |
| 19 | 18 | 17 | VDD1 | Probe VDD1 tied to VDD0; voltage sense |
| 20 | 19 | --- | IC2 | Not connected on probe |
| 21 | 20 | 18 | P21/SO20/TxD20 | |
| 22 | 21 | 19 | P22/SI20/RxD20 | |
| 23 | 22 | 20 | P23/SCL0 | |
| 24 | 23 | 21 | P24/SDA0 | |
| 25 | 24 | 22 | VPP | Not connected on probe |
| 26 | 25 | 23 | XT2 | Not connected on probe |
| 27 | 26 | 24 | XT1 | External secondary clock input from target |
| 28 | 27 | 25 | $\overline{\text{RESET}}$ | Negative true |
| 29 | 28 | 26 | X2 | Not connected on probe |
| 30 | 29 | 27 | X1 | External clock input from target oscillator |
| 31 | 30 | 28 | VSS0 | Tied to GND |
| 32 | 31 | --- | IC2 | Not connected on probe |
| 33 | 32 | 29 | VDD0 | Probe VDD1 tied to VDD0; voltage sense |
| 34 | 33 | 30 | P25/TI80/SS20 | |

Table 2. P1 Pin Assignments (continued)

| P1 Connector | 48-Pin TQFP Package | 44-Pin PQFP Package | Signal Name | Note |
|--------------|---------------------|---------------------|-------------|---------------------------|
| 35 | 34 | 31 | P26/TO80 | |
| 36 | 35 | 32 | P00 | |
| 37 | 36 | 33 | P01 | |
| 38 | 37 | 34 | P02 | |
| 39 | 38 | 35 | P03 | |
| 40 | 39 | 36 | P04 | |
| 41 | 40 | 37 | VSS1 | Tied to GND |
| 42 | 41 | 38 | P05 | |
| 43 | 42 | 39 | P50 | |
| 44 | 43 | 40 | P51 | |
| 45 | 44 | --- | IC0 | Not connected on probe |
| 46 | 45 | 41 | P52 | |
| 47 | 46 | 42 | P53 | |
| 48 | 47 | 43 | AVDD | Connected to target VDD |
| 49 | 48 | 44 | AVREF | Connected to target AVREF |
| 50 | | | | GND on probe cable |

Emulation Probe (Optional)

In place of a ribbon cable, an emulation probe can be used to connect the LCE to the user target, provided the target has a conversion socket/adaptor installed.

Table 3. NP-44GB Emulation Probe Pin Assignments

| Emulation Device Pin No. | J1 Pin No. | Emulation Device Pin No. | J1 Pin No. |
|--------------------------|------------|--------------------------|------------|
| 1 | 104 | 23 | 18 |
| 2 | 103 | 24 | 17 |
| 3 | 100 | 25 | 22 |
| 4 | 99 | 26 | 21 |
| 5 | 94 | 27 | 28 |
| 6 | 93 | 28 | 27 |
| 7 | 30 | 29 | 92 |
| 8 | 29 | 30 | 91 |
| 9 | 24 | 31 | 98 |
| 10 | 23 | 32 | 97 |
| 11 | 20 | 33 | 102 |
| 12 | 47 | 34 | 73 |
| 13 | 48 | 35 | 72 |
| 14 | 51 | 36 | 69 |
| 15 | 52 | 37 | 70 |
| 16 | 57 | 38 | 63 |
| 17 | 58 | 39 | 64 |
| 18 | 59 | 40 | 61 |
| 19 | 60 | 41 | 62 |
| 20 | 55 | 42 | 65 |
| 21 | 56 | 43 | 66 |
| 22 | 49 | 44 | 71 |

Table 4. NP-48GA Emulation Probe Pin Assignments

| Device Pin No. | J1 Pin No. | Device Pin No. | J1 Pin No. |
|----------------|------------|----------------|------------|
| 1 | 104 | 25 | 18 |
| 2 | 103 | 26 | 17 |
| 3 | 100 | 27 | 22 |
| 4 | 99 | 28 | 21 |
| 5 | 94 | 29 | 28 |
| 6 | 93 | 30 | 27 |
| 7 | 30 | 31 | 101 |
| 8 | 29 | 32 | 92 |
| 9 | 24 | 33 | 91 |
| 10 | 23 | 34 | 98 |
| 11 | 20 | 35 | 97 |
| 12 | 19 | 36 | 102 |
| 13 | 47 | 37 | 73 |
| 14 | 48 | 38 | 72 |
| 15 | 51 | 39 | 69 |
| 16 | 52 | 40 | 70 |
| 17 | 57 | 41 | 63 |
| 18 | 58 | 42 | 64 |
| 19 | 50 | 43 | 61 |
| 20 | 59 | 44 | 74 |
| 21 | 60 | 45 | 62 |
| 22 | 55 | 46 | 65 |
| 23 | 56 | 47 | 66 |
| 24 | 49 | 48 | 71 |

Table 5. Emulation Probe and Socket for μ PD789177 Subseries

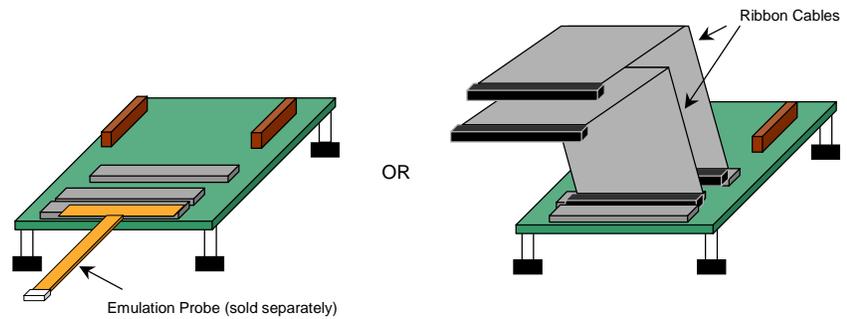
| Package | Target Device | Emulation Probe + Conversion Socket |
|-------------|-------------------|--|
| 44-Pin QFP | μ PD789166GB | NP-44GB + EV-9200G-44 or NP-44GB-TQ + EV-TGB-044SAP |
| | μ PD789167GB | |
| | μ PD789176GB | |
| | μ PD789177GB | |
| | μ PD78F9177GB | |
| 48-Pin TQFP | μ PD789166GA | NP-48GA + EV-TGA-48SDP |
| | μ PD789167GA | |
| | μ PD789176GA | |
| | μ PD789177GA | |
| | μ PD78F9177GA | |

Assembly

This procedure explains how to connect the LCE-789177-EM to the LCE-78K0S motherboard.

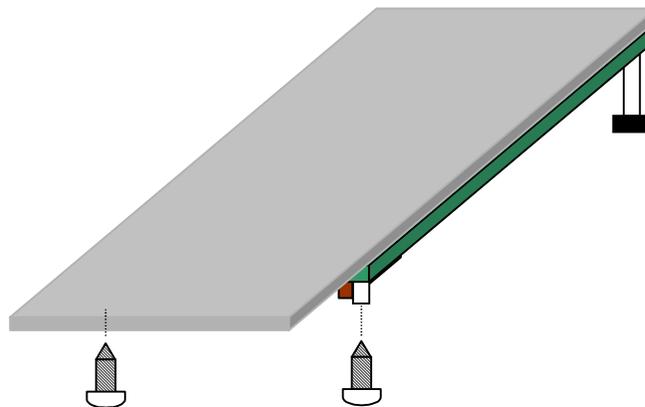
1. Connect the probe or ribbon cable to their respective connectors on the LCE-789177-EM (Figure 4). Note that the number of KEL connectors, headers, and ribbon cables shown in Figure 4 varies for each emulation board. The LCE-789177 has one KEL connector, one header, and one ribbon cable.

Figure 4. Connections for Emulation Probe or Ribbon Cables



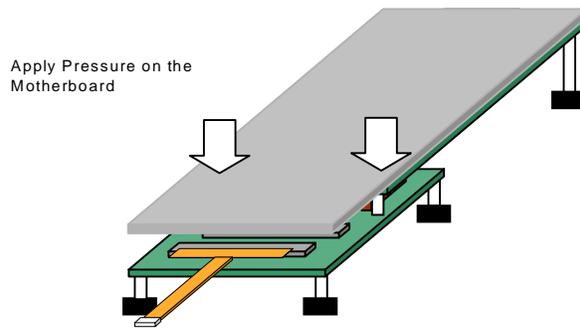
2. Make sure power is off from the LCE-78K0S motherboard.
3. Remove the two screws at the bottom of the standoffs on the motherboard (Figure 5).

Figure 5. Screws on Bottom of Motherboard



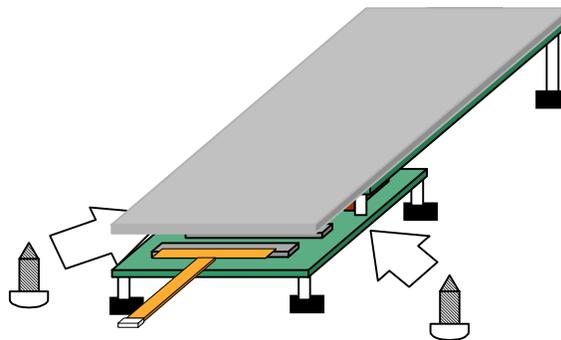
4. With the daughterboard on a stable surface, connect the motherboard on the daughterboard by gently applying pressure on the mating connectors. Avoid applying too much pressure on the plastic cover (Figure 6).

Figure 6. Daughterboard Mating Connectors



5. Replace the screws on the bottom of the daughterboard to securely connect it to the motherboard (Figure 7).

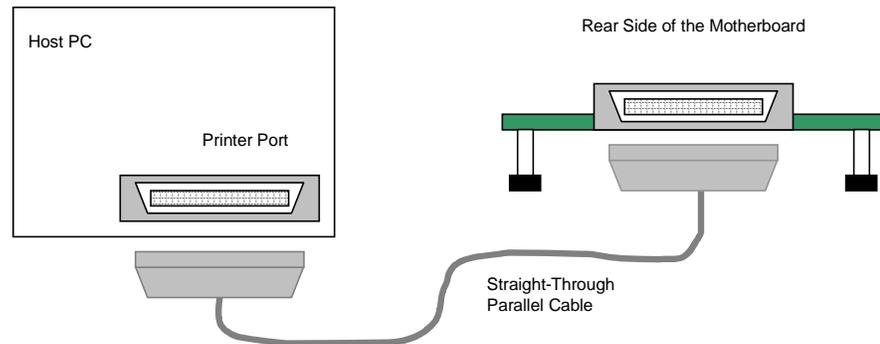
Figure 7. Connection to Motherboard



6. Connect the loose end of the probe or ribbon cable to the user target. Refer to Tables 2-4 for pin assignments.

7. With a 25-pin male-to-male parallel cable (included in the motherboard package), connect the LCE-K0S system to the host computer (Figure 8).

Figure 8. Connection to Host PC



8. With the power adapter connected, turn the switch to the ON position. The green LED turns on when power is supplied to the system.
9. Launch the debugger from your PC.



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