

Using the Evaluation Board

EL7531 is a high efficiency 1A synchronous step-down regulator in a tiny MSOP10 package. It operates at PFM mode at light load, automatically switches to PWM mode when the load increases to about 200mA. The no load quiescent current is only 120μA. The internal compensation makes it possible for the full-featured 1A converter to occupy less than 0.18 in² of PCB area with all components on one side.

1. Output Adjustment

Use R₁ and R₂ to adjust output voltage according to the following formula:

$$V_O = 0.8 \times \left(1 + \frac{R_2}{R_1} \right)$$

2. Chip Enable

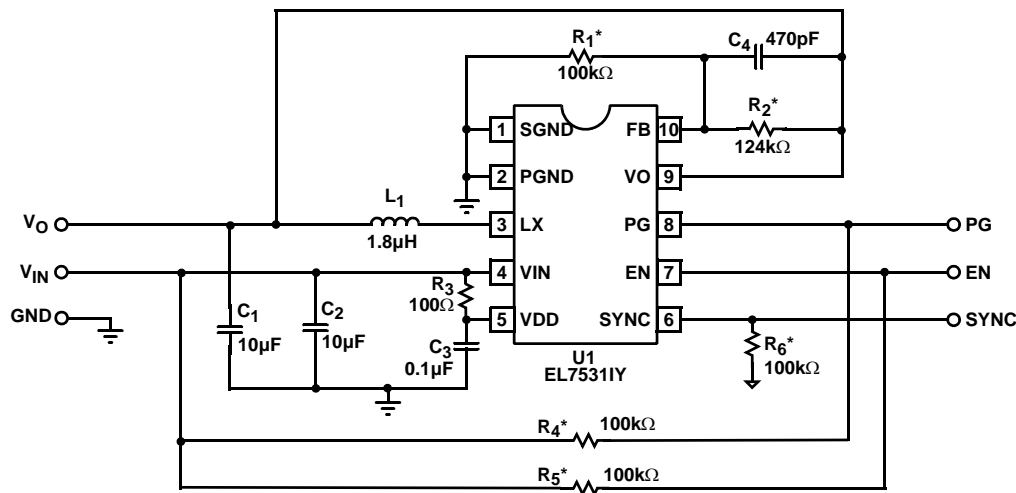
When EN pin is pulled to Ground, the regulator is disabled. It consumes less than 1μA of current. R₅ can be removed and EN connected to V_{IN} directly if this function is not needed, reducing the component count.

3. Sync Function

When a sync signal is fed to the SYNC pin, the converter will operate at PWM mode only. The sync frequency can be 1.6MHz up to 12MHz. When this pin is tied HIGH, the converter operates at forced PWM mode all the time with switching frequency of 1.5MHz. When this pin is tied LOW, it operates at auto-switchable PFM/PWM mode. Therefore, R₆ is not needed in actual application.

4. Power Good Function

When the output voltage reaches 90% of the set value, the PG goes to HIGH. Leave this pin open if the function is not used. Pull-up resistor R₄ can be removed.



* Optional depending on actual application.

FIGURE 1. DEMO BOARD SCHEMATIC

Evaluation Board Bill of Materials

REFERENCE DESIGNATOR	VALUE	PACKAGE	MANUFACTURER	MANUFACTURER'S PART NUMBER	MANUFACTURER'S PHONE NUMBER
C ₁ , C ₂	10μF/MLCC, X5R	1206	TDK	C3216X7R1A106K	847-803-6100
C ₃	0.1μF/MLCC, X5R	0603	Any		
L ₁	1.8μH		Coilcraft	1008PS-182M	847-639-6400
R ₂	124K, 1%	0603	Any		
R ₁ , R ₄ , R ₅ , R ₆	100K, 1%	0603	Any		
R ₃	100	0603	Any		
U ₁	EL7531IY	MSOP10	Intersil	EL7531IY	888-INTERSIL
C ₄	470pF	0603	ANY		

Demo Board Layout (Actual Size - 3" x 2")

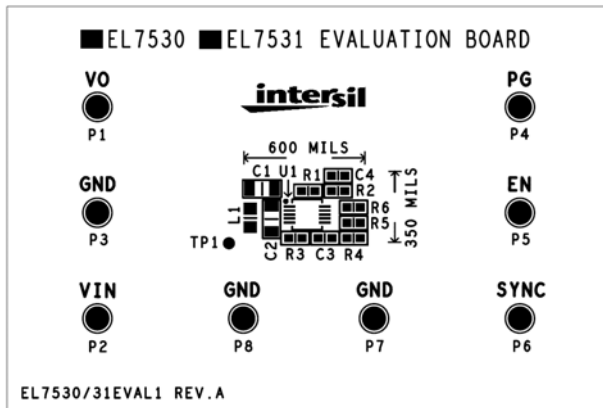


FIGURE 2. SILKSCREEN TOP

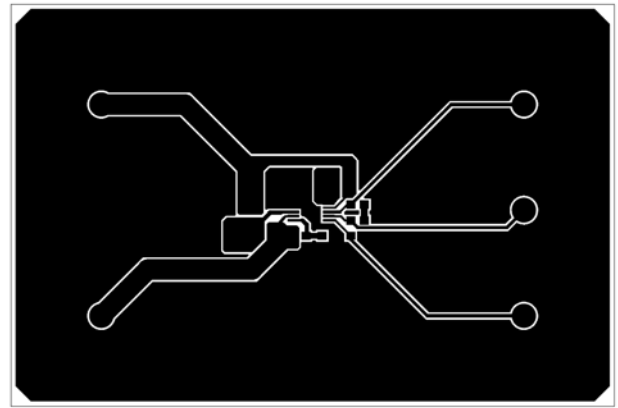


FIGURE 3. TOP LAYER

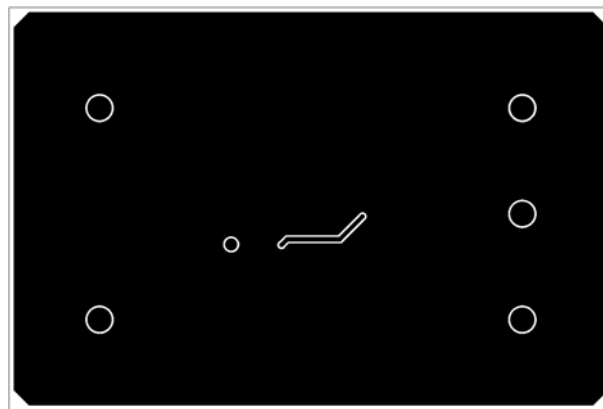


FIGURE 4. BOTTOM LAYER

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