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## **RENESAS TECHNICAL UPDATE**

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Product Category	MPU/MCU		Document No.	TN-SH7-A917A/E	Rev.	1.00		
Title	Clearing condition of PER and DER bits in Direct Memory Access Controller for Local Peripheral Modules (LBSC-DMAC/HPB-D)	Bus and	Information Category	Technical Notification				
		Lot No.						
Applicable Products	SH7734	All lots	Reference Document	SH7734 User's Manual: Hardware Rev.1.00 (R01UH0233EJ0100)				

We would like to inform you of a usage note regarding the clearing condition of the UltraATA Error Indication Register bit of the Direct Memory Access Controller for Local Bus and Peripheral Modules (LBSC-DMAC/HPB-DMAC) descried in the SH7734 User's Manual: Hardware.

The description on Table 6A.2 (1), List of LBSC-DMAC Registers, has been corrected as shown below.

[Before change]

Address (Bytes)	Name	Abbreviation		Access Size
H'FF8014CC	[Common to LBSC-DMAC]	UATTER	R/W	32
	UltraATA error indication register			

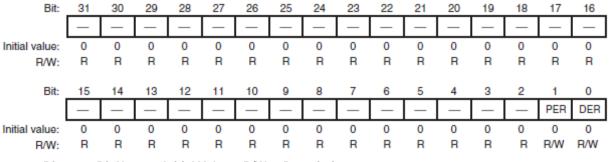
[After change]

Address (Bytes)	Name	Abbreviation		Access Size
H'FF8014CC	[Common to LBSC-DMAC]	UATTER	R/WC1	32
	UltraATA error indication register			



The description on section 6A.4.32, UltraATA Error Indication Register (UATTER), has been corrected as shown below.

## [Before change]



Bit	Bit Name	Initial Value	R/W	Description
31 to 2	_	All 0	R	Reserved
				These bits are always read as 0. The write value should always be 0.
1	PER	0	R/W	Indicates whether PIO access is executed for the area allocated to the ATA space during UltraATA DMA operation.
				(The PIO access attempted for the area allocated to the ATA space during UltraATA DMA operation is ignored.)
				<ol> <li>No PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation.</li> </ol>
				<ol> <li>PIO access has been executed for the area allocated to the ATA space during UltraATA DMA operation.</li> </ol>
0	DER	0	R/W	Indicates whether timeout occurs due to a temporary communication stop (no change in DSTROBE) during UltraATA DMA read operation. The timeout period is specified through UATTSR and UATMR2.
				(When reading)
				0: No timeout error has occurred.
				<ol> <li>A timeout error has occurred (interrupt is generated when enabled through UATIER).</li> </ol>
				(When writing)
				No timeout detection.

Note: For the UltraATA DMA operation, refer to section 6B, LBSC within Bus Bridge.

[After change]																
Bit	: 31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_	_
Initial value R/W		0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R
Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	_	_	_	_	_	_	_	_	_	_	_	_	_	_	PER	DER
Initial value		0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R	0 R/WC1	0 R/WC1
										п	n	n	n	-	Ny WCI	Ny WCI
Bi		Bit Na		Initial All 0	value	R/W		scripti								
31	to 2	_		All U		R Reserved  These bits are always read as 0. The write value should always be 0.							е			
1	1 PER 0					R/W 1	R/WC Indicates whether PIO access is executed for the ATA space during UltraAT DMA operation.									
(The PIO access attempted for the area allocat the ATA space during UltraATA DMA operation ignored.)																
0: No PIO access has been executed for the allocated to the ATA space during UltraATA operation.																
1: PIO access has been executed for the a allocated to the ATA space during Ultra operation.							DMA									
								[Clearing condition]								
							is i	gnored		bit cle ould be nis bit.						
0	0 DER 0 R/WC Indicates whether timeout occurs du communication stop (no change in I during UltraATA DMA read operatio period is specified through UATTSR				DSTR on. Th	STROBE) n. The timeout										
						(When reading)										
							1:0	No time	eout er	ror ha	s occu	rred.				
							<ol> <li>A timeout error has occurred (interrupt is generated when enabled through UATIER).</li> </ol>									
							-	hen wi	-							
								ut dete condit								
							Wr is i	iting 1 gnored	to this I. 0 sho	bit cle						
when clearing this bit.																

Note: For the UltraATA DMA operation, refer to section 6B, LBSC within Bus Bridge.

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