Microcontroller Technical Information

QB-78K0RFX3	Document No.	ZBG-	-CD-10-0001	1/2
In-Circuit Emulator for	Date issued	January 13, 2010		
78K0R/FB3, 78K0R/FC3, 78K0R/FE3,	Issued by	Development Tool Solution Group		
78K0R/FF3, 78K0R/FG3		Multipurpose Microcomputer Systems Division		
		Microcomputer Operations Unit		
Usage Restrictions		NEC Electronics Corporation		
Related documents	Notification		Usage restriction	
QB-78K0RFX3 User's Manual: ZUD-CD-09-0139-02	classification	Upgrade		
			Document modification	
			Other notification	

1. Affected product

Product	Outline	Control Code ^{Note}
QB-78K0RFX3	In-circuit emulator for 78K0R/FB3, 78K0R/FC3, 78K0R/FE3,	A, B, C
	78K0R/FF3, 78K0R/FG3	

Note The control code is the second digit from the left in the 10-digit serial number. To see if the product has been upgraded, click the ID78K0R-QB **Help** menu, select **About**, and then check the control code. X in **IECUBE** **** X F/W: V*.** is the control code.

2. New restriction

Restriction No. 6 has been added. See the attachment for details.

3. Workaround

See the attachment for details.

4. Modification schedule

Products in which No. 6 is corrected are scheduled for release as follows:

Accepting orders of corrected products (control code D): From January 29, 2010

Accepting orders for exchanging already shipped products

(upgrade by sending the product to NEC Electronics): From January 29, 2010 (upgrade by a user who uses a product with control code C): From January 22, 2010

* Note that this schedule is subject to change without notice. For the detailed release schedule of modified products, contact an NEC Electronics sales representative.

5. List of restrictions

See the attachment.

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6. Document revision history

QB-78K0RFX3, In-Circuit Emulator for 78K0R/FB3, 78K0R/FC3, 78K0R/FE3, 78K0R/FF3, 78K0R/FG3 - Usage Restrictions

Document Number	Issued on	Description
ZBG-CD-09-0042	August 24, 2009	Addition of restrictions (Nos. 3, 4, 5)
ZBG-CD-10-0001	January 13, 2010	Addition of restriction (No. 6)

Operating Precautions for QB-78K0RFX3

This document describes the items below. See the user's manual for cautions on using this emulator.

- Restrictions not applicable to the target device but applicable to this emulator
- Restrictions applicable to both the target device and this emulator, but for which correction is planned only for this emulator

Also see the following documents for the restrictions related to the target device:

- User's manual of target device
- Restrictions notification document for target device

1. Product Version

The product versions of NEC Electronics in-circuit emulators are indicated by a control code. The control code is the second digit from the left in the 10-digit serial number. To see if the product has been upgraded, click the ID78K0R-QB **Help** menu, select **About**, and then check the control code.

In Figure 2, **X** in **IECUBE** **** **X F/W**: **V***.** is the control code.

Figure 1. Checking the Control Code (Label on QB-78K0RFX3)

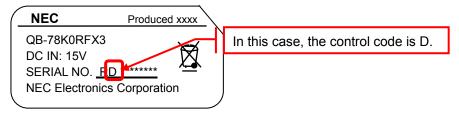
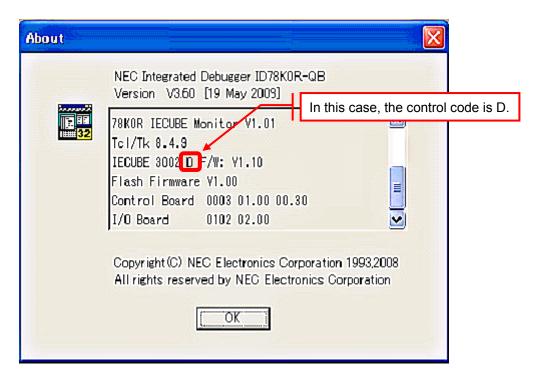


Figure 2. Checking the Control Code (ID78K0R-QB)



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2. Restrictions

2.1 List of restrictions

No.	Restrictions	Control Code		
		Α	В	С
1	Self-programming	×	×	0
2	Data flash	×	×	×
3	Restriction on A/D conversion	×	×	0
4	Restriction whereby the CPU deadlocks	×	0	0
5	Restriction on EEPROM emulation	×	×	0
6	Restriction on trace data when an interrupt occurs	×	×	×

-: Not relevant, x: Applicable, O: Corrected

2.2 Restriction details

No. 1 Self-programming

Description:

Self-programming is not supported.

Workaround:

There is no workaround.

Correction:

This issue has been corrected in QB-78K0RFX3 with control code C.

No. 2 Data flash

Description:

Data flash is not supported.

Workaround:

There is no workaround.

Correction:

Will be corrected in the library that supports data flash to be released.

No. 3 Restriction on A/D conversion

Description:

The A/D conversion error increases under the following conditions:

- (a) An external resistor is connected to an analog pin.
- (b) A/D conversion is performed in a short time in scan mode.

Workaround:

There is no workaround for either (a) or (b).

Correction:

This issue has been corrected in QB-78K0RFX3 with control code C.

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No. 4 Restriction whereby the CPU deadlocks

Description:

The CPU deadlocks if one of the following conditions is satisfied:

- (a) The clock frequency for the code flash area is changed (by using FSEL) while the CPU is running on the 1 MHz main clock.
- (b) The STOP instruction is executed immediately after PLLON is cleared to 0, with SELPLLS set to 1.

Workaround:

There is no workaround for either (a) or (b).

Correction:

This issue has been corrected in QB-78K0RFX3 with control code B.

No. 5 Restriction on EEPROM emulation

Description:

When executing error emulation on the code flash area, internal verification for EEPROM writing and internal verification for block erasure cannot be distinguished. As a result, if an error is specified to occur for the former, an error also occurs for the latter, and vice versa.

Workaround:

If error emulation is to be used for internal verification for EEPROM writing and internal verification for block erasure, do not debug these processes at the same time. Instead, execute error emulation separately for each verification process.

Correction:

This issue has been corrected in QB-78K0RFX3 with control code C.

No. 6 Restriction on trace data when an interrupt occurs

Description:

If interrupt servicing is executed under a specific condition, the trace result might be incorrect.

Although the correct trace result is not displayed, the instructions are executed correctly. The following describes the detailed condition and operations:

Condition:

Execution jumps to an interrupt vector immediately after executing one of the following instructions:

- (1) MOVW SP, #word
- (2) MOVW SP, AX
- (3) ADDW SP, #byte
- (4) SUBW SP, #byte

If the instruction fetches data from the ROM, the displayed trace result is incorrect if any instruction from (1) to (4) is executed.

If the instruction fetches data from the RAM, the displayed trace result is incorrect if instruction (3) or (4) is executed.

Operation:

If execution jumps to an interrupt vector immediately after executing one of the above instructions, the instruction that follows the above instructions is not supposed to be executed or displayed in the trace result. However, due to this problem, the following items are displayed in the trace result:

- The instruction that follows the above instructions
- · The incorrect vector address

Workaround:

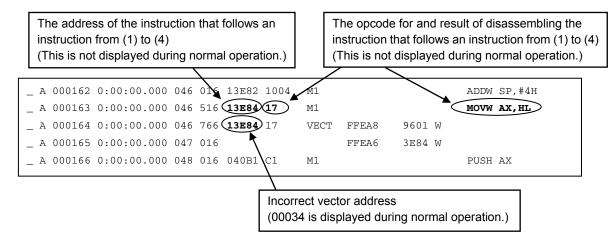
There is no workaround.

Correction:

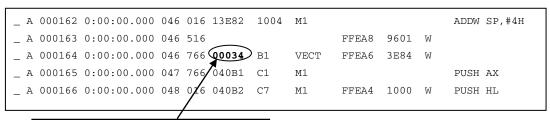
This issue will be corrected in products with control code D.

An example of trace data before and after correcting this restriction is shown below.

Before correction:



After correction:



The correct vector address is displayed.