Power Saving Solenoid Driver
SLG47105

A DC solenoid requires a significant current to activate and pull in its plunger. The current required to hold the plunger is much lower than the current for the pull-in. In the simple transistor driver, the hold current is as high as the activation current, wasting power in the solenoid resistance as heat. This application note shows a smart solenoid driver with current regulation that can save more than 60 percent of the power.

Contents

1. References

For related documents and software, please visit:

https://www.renesas.com/us/en/products/programmable-mixed-signal-asic-ip-products/greenpak-programmable-mixed-signal-products/hvpak

Download our free GreenPAK Designer software [1] to open the .gp files [2] and view the proposed circuit design. Use the GreenPAK development tools [3] to freeze the design into your own customized IC in a matter of minutes. Find out more in a complete library of application notes [4] featuring design examples as well as explanations of features and blocks within the GreenPAK IC.

[1] GreenPAK Designer Software, Software Download and User Guide

[2] AN-CM-342 Power Saving Solenoid Driver.hv, GreenPAK Design File

[3] GreenPAK Development Tools, GreenPAK Development Tools Webpage

[4] GreenPAK Application Notes, GreenPAK Application Notes Webpage

[5] SLG47105 Datasheet

[6] https://www.electronics-tutorials.ws/io/io_6.html

[7] https://www.sparkfun.com/products/11015

[8] https://www.adafruit.com/product/1512

2. Solenoid Principles

Solenoids are electromechanical actuators with a freely moving magnetic core called a plunger. In general, solenoids consist of a helicoidal coil of wire with a moving core made of iron.

When current is applied through the solenoid coil it generates a magnetic field inside it. This magnetic field generates a force to pull in the plunger. When the magnetic field generates enough force to pull in the plunger, it moves inside the solenoid until it reaches a mechanical stop position. When the plunger is already inside the solenoid, the magnetic field generates force to hold the plunger in place. When the current is removed from the solenoid coil, the plunger will return to its original position, pushed by a mounted spring in the solenoid.

Figure 1 shows the construction of a solenoid.

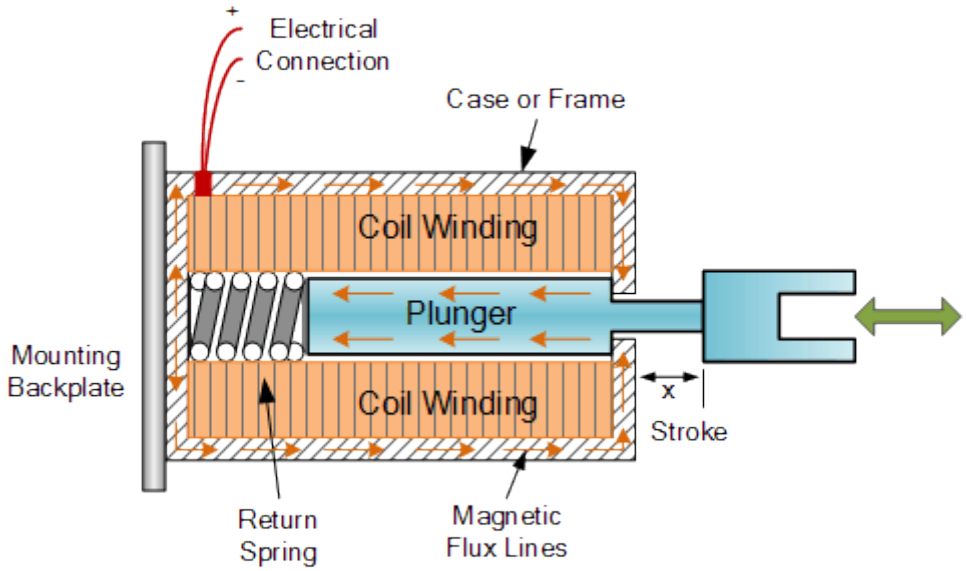

Figure 1. Solenoid construction drawing [1]

The most common approach to drive a solenoid is to apply the required voltage in the solenoid coil. This can usually be done using a single power transistor configured on the high side or on the low side. The power transistor will require a flywheel diode in parallel with the solenoid because the solenoid coil has a high inductance that will try to push a current into the transistor. Although this approach is simple and cheap, it is not

power efficient. This is because solenoids usually require significant current to pull in the plunger, but when the plunger is pulled in, it does not require the same amount of current. In the simple driver approach, when the plunger is pulled in, holding the plunger, the current applied to the solenoid mainly generates heat through its internal resistance. The power dissipated in internal solenoid resistance is given by Equation 1.

$$P_{Dissipated} = Resistance * Current^2 \ (Watts) \quad Equation\ 1$$

An alternative approach to overcome this issue is to use a current regulated driver to activate and deactivate the solenoid. This driver can apply a peak current value in the solenoid until it pulls in the plunger and, after that, it can reduce the current to a hold value. This strategy greatly reduces the power consumed in the internal solenoid resistance. Another advantage of this driver is the possibility to use a solenoid in a larger range of voltages. It means that the driver allows a solenoid designed to operate with a lower voltage (for example, 5 volts) to operate with a higher power voltage without damage (for example, with a 12 volt power supply).

The following sections will describe the implementation of the current regulated driver for two solenoids with the SLG47105 GreenPAK device.

3. GreenPAK Design Concept

This application note will show an example of how to independently drive two different solenoids using a single SLG47105 device. The SLG47105 device will control the current through the solenoids and will inform a user about each solenoid's status (on, off, or in a fault state). A conceptual block diagram showing its internal construction is shown in Figure 2.

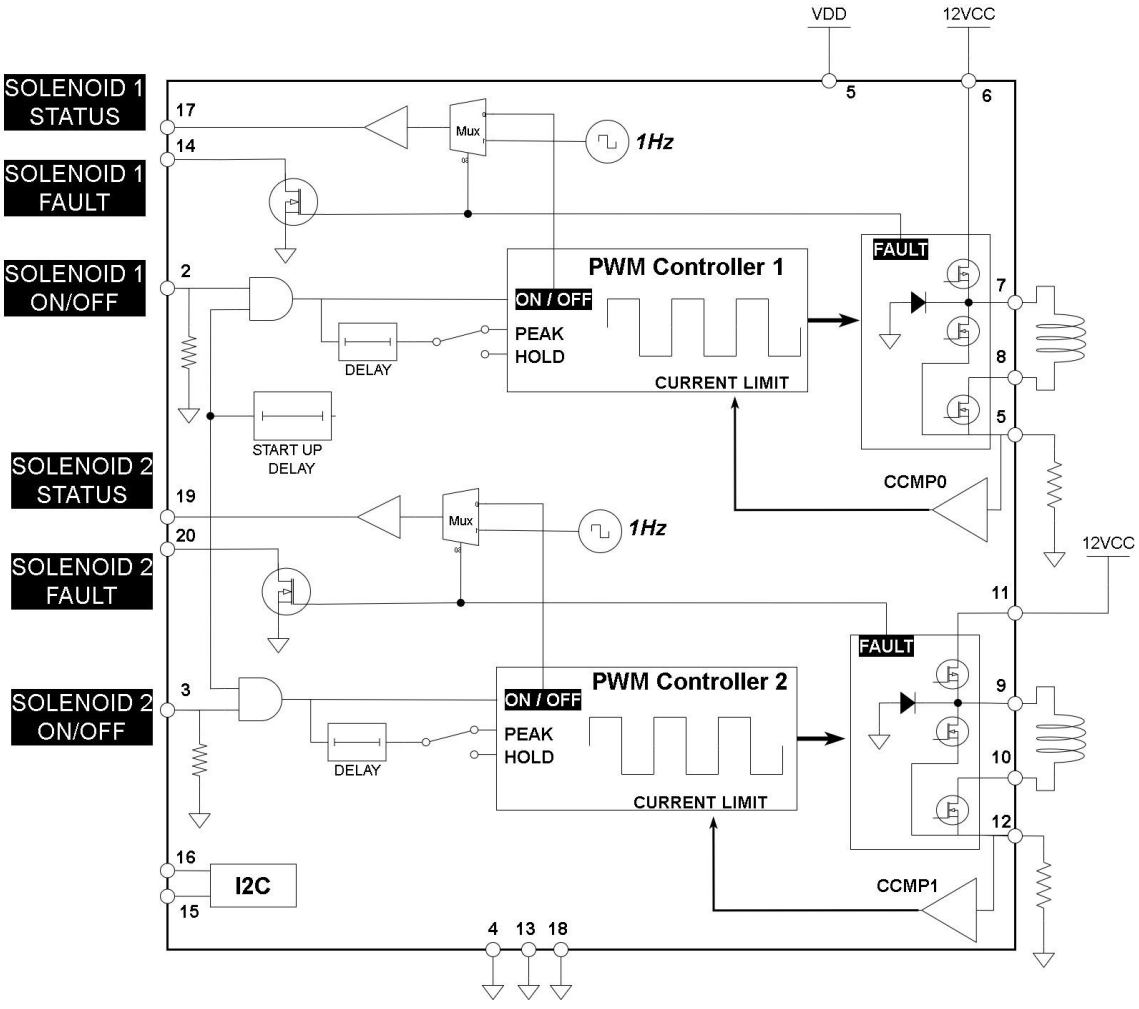

Figure 2. Block diagram of power-saving solenoid driver with SLG47105

The upper right side of the diagram shows how the High Voltage Output (HVOUT) block is configured internally and its connection to the external solenoid. The output connected to Pin 7 is configured as push-pull and the

output connected to pin 8 is configured as open drain. This open drain output is always kept turned on after startup delay. Pin 5 is internally connected to the N-Mosfet of Pin 8 and the internal current amplifier. Pin 5 is used to measure the solenoid current and compare it with an internal reference, sending the result of the comparison to the PWM Controller 1 block. The PWM Controller 1 block generates the PWM required to regulate the solenoid current connected to Pins 7 and 8. It has two setpoints, one for the solenoid peak current and another for the solenoid hold current. The On/Off input of the PWM Controller is activated by the AND port on its left. The AND port is connected to a startup delay block and Pin 2, which is used as the external interface to turn the solenoid on and off. The startup delay block connected to the AND port is used to guarantee that all internal blocks initialize properly at IC power-up. The output of the AND port is connected to another delay block. When the PWM controller is turned on it is configured to regulate the solenoid current at its peak current value. After a delay of 50 milliseconds, the delay block switches the PWM configuration to regulate the solenoid current at its hold current value.

The On/Off input of the PWM Controller 1 block is also connected to one of the inputs of a mux. The other mux input is connected to a square wave signal with a frequency of 1 hertz. The mux output is controlled by the FAULT signal in the HVOUT block. When the FAULT signal does not indicate any failure, the On/Off input is buffered through Pin 17, the SOLENOID 1 STATUS output. When the FAULT signal indicates a failure, the square wave signal is driven in this output. The SOLENOID 1 STATUS is designed to drive an external LED and show the solenoid status to a user. This status can be turned on, turned off, or in a fault state when the LED blinks at the square wave output frequency.

An additional FAULT output is provided as an open drain output in Pin 14. This output was designed to drive an external device, like a microcontroller.

Below the PWM Controller 1 is PWM Controller 2 and, as can be seen in Figure 2, the control structure around PWM Controller 2 is like PWM Controller 1.

The two FAULT outputs can be connected externally, since they are open drain outputs, supplying a single FAULT signal for an external device if any of the outputs fail.

An additional block is the I2C; it can be used to reconfigure peak and hold current setups.

4. Application Circuit

The typical application circuit, which is the same used alongside this application note, is shown in Figure 3. Figure 3 shows a simplified schematic of the typical application driving two different solenoids, identified as S1 and S2. As shown in the schematic, the driver is controlled by two push buttons connected to the 5 volt power supply. The solenoids are connected to the respective HVOUT outputs, together with a small 0.1Ω resistor. This resistor is used to allow an external current measurement through the solenoid and is not required for an end application. For the SLG47105 current measurements, two resistors of 0.11Ω are connected to Pins 5 and 12. The solenoid status outputs are connected to green LEDs and the fault outputs are connected to red LEDs.

In this application note we use two solenoids with completely different specifications. Table 1 shows the main specs of solenoids S1 and S2.

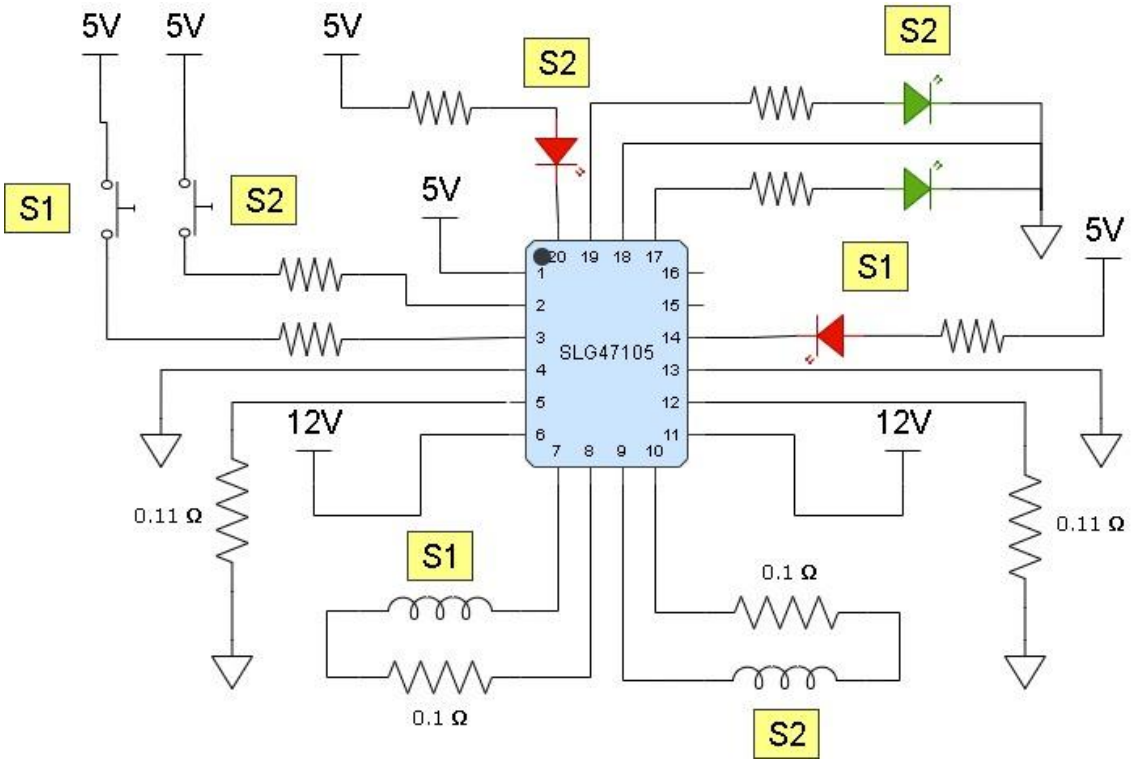

Figure 3. Simplified schematic of the electronic circuit for a typical application

Table 1. Specifications of the solenoids S1 and S2

Part Number	Schematic Reference	Nominal Voltage (Volts)	Nominal Current (mA)	Nominal Internal Coil Resistance (Ω)	Picture
ROB-11015 [2]	S1	5	1100	4.5	
Adafruit 1512 [3]	S2	12	650	18.46	

5. Solenoid Current Setup

The solenoid current will start with a regulated peak current value and, after an initial delay, it will decrease to a hold current value. We arbitrarily define that the hold current should be 20 percent of the nominal peak current. Based on this definition, it is possible to calculate the power dissipated in the hold current and the respective voltage at the sense resistor. The ideal solenoid current, dissipated power, and voltage at the sense resistor for each solenoid are shown in Table 2. The peak current value is the solenoid nominal current at the nominal voltage. The hold current is calculated by multiplying the peak current by 0.2 (20 percent). The peak and hold currents are calculated as the power dissipated over the internal solenoid resistance. The sense resistor is calculated using Ohm's Law through the sense resistor with 0.11Ω. The nominal coil resistance for S2 was calculated using the nominal solenoid voltage and its peak current values.

Table 2. Currents, dissipated power, and sense resistor voltages for the ideal configuration

Solenoid	Peak Current (mA)	Hold Current (mA)	Nominal Coil Resistance (Ω)	Peak Current Power (mW)	Hold Current Power (mW)	Sense Resistor Voltage - Peak (mV)	Sense Resistor Voltage - Hold (mV)
S1	1100	220	4.5	5500	217.8	121	24.2
S2	650	130	18.46*	7799	312	71.5	14.3

It is important to note that the reference voltage for comparison with the sense resistor voltage in SLG47105 is supplied by an internal 6-bit DAC. We must adjust the regulated current to the nearest SLG47105 internal reference voltage. Considering that, the following values of voltage references shown in Table 3 were selected. Table 3 shows the internal voltage and the respective currents. All internal values are 8 times the desired sense resistor voltage because the external voltage is amplified by 8 internally (described in more detail in the next sections). The peak and hold current values are calculated using Ohm's Law through the sense resistor.

Table 3. Internal voltage references and respective currents and dissipated power

Solenoid	Internal / External voltage reference for peak current (mV)	Internal / External voltage reference for hold current (mV)	Peak Current (mA)	Hold Current (mA)	Peak Current Power (mW)	Hold Current Power (mW)
S1	960 / 120	192 / 24	1090.9	218.18	5355.4	214.2
S2	2016 / 252	128 / 16	2290.9*	145.5	96.88*	390.8

The values marked with an (*) in Table 3 are achieved in calculations, but these values are impossible and do not represent reality. For S2, the peak current is not required current regulation, because the solenoid's internal resistance will limit the current. Considering this, we decided to set up the reference for the maximum current value.

6. GreenPAK Design

The complete internal SLG47105 design is shown in Figure 4. The following sub-sections will explain each part of this design.

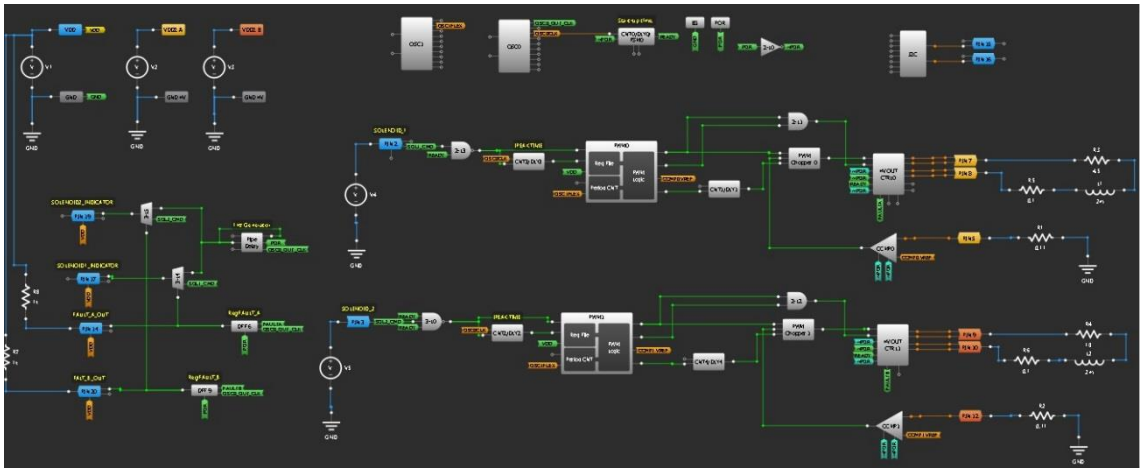

Figure 4. Overview of the complete SLG47105 internal design

6.1 OSC1

Figure 5 shows the OSC1 block and its internal configuration. The OSC1 block is the oscillator that supplies a clock signal for the PWM Controller blocks. The clock frequency is 6.25 Mhz. This block is always turned on.

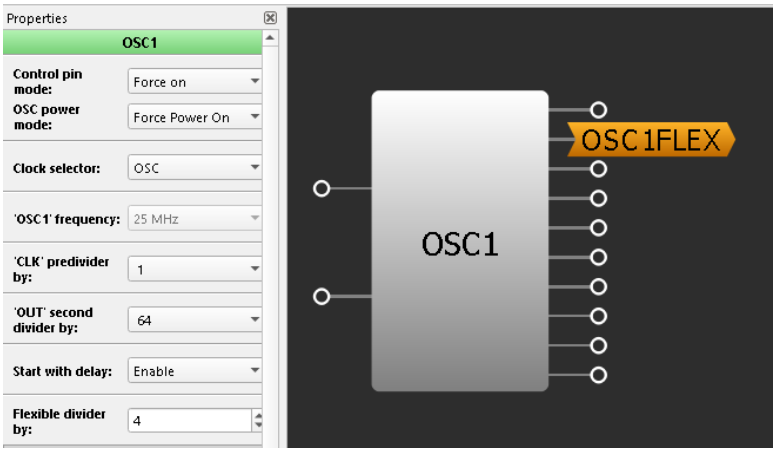

Figure 5. OSC1 block signals and internal configuration

6.2 OSC0

Figure 6 shows the OSC0 block and its internal configuration. OSC0 supplies a clock for the start-up delay block and the low-frequency square wave generator.

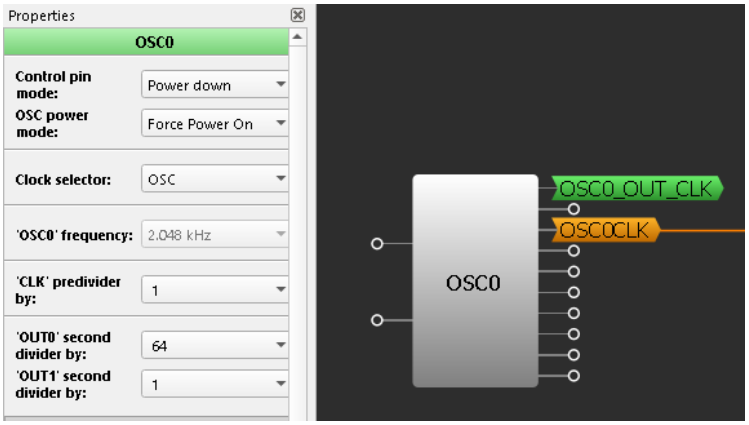

Figure 6. OSC0 block and its internal configuration

6.3 Start-up Time Delay Block

Figure 7 shows all the blocks used for the start-up time delay functionality. The main block in this functionality is the CNT0/DLY0/FSMO component. Its configuration is shown in Figure 7. The CNT0 will delay for almost 2 milliseconds the inverted POR signal, raising a positive edge in the READY signal connection after this initial time. This initial start-up time is required to guarantee that all internal and external components (power supply and capacitors) are ready to properly drive the power outputs and regulate the solenoid current.

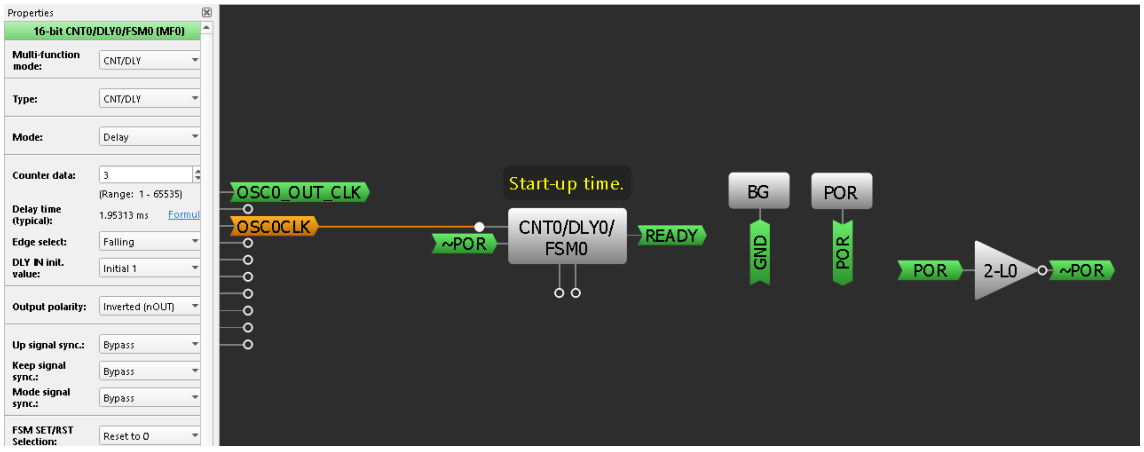

Figure 7. Start-up time delay block. The CNT0/DLY0/FSM0 configuration is shown on the left side

6.4 HVOUT

Figure 8 shows the HVOUT CTRL0 connections and their internal configuration. HVOUT CTRL0 is the block that controls the SLG47105 internal power transistors. This block controls the power transistors connected to the S1 solenoid. At power-up the block is deactivated. It is activated by the inverted POR signal connected in Sleep0 and Sleep1 inputs. The output of Pin 8 is always set to activate the push-pull low side by the same inverted POR signal connected in the input IN1. However, the output transistors are only active when the READY signal connected to the OE1 input is at a high level. The push-pull output of Pin 7 is entirely controlled by the PWM Controller block (its operation will be explained below).

Furthermore, the HVOUT CTRL 0 block supplies the FAULT_A signal to indicate when a fault condition occurs in this power output.

The HVOUT CTRL 1 block is configured in the same way as the HVOUT CTRL 0 block. Its connections behave similarly and have similar purposes. The HVOUT CTRL 1 block is connected to the S2 solenoid through Pins 9 and 10. This block is connected to the PWM Controller 2 block and it supplies the FAULT_B signal for any fault in its operation.

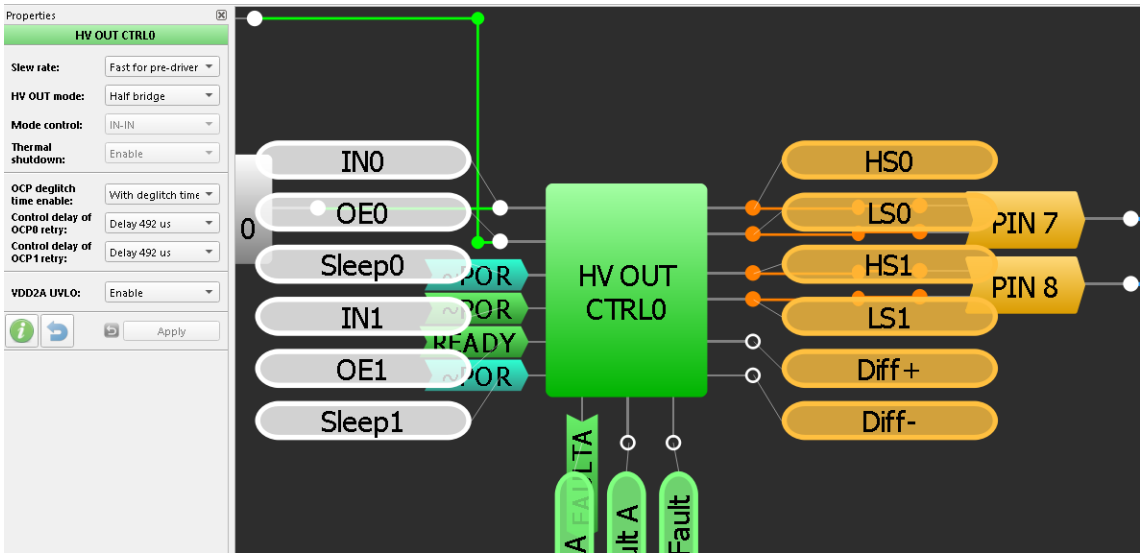

Figure 8. HV OUT CTRL0 block connections and configuration

6.5 PWM Controller and Current Regulation

Figure 9 shows the PWM Controller 1 block inside a yellow box. This block is formed by four components: PWM0, PWM Chopper 0, CNT1/DLY1, and LUT (Look-Up Table) 2-L1 configured as an AND gate. These four components adjust the PWM output for solenoid S1 accordingly to the signal supplied by the current comparator CCMP0. On the left side of Figure 9 is the internal configuration of the PWM0 block. The PWM0 block generates a complementary PWM with dead-band time. The two complementary PWM signals are used in the 2-L1 AND port to enable/disable the HV GPO0 output. HV GPO0 is disabled before it turns on the high-side transistor as a protective measure. The OUT+ output of the PWM0 block is connected to the PWM Chopper 0 to be chopped by the current comparator CCMP0 signal. PWM Chopper 0 has its blanking input connected to CNT1/DLY1. The CNT1/DLY1 will generate a short pulse of 200 nanoseconds to the blanking time input, allowing a minimum PWM on time. The output of PWM Chopper 0 is connected to the IN0 input of the HV OUT CTRL0 block, controlling the push-pull output of HV GPO0. As seen in Figure 9, the PWM0 block supplies a dynamic reference for the current comparator CCMP0. PWM0 is configured to use the Register File Data to set up the maximum PWM and the reference voltage for the current comparator. There are only two values in use, the first one for the peak current, byte 8, and the second one for the hold current, byte 9. The change of configuration will happen when a positive edge raises in the PWM0 input Duty Cycle CLK.

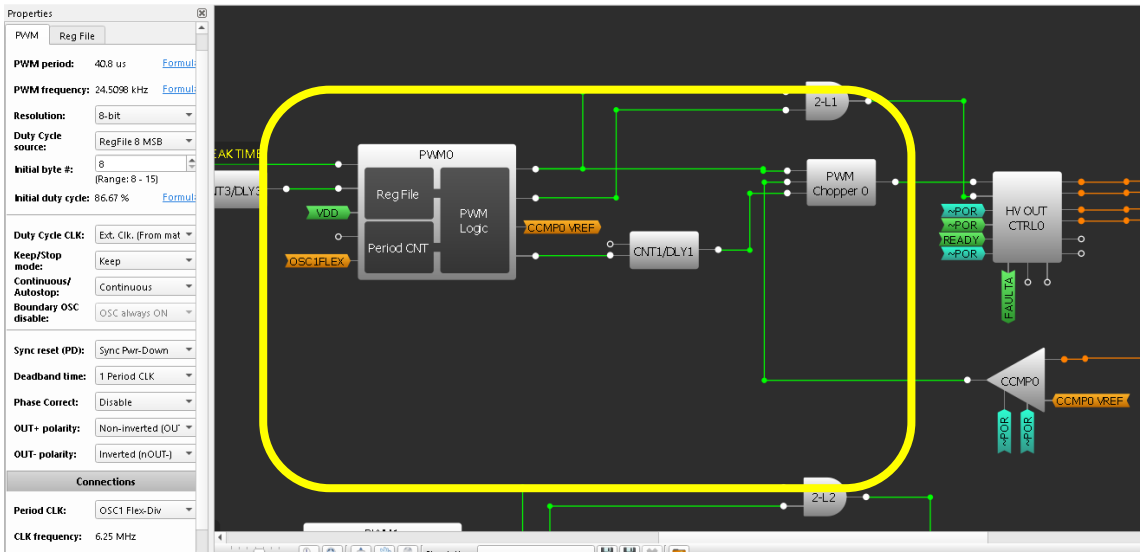

Figure 9. PWM Controller 1 block is inside the yellow box

The components connected to the input of the PWM0 block are shown in Figure 10. The components are an AND gate connected to the PWR DOWN input of PWM0 and CNT3/DLY3 connected to the Duty Cycle CLK input of PWM0. The AND gate operates as an enabler for the S1 On/Off pin signal. The signal from this pin can turn on the PWM0 block just after the start-up delay time when the READY signal is at a high level. The output of the AND port turns on the PWM0 block and is delayed by 50 milliseconds in the IPEAK TIME delay component. The delay of this block controls how long the PWM will regulate the solenoid current at its peak value. After this time, a positive edge is generated for the Duty Cycle CLK input of PWM0, and the reference register byte is increased, changing the PWM value and the reference voltage for the current comparator CCMP0. When SOL1_CMD is at a high level the PWM0 output is turned on and when SOL1_CMD is at a low level the PWM0 output is immediately turned off.

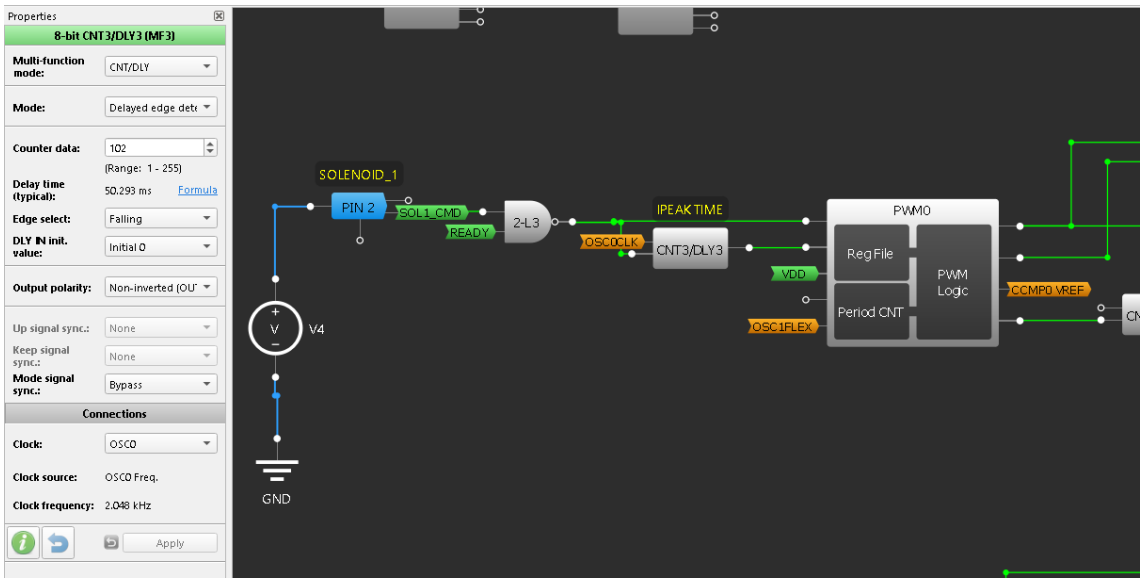

Figure 10. Input connections for the PWM0 component

The current comparator CCMP0 is used to regulate the solenoid current, and the configuration of this component is shown in Figure 11. The current comparator internally amplifies the voltage in Pin 5 by 8 (see IN+ gain in Figure 11). This multiplier factor must be considered when setting the reference voltages for comparison. The component is turned on with the inverted POR signal and it is always on after POR. The IN- input of CCMP0 is connected to the PWM0 CCMP0 VREF output. This output will supply the voltage references of bytes 8 and 9 of the Register File Data. The Register File Data is shown in Figure 12.

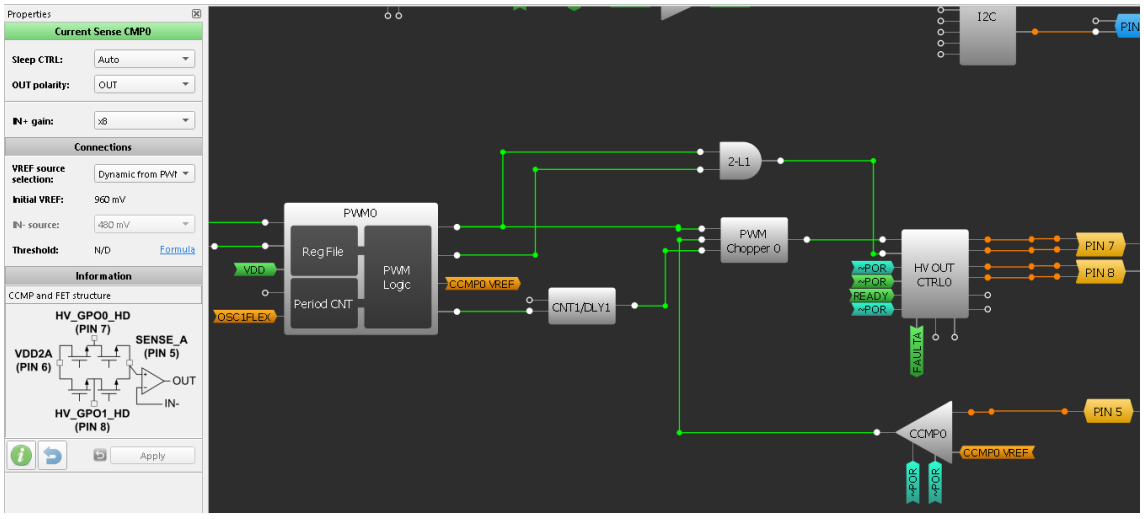

Figure 11. CCMP0 configuration and connection to PWM Chopper 0

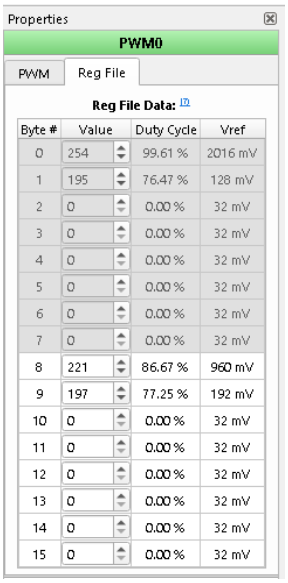

Figure 12. Register Data File configuration

The structure of PWM Controller 2 is like the structure of PWM Controller 1. The register bytes used for current regulation are bytes 0 and 1. The components of PWM Controller 2 are shown in Figure 13. It is important to note that the solenoid current settings are different in PWM Controller 1 and PWM Controller 2. The current regulation is independent, as are the PWM values.

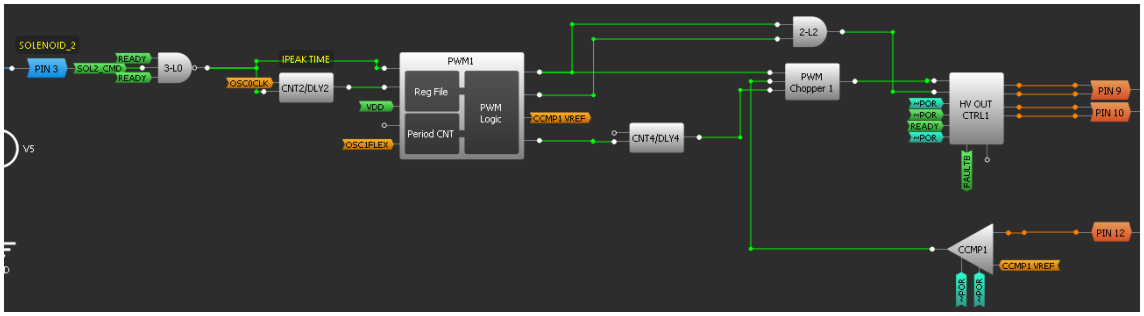

Figure 13. PWM Controller 2 structure and connections

6.6 Solenoid Status Indication and Fault Signal

Figure 14 shows the components used for solenoid status indication and fault output signal. The Pipe Delay component is used to generate the 1Hz square wave signal. Its configuration is shown on the left side of Figure 14. This component divides the OSC0 output clock to generate this square wave signal. The signals FAULT_A and FAULT_B are the fault signals for the respective solenoids S1 and S2. These signals are registered to avoid glitches in the output pins. The respective pins are configured as open drain outputs. The output pins connected to the solenoid status indicators are configured as push-pull outputs.

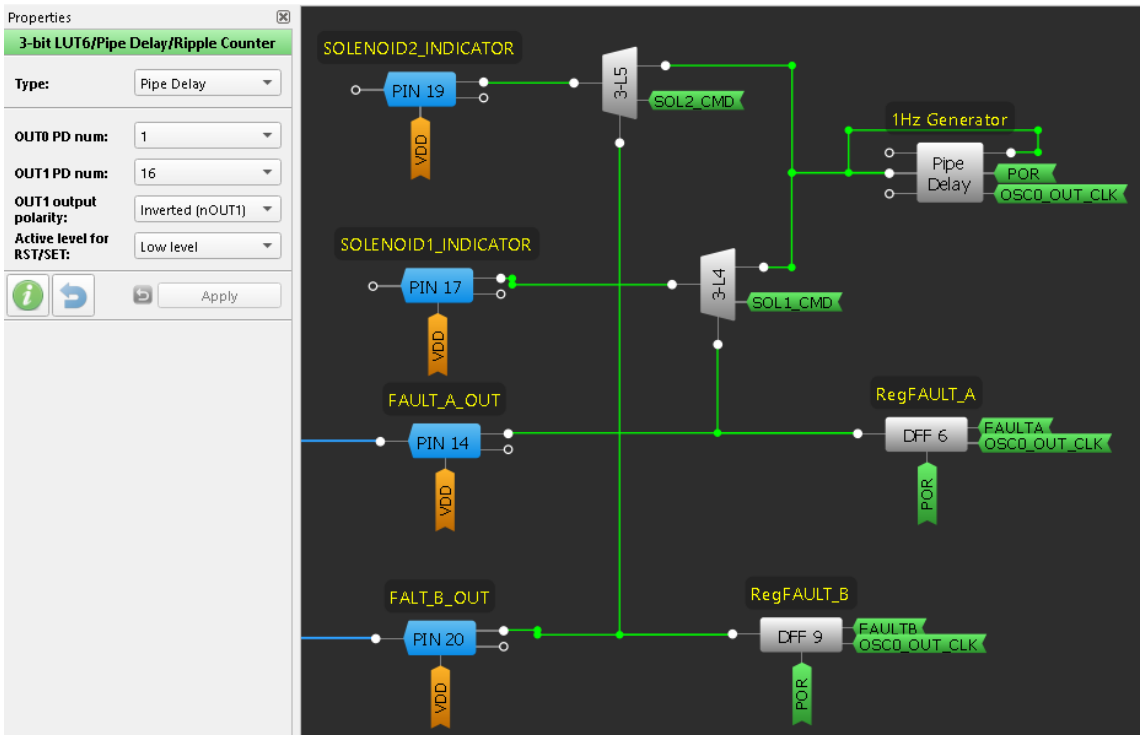

Figure 14. Solenoid status indication and fault output signal

6.7 I2C

The I2C is kept active in the design, allowing users to set PWM values through an external device. There are no internal signals connected to the I2C block, just the respective external pins connected to it.

7. Verification Prototype

Figure 15 shows a picture of the verification prototype built to test this design. The prototype was assembled on a breadboard using the SLG47105 DIP Board.

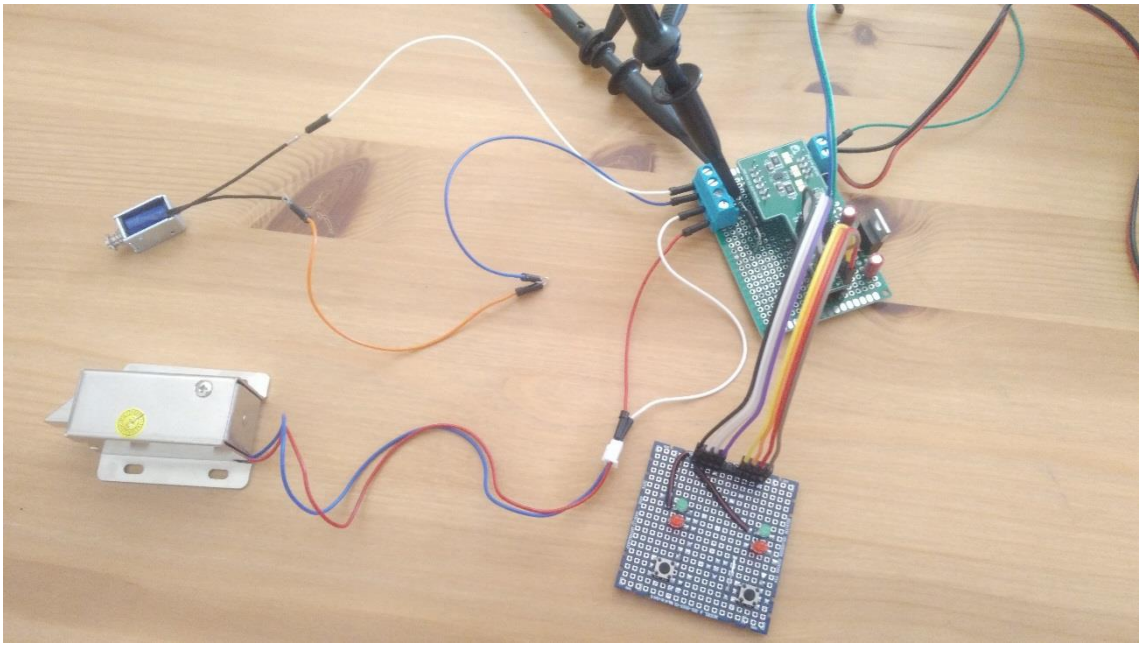

Figure 15. Verification prototype

8. Tests

8.1 Test Procedures

The prototype testing procedure consists of pressing the respective solenoid pushbutton and then verifying the following:

- Plunger movement and position: The solenoid plunger must be pulled-in when it is activated by the driver. The driver must hold the plunger in the pulled-in position while it is active. The driver must release the plunger from its pulled-in position and return it to the de-energized position when the driver is deactivated.
- LED indicators: When the solenoid is deactivated its green LED indicator must be off. When it is activated its green LED indicator must be on. When the respective solenoid output has a fault condition (short circuit) the solenoid green indicator must blink at a frequency of 1Hz. The fault red LED indicator must be on when there is a fault condition and off otherwise.
- Current measurement: the maximum peak and hold currents must be measured and should comply with the designed values (see Table 3 in Section 5).

To measure the current through the solenoids we added a small resistor of 0.1Ω (0.1 percent) in series with each solenoid (see the typical application circuit in Section 4).

The voltage through this resistor is measured using two channels of an oscilloscope. The oscilloscope used is the Hantek 6022BE. The current in Ampères will be:

$$Current\ (A) = 10\ x\ (Sense\ Resistor\ Voltage)(V) \qquad Eq.2$$

8.2 Test Results Solenoid S1

Figure 16 shows the measured current when activating the solenoid S1. The figure shows the initial peak current through the solenoid and, after 50.7 milliseconds, the current reduction to the hold value.

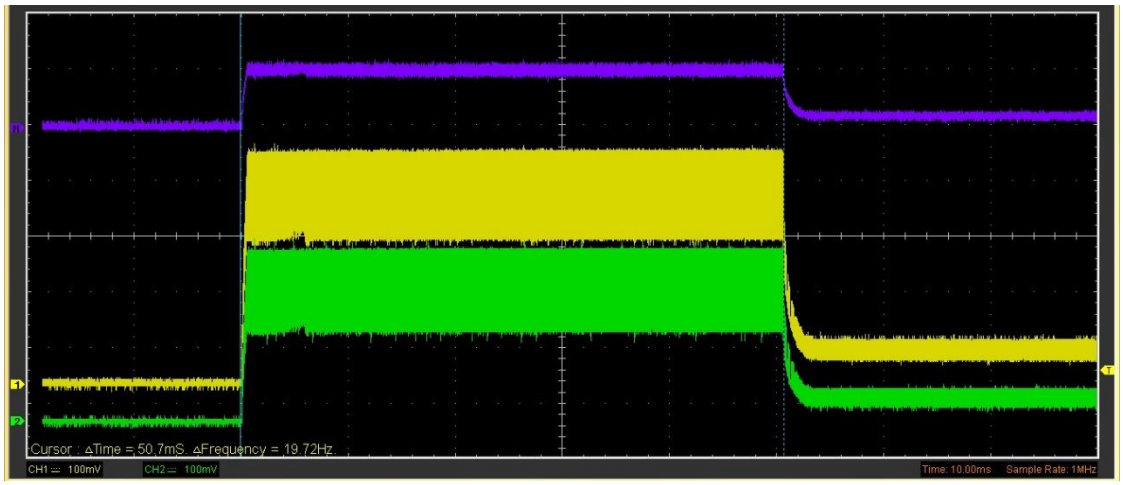

Figure 16. Solenoid S1 current measurement. The current is shown through the math channel M, which is equal to (CH1 – CH2)

Figure 17 shows a close view of the peak current and the measurement of its value. The measured peak current value is 113mV, corresponding to 1.13A.

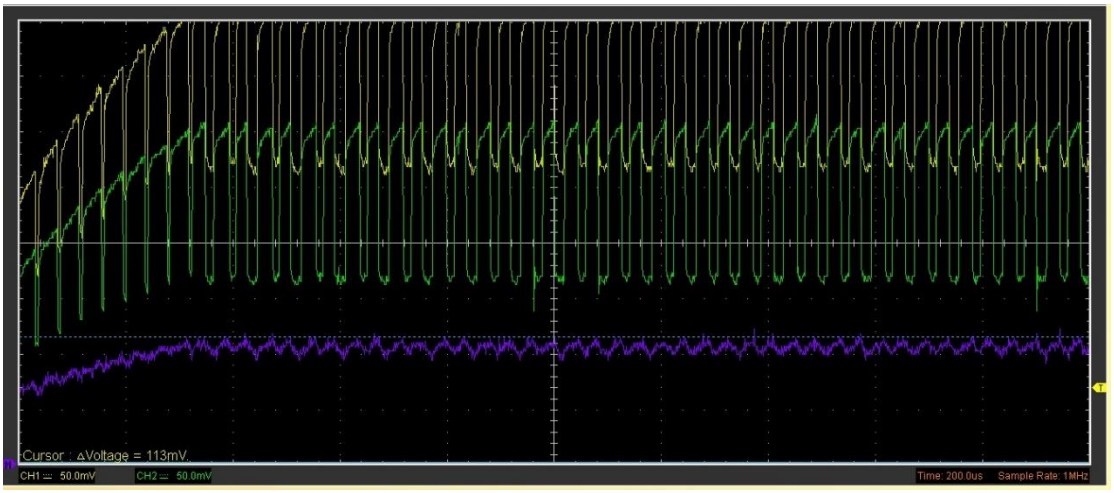

Figure 17. Solenoid S1 close view of peak current measurement. The cursor is positioned over the math channel M, where M = (CH1 – CH2)

Figure 18 shows a close view of the hold current measurement. The measured maximum hold current is 25.5mV, equivalent to 255mA.

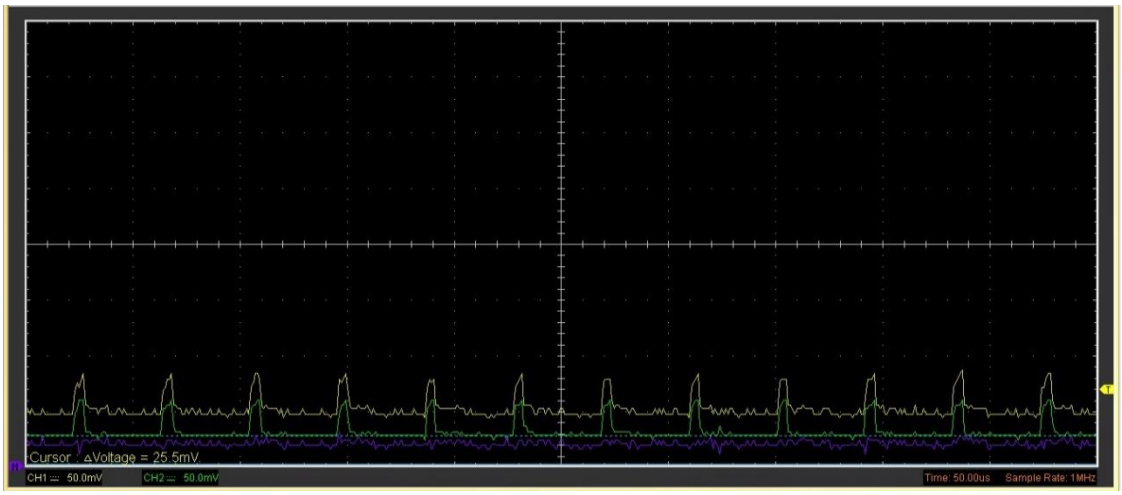

Figure 18. Solenoid S1 close view of hold current measurement. The cursor is positioned over the math channel M, where M = (CH1 – CH2)

Figure 19 shows the PWM generated in Pin 7 (HV_GPO0) during the activation of solenoid S1 (peak current setting). Figure 19 reveals the reduction of the PWM duty cycle over time.

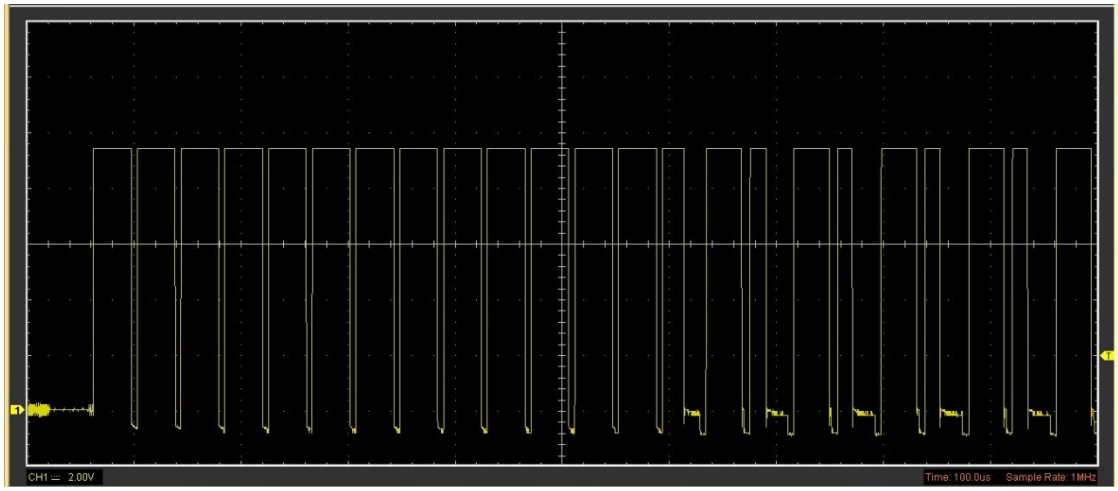

Figure 19. Solenoid S1 peak current PWM applied

Figure 20 shows the PWM applied in the solenoid S1 when it is in hold current regulation. The cursor in the figure shows the high-side transistor on time.

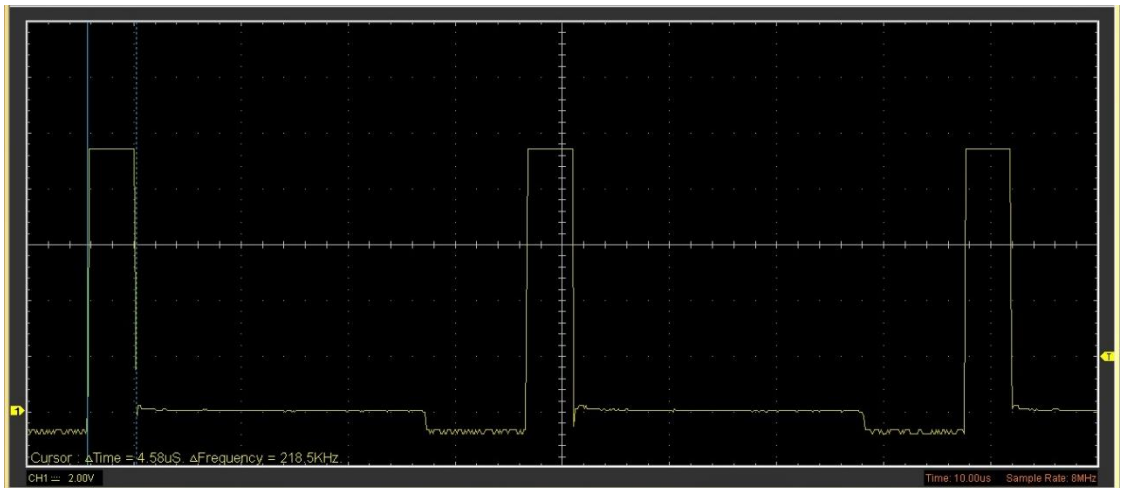

Figure 20. Solenoid S1 PWM generated in hold current regulation

Figure 21 shows the voltage at the sense resistor used by SLG47105 to measure the solenoid current in hold current regulation.

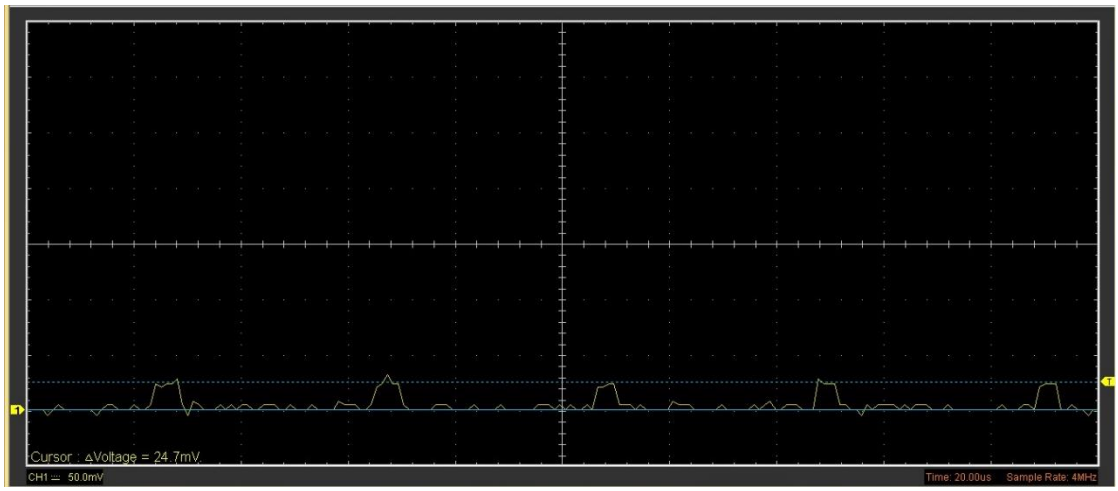

Figure 21. Solenoid S1 voltage in sense resistor with driving solenoid in hold current regulation

Figure 22 shows the PWM applied to the solenoid S1 when it is short-circuited (a fault condition).

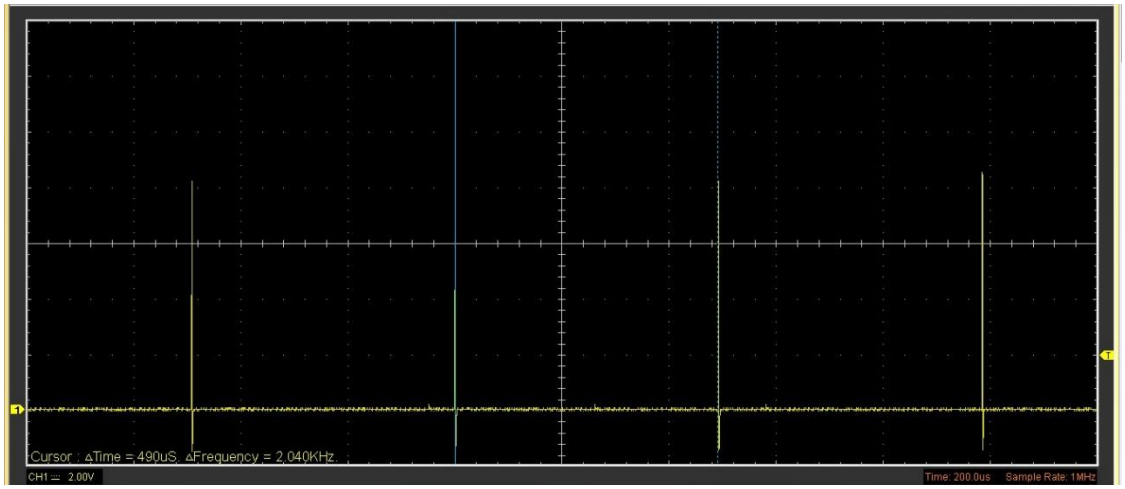

Figure 22. Solenoid S1 driver PWM when the output is short-circuited

8.3 Test Results Solenoid S2

Figure 23 shows the measured current when activating the solenoid S2. The figure shows the initial peak current through the solenoid and, after nearly 50 milliseconds, the current reduction to the hold value. Before the current regulation switch from peak to hold value, there is a visible fall in the measured current. The reason for this valley is the back electromagnetic force (EMF) generated by the moving core of the solenoid (the plunger). When the plunger starts to move, its movement in the magnetic field of the solenoid induces a current in the coil winding against the current that is pulling the core into the solenoid. This effect ends when the plunger arrives at its limit point and stops moving.

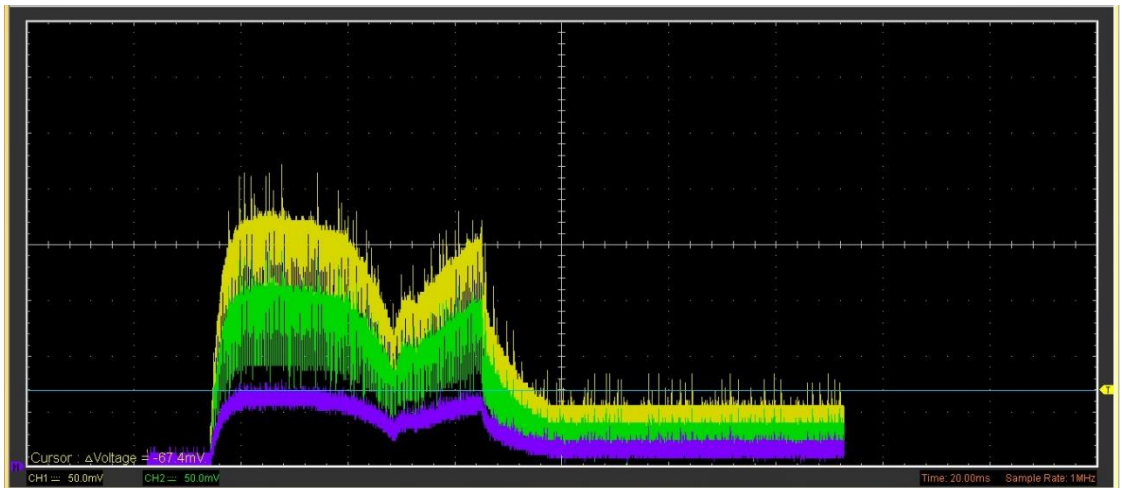

Figure 23. Solenoid S2 overview of the current measurement. The current is shown through the math channel M, which is equal to (CH1 – CH2)

Figure 24 shows a close view of the peak current and the measurement of its value. The measured peak current is 66.5mV, meaning a peak current value of 665mA.

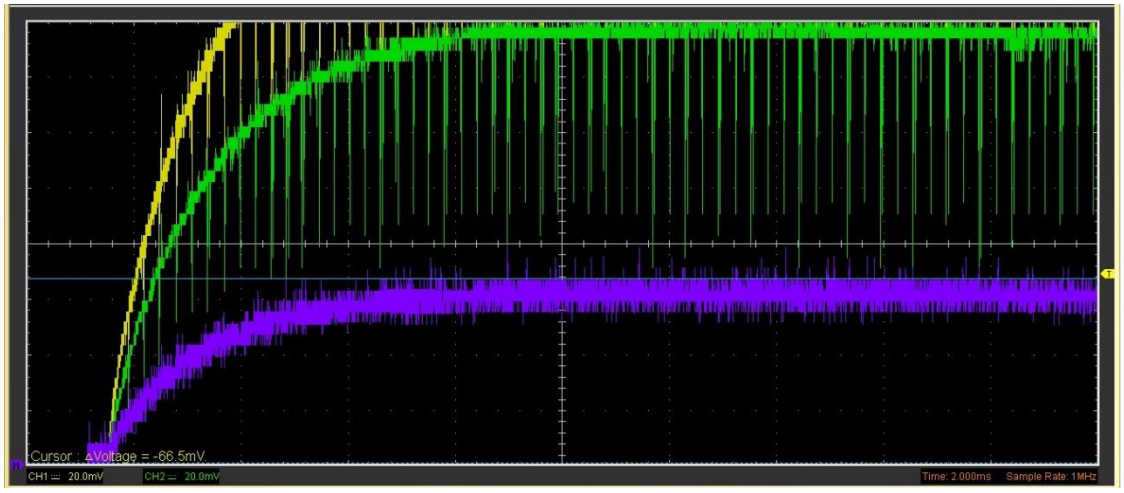

Figure 24. Solenoid S2 close view of peak current measurement. The current is shown through the math channel M, which is equal to (CH1 – CH2)

Figure 25 and Figure 26 show a close view of the hold current and the measurement of its value. Figure 25 shows the cursor value in Channel1 and Figure 26 shows the cursor value in Channel 2. The cursor reading in Channel 1 is 55.4mV and in Channel 2 is 38.7mV. The difference between them is equal to 16.7mV, meaning a current of 167mA in the solenoid.

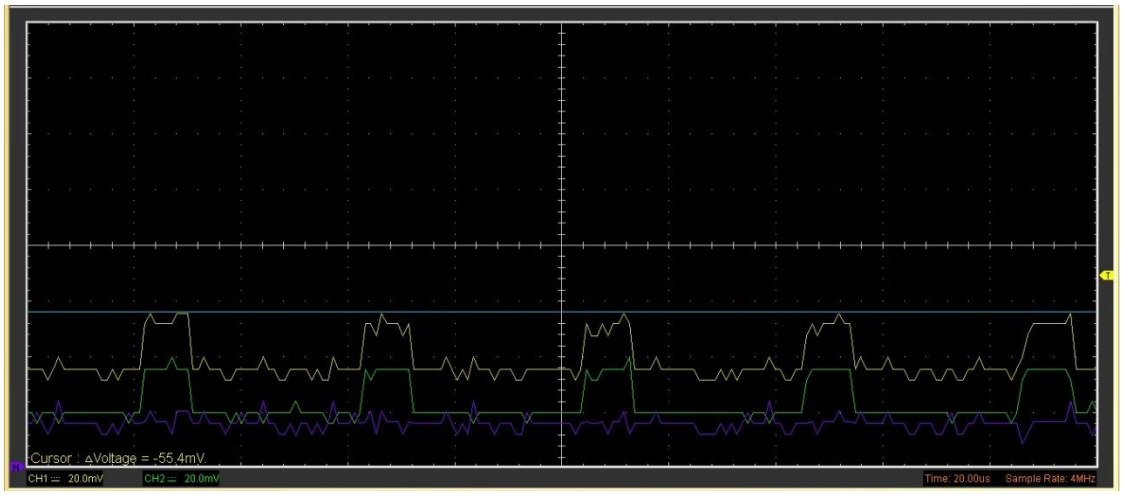

Figure 25. Solenoid S2 close view of hold current. The cursor is positioned at the peak of channel 1

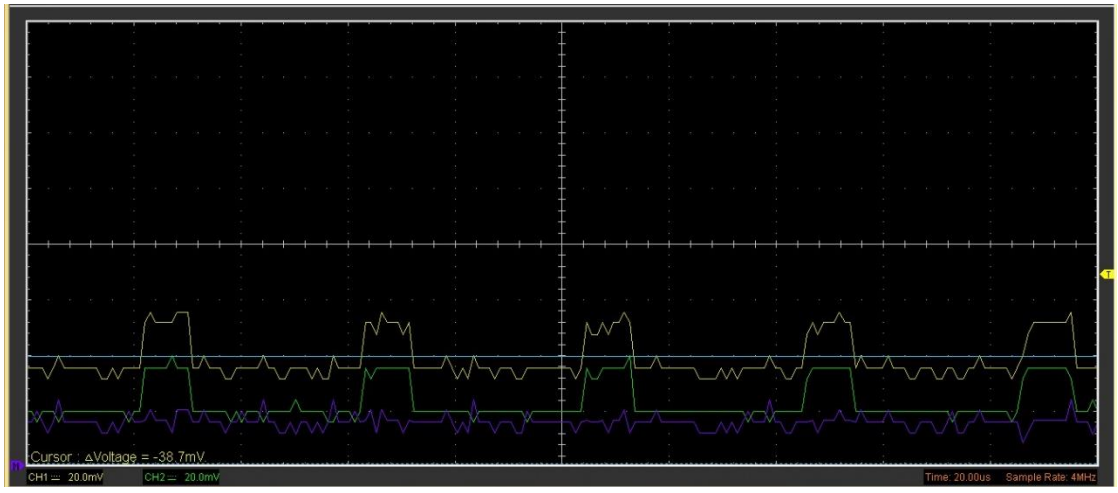

Figure 26. Solenoid S2 close view of hold current. The cursor is positioned at the peak of channel 2

Figure 27 shows the PWM applied in the solenoid S2 when it is in hold current regulation.

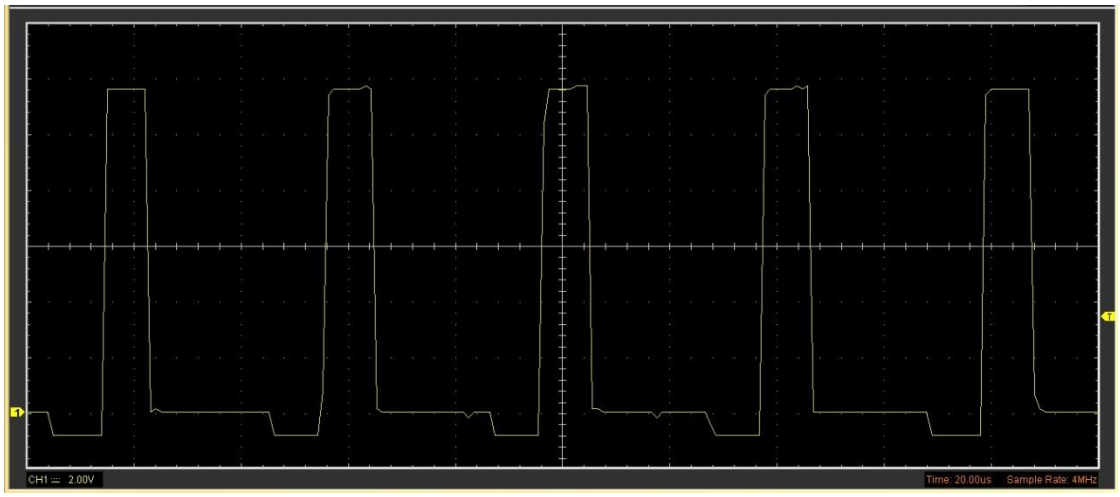

Figure 27. Solenoid S2 view of applied PWM in hold current regulation

Figure 28 shows the voltage at the sense resistor used by SLG47105 to measure the solenoid current in hold current regulation.

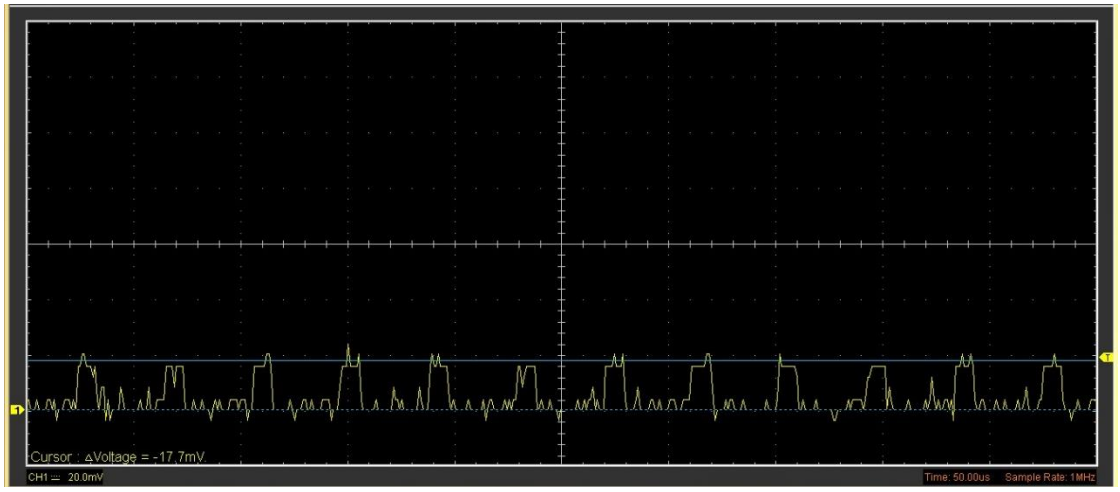

Figure 28. Solenoid S2 voltage in sense resistor with driving solenoid in hold current regulation

8.4 Summary of Current Measurements

Table 4 shows a comparison between the calculated and measured peak and hold currents of each solenoid.

Table 4. Comparison of measured and calculated currents. All current values are in mA.

Sol.	Calculated peak current	Measured peak current	Peak current Error	Peak current Error (%)	Calculated hold current	Measured hold current	Hold current Error	Hold current Error (%)
S1	1090.9	1130	39.1	+3.58%	218.18	255	36.82	+16.9%
S2	650	665	15	+2.31%	145.5	167	21.5	+14.8%

8.5 Summary of Power Measurements

Table 5 shows a comparison between the calculated and measured (considering the measured current and nominal resistance) power of each solenoid.

Table 5. Comparison of measured and calculated power dissipations. All power values are in mW

Sol.	Calculated peak current power	Measured peak current power	Peak current power difference (mW / %)	Calculated hold current power	Measured hold current power	Hold current power difference (mW / %)
S1	5355.4	5746	+381 / 7.11%	214.2	292.6	+78.4 / 36.6%
S2	7799	8163	+364 / 4.67%	390.8	514.8	+124 / 31.7%

Table 6 shows the calculated and measured power savings achieved with the power saving solenoid driver. The nominal power consumption is considered for this calculation.

Table 6. Comparison of calculated and measured power saving

Solenoid	Nominal Power (mW)	Calculated power saving (mW / %)	Measured power saving (mW / %)	Power saving difference (mW / %)
S1	5500	5285.8 / 96.1 %	5207.4 / 94.68%	-78.4 / -1.42%
S2	7800	7409.2 / 94.99%	7285.2 / 93.4 %	-124 / -1.59%

9. Conclusion

This application note showed the implementation of a dual power-saving solenoid driver. It was shown that the driver can achieve huge power savings for the two solenoids, depending on the ratio of hold current to peak current. The higher the ratio, the higher the power saving. However, it is important to say that the ratio depends on the application. Reducing the hold current will reduce the force to maintain the plunger pulled in the solenoid.

It is important to discuss the results shown in the comparison of the calculated and measured currents. The hold current had a significant error, higher than 10 percent, for both solenoids. From the analysis of the absolute and percentual current errors it is possible to say that there are side effects of gain and offset errors. As shown in Table 4, the absolute error increases with the current setpoint, which is a signal of gain error. This gain error can be associated with limitations in the sense resistor accuracy. However, the increase in the percentual error when the current is reduced to the hold value indicates an offset error. This means an almost constant error, and that will be more relevant for lower values. It seems that the offset error is more relevant than the gain error. Unfortunately, is not possible to identify the source of this error. Some of the hypotheses are an error in the SLG47105 current comparator or an error in the current measurement made with the oscilloscope.

10. Revision History

Revision	Date	Description
1.00	Sep 27, 2022	Initial release.

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