RISC-V

A/D Converter (Scan mode)

Introduction

This application note describes how to convert an analog voltage to a digital voltage with the RISC-V A/D converter (scan mode).

It also describes how A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

Target Device

RISC-V

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1. Specifications

1.1 Overview of Specifications

This application note shows an example of the use of the A/D converter in scan mode. The A/D converter is set to scan mode and analog input signal levels of the P400 / ANI2, P401 / ANI3, P006 / ANI4, and P007 / ANI5 pins are converted to digital values. Then the A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

Table 1.1 shows the peripheral function and use. Figure 1.1 shows conversion operation of the A/D converter.

Table 1.1 Peripheral Function and Use

Peripheral Function	Use
A/D converter	Converts analog input signal levels of the P400 / ANI2, P401 / ANI3, P006 / ANI4, and P007 / ANI5 pins.

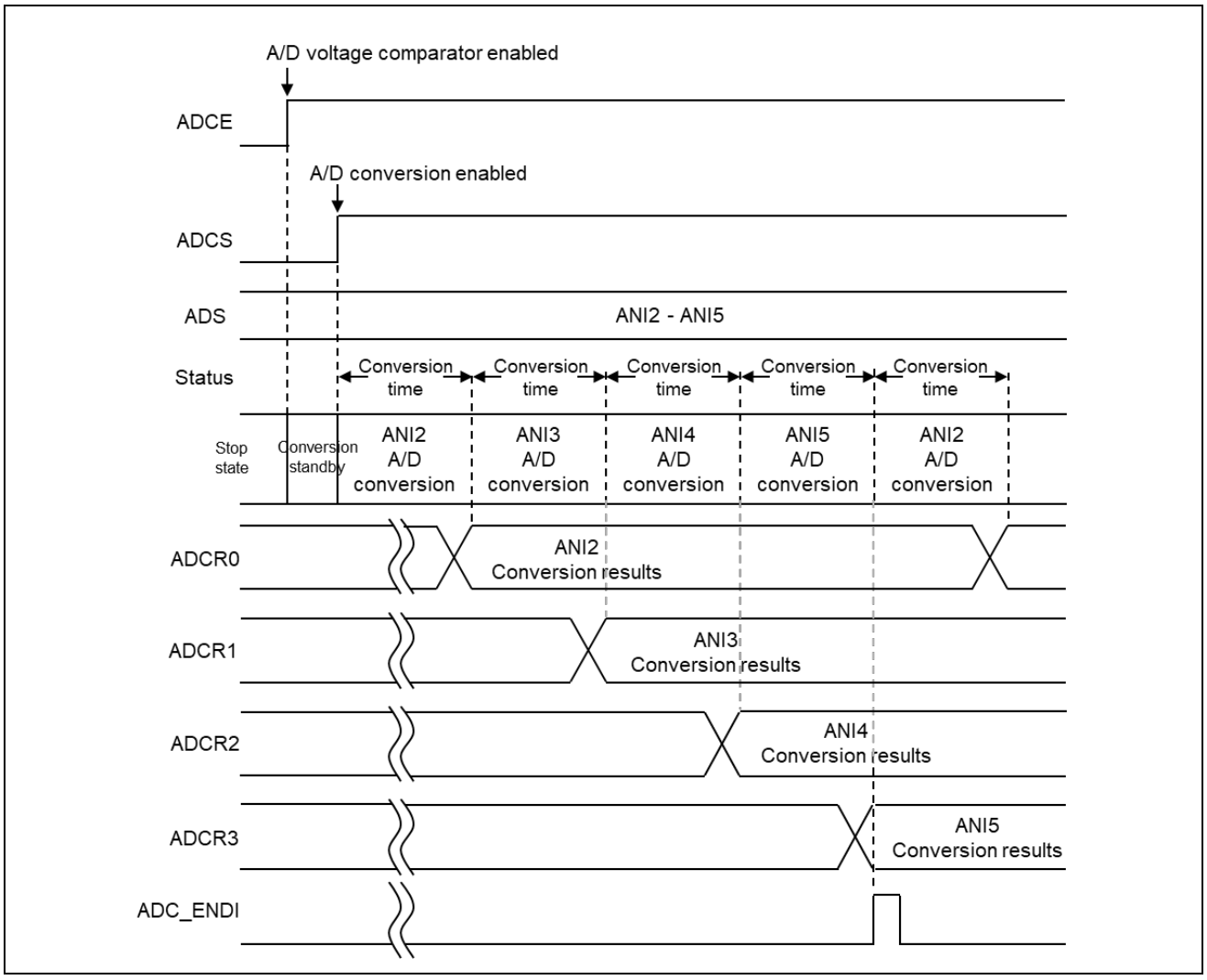

Figure 1.1 Outline of the A/D Converter Conversion Processing

1.2 Outline of Operation

Analog signals that are input to the ANI2, ANI3, ANI4, and ANI5 pins are converted to digital data. In Sleep mode, completion of A/D conversion is waited for. Upon completion of A/D conversion, the A/D conversion results are converted to data and the converted values are stored in the on-chip RAM.

The following describes the main settings.

(1) Initial settings for the A/D converter
Make initial settings as shown in Table 1.2.

Table 1.2 A/D Converter Initial Setting Conditions

Register Name	Setting Value	Content
ADM0	68H	Conversion time setting Conversion time mode: Normal 1 Conversion time: 258/PCLKB (5.375 µs) A/D conversion channel selection mode: Scan mode
ADM1	00H	A/D conversion mode: Sequential conversion mode A/D conversion trigger mode: Software trigger no-wait mode
ADM2	02H	A/D conversion resolution: 12-bit resolution Reference voltage source setting VREF (+): Vcc VREF (-): Vss
ADUL	FFH	Conversion result comparison upper limit: FFH
ADLL	00H	Conversion result comparison lower limit: 00H
ADS	02H	Analog input channel: ANI2, ANI3, ANI4, ANI5
-	-	Use the A/D conversion end interrupt request signal (ADC_ENDI).

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RISC-V (R9A02G021)
Board used	RISC-V-48p Fast Prototyping Board (RTK9FPG021S000W0BJ)
Operating frequency	・ High-speed on-chip oscillator clock : 48 MHz ・ CPU/peripheral hardware clock: 48 MHz
Operating voltage	3.3 V (can be operated at 1.6 V to 5.5 V) LVD0 operations ：reset mode At rising edge TYP. 1.95 V (1.83 V to 2.07 V) At falling edge TYP. 1.90 V (1.78 V to 2.02 V)
Integrated development environment (e^2studio)	e^2studio V2024-01.1 (24.1.1) from Renesas Electronics Corp.
C compiler (e^2studio)	LLVM for RISC-V 17.0.2.202401
Smart configurator (SC)	Smart Configurator for RISC-V V24.1.1.v20240125-1623
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3.1 shows an example of the hardware configuration used in the application note.

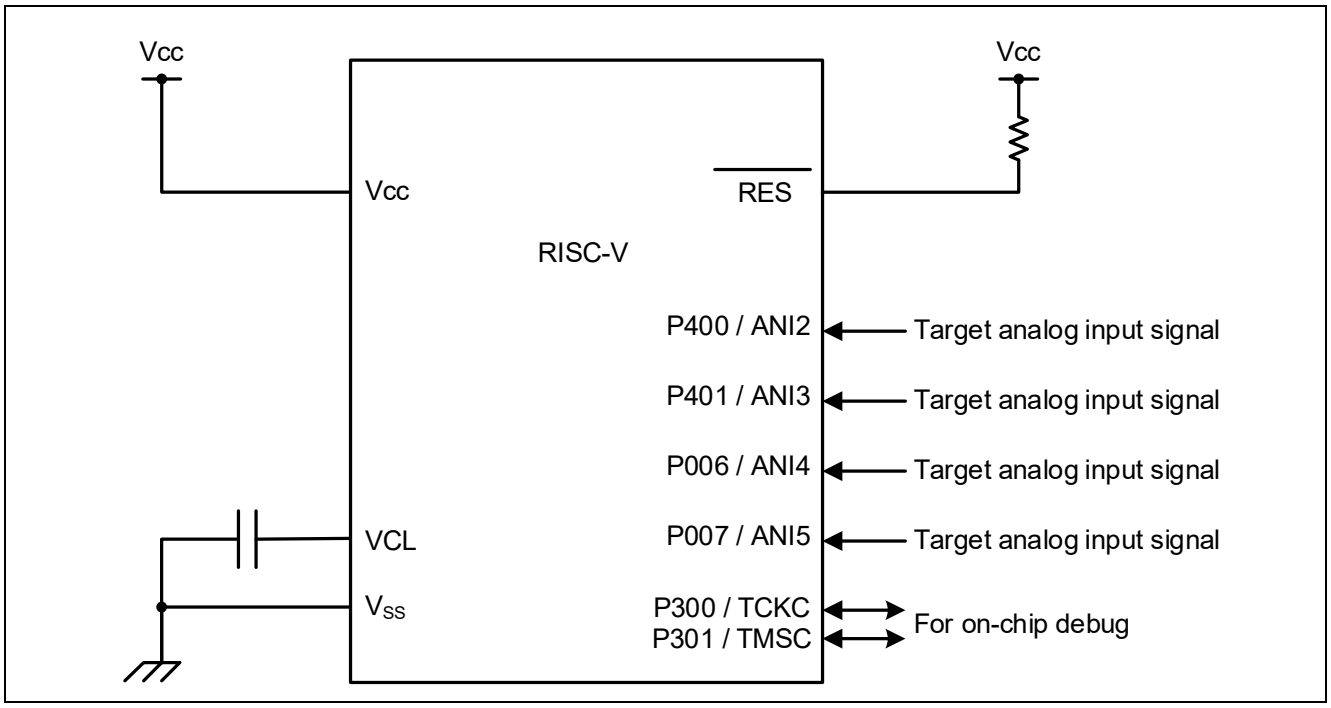

Figure 3.1 Hardware Configuration

Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to Vcc or Vss through a resistor).

Note 2. Vcc must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3.1 lists the pins to be used and their functions.

Table 3.1 Pins to be Used and Their Functions

Pin name	I/O	Function
P400 / ANI2	Input	A/D converter analog input port
P401 / ANI3	Input	A/D converter analog input port
P006 / ANI4	Input	A/D converter analog input port
P007 / ANI5	Input	A/D converter analog input port

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4.1 shows the option byte settings.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
0000_0400H	FFFF_FFFFH	Disables the watchdog timer. (Counting stopped after reset)
0000_0404H	FFFF_CFDBH	LVD0 detection voltage: reset mode At rising edge TYP. 1.95 V (1.83 V to 2.07 V) At falling edge TYP. 1.90 V (1.78 V to 2.02 V)
		High-speed on-chip oscillator clock : 48 MHz
0101_0008H	FFFF_FFFFH	Enables on-chip debugging

4.2 List of Variables

Table 4.2 lists global variables.

Table 4.2 Global Variables

Type	Variable Name	Description	Function Used
uint16_t	g_result_buffer[4]	A/D conversion result storage area	main()

4.3 Flowchart

4.3.1 Main Processing Function

Figure 4.1 shows the flowchart of the main processing.

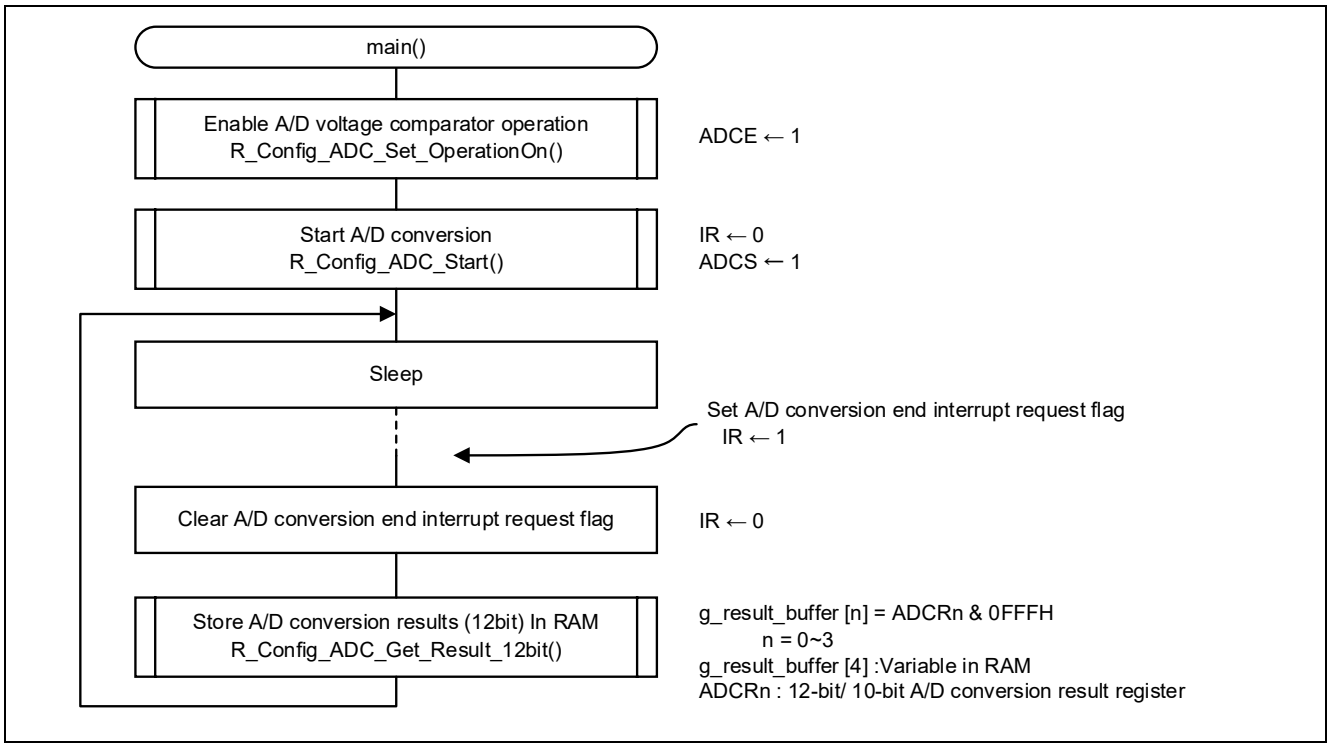

Figure 4.1 Main Processing Function

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RISC-V User's Manual: Hardware (R01UH1036EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.24	—	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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