HS-201HSRH, HS-201HSEH

Radiation Hardened High Speed, Quad SPST, BiCMOS Analog Switch

FN4874
Rev 4.00
February 21, 2017

The HS-201HSRH and HS-201HSEH are monolithic BiCMOS analog switches featuring power-off high input impedance, very fast switching speeds and low ON-resistance. Fabrication on our DI RSG process ensures SEL immunity and only very slight low dose rate sensitivity (ELDRS). These Class V/Q devices are tested and guaranteed for 300krad(Si) total dose performance.

Power-off high input impedance enables the use of this device in redundant circuits without causing data bus signal degradation. ESD protection, overvoltage protection, fast switching times, low ON-resistance, and guaranteed radiation hardness make the HS-201HSRH ideal for any space application that requires improved switching performance.

Related Literature

- For a full list of related documents, visit our website
  - HS-201HSRH product page
  - HS-201HSEH product page

Features

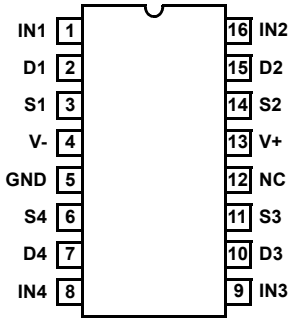
- Electrically screened to DLA SMD# 5962-99618
- QML qualified per MIL-PRF-38535
- Radiation performance
  - High dose rate (50-300rad(Si)/s) . . . . . 300krad(Si)
  - Low dose rate (0.01rad(SI)/s) . . . . . 50krad(Si)
  - SEL immune . . . . . DI RSG process
- Overvoltage protection (power on, switch off) . . . . . ±30V
- Power off high impedance . . . . . ±17V
- Fast switching times
  - t_{ON} . . . . . 110ns (max)
  - t_{OFF} . . . . . 80ns (max)
- Low “ON” resistance . . . . . 50Ω (max)
- Pin compatible with industry standard 201 types
- Operating supply range . . . . . ±10V to ±15V
- Wide analog voltage range (±15V supplies) . . . . . ±15V
- TTL compatible

Applications

- High speed multiplexing
- Sample and hold circuits
- Digital filters
- Operational amplifier gain switching networks
- Integrator reset circuits

Pin Configuration

HS1-201HSRH, HS1-201HSEH SBDIP (CDIP2-T16)
HS9-201HSRH, HS9-201HSEH FLATPACK (CDFP4-F16)
TOP VIEW



Ordering Information

ORDERING SMD NUMBER (Note 2)	INTERNAL MKT. NUMBER (Note 1)	TEMP. RANGE (°C)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
5962F9961801VEC	HS1-201HSRH-Q	-55 to +125	16 Ld SBDIP	D16.3
5962F9961802VEC	HS1-201HSEH-Q	-55 to +125	16 Ld SBDIP	D16.3
5962F9961801QEC	HS1-201HSRH-8	-55 to +125	16 Ld SBDIP	D16.3
5962F9961801VXC	HS9-201HSRH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9961802VXC	HS9-201HSEH-Q	-55 to +125	16 Ld Flatpack	K16.A
5962F9961801QXC	HS9-201HSRH-8	-55 to +125	16 Ld Flatpack	K16.A
5962F9961801V9A	HS0-201HSRH-Q	-55 to +125	Die	
5962F9961802V9A	HS0-201HSEH-Q	-55 to +125	Die	
N/A	HS1-201HSRH/PROTO (Note 3)	-55 to +125	16 Ld SBDIP	D16.3
N/A	HS9-201HSRH/PROTO (Note 3)	-55 to +125	16 Ld Flatpack	K16.A
N/A	HS0-201HSRH/SAMPLE (Note 3)	-55 to +125	Die	

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The listed SMD numbers must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions over-temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening over-temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because there is no Radiation Assurance testing and they are not DLA qualified devices.

Die Characteristics

Die Dimensions

4950µm x 2970µm (195 mils x 117 mils)
Thickness: 483µm ±25.4µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Phosphorus Silicon Glass (PSG)
Thickness: 8.0kÅ ±1.0kÅ

METALLIZATION

Type: AlSiCu
Thickness: 16.0kÅ ±2kÅ

SUBSTRATE

Rad Hard Silicon Gate, Dielectric Isolation

BACKSIDE FINISH

Silicon

Assembly Related Information

SUBSTRATE POTENTIAL

Unbiased (DI)

Additional Information

WORST CASE CURRENT DENSITY

$<2.0 \times 10^5 A/cm^2$

TRANSISTOR COUNT

328

Metallization Mask Layout

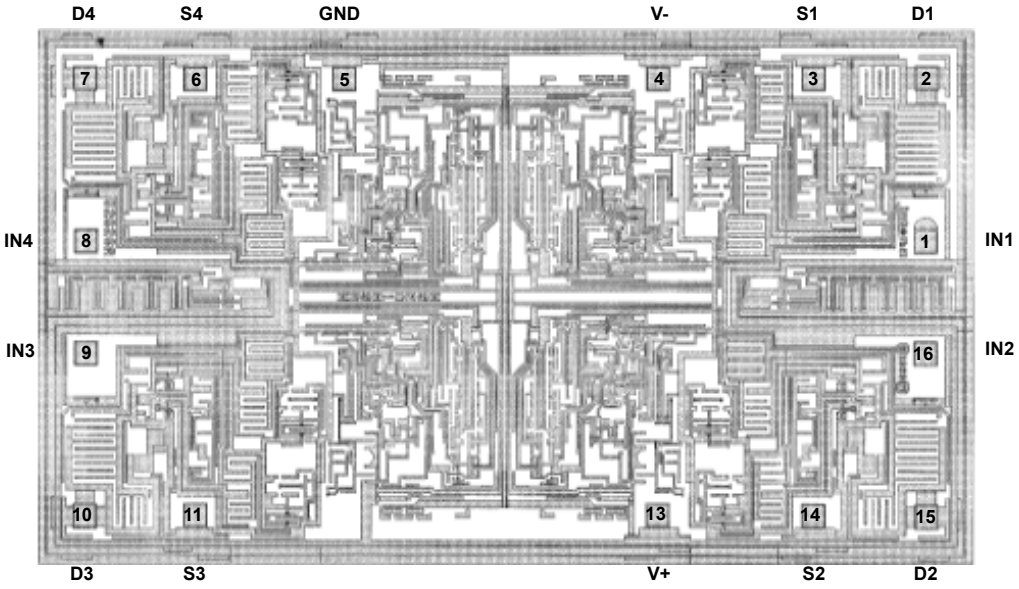


FIGURE 1. HS-201HSRH AND HS-201HSEH MASK LAYOUT

TABLE 1. LAYOUT X-Y COORDINATES

PAD NUMBER	PAD NAME	X (µm)	Y (µm)
01	IN1	365.5	1080.5
02	D1	364.5	277
03	S1	935	280
04	V-	1733	280
05	GND	3345	280
06	S4	4097	280
07	D4	4667.5	277
08	IN4	4666.5	1080.5
09	IN3	4666.5	1632.5
10	D3	4667.5	2436
11	S3	4097	2433
12	No Pad	-	-
13	V+	1733	2433
14	S2	935	2433
15	D2	364.5	2436
16	IN2	365.5	1632.5

NOTES:

1. Origin of coordinates is the upper right hand corner of the die.
2. Pad numbers are increased counter clockwise around the die.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
February 21, 2017	FN4874.4	Changed die dimension from 2790µm x 4950µm (110 mils x 195 mils) to 4950µm x 2970µm (195mils x 117 mils). Added Table 1 “LAYOUT X-Y COORDINATES”. Changed pin names to match the pin names in the SMD data sheet. Added Revision History and About Intersil sections.

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing, and high-end consumer markets.

For the most updated datasheet, application notes, related documentation, and related parts, see the respective product information page found at www.intersil.com.

For a listing of definitions and abbreviations of common terms used in our documents, visit: www.intersil.com/glossary.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

Reliability reports are also available from our website at www.intersil.com/support.

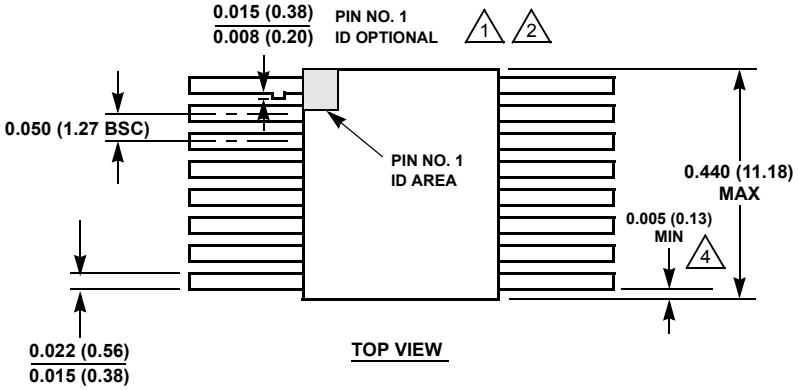
Package Outline Drawing

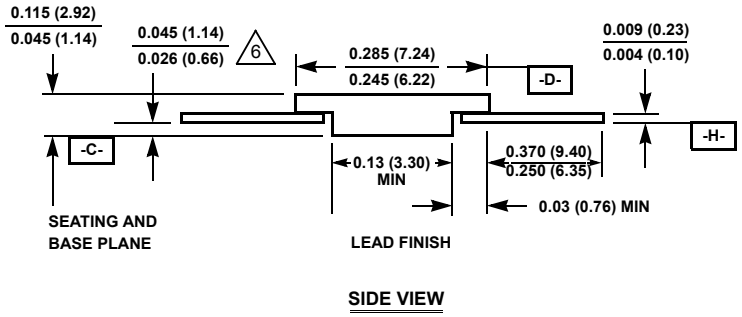
For the most recent package outline drawing, see K16.A.

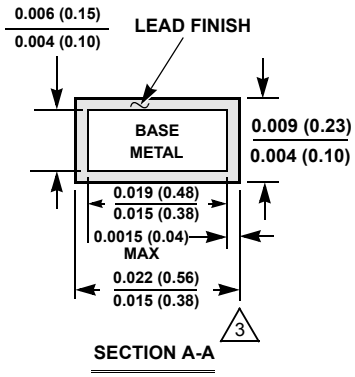
K16.A

16 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 2, 1/10



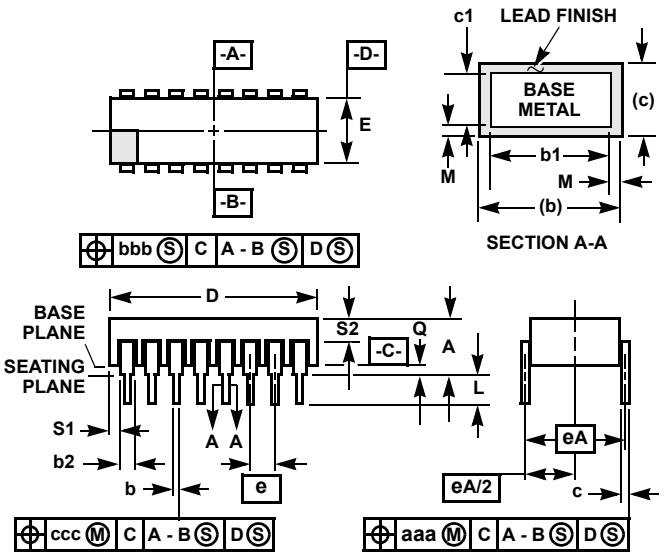




NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

D16.3 MIL-STD-1835 CDIP2-T16 (D-2, CONFIGURATION C)
16 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
a	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	16		16		8

Rev. 0 4/94

For the most recent package outline drawing, see D16.3.