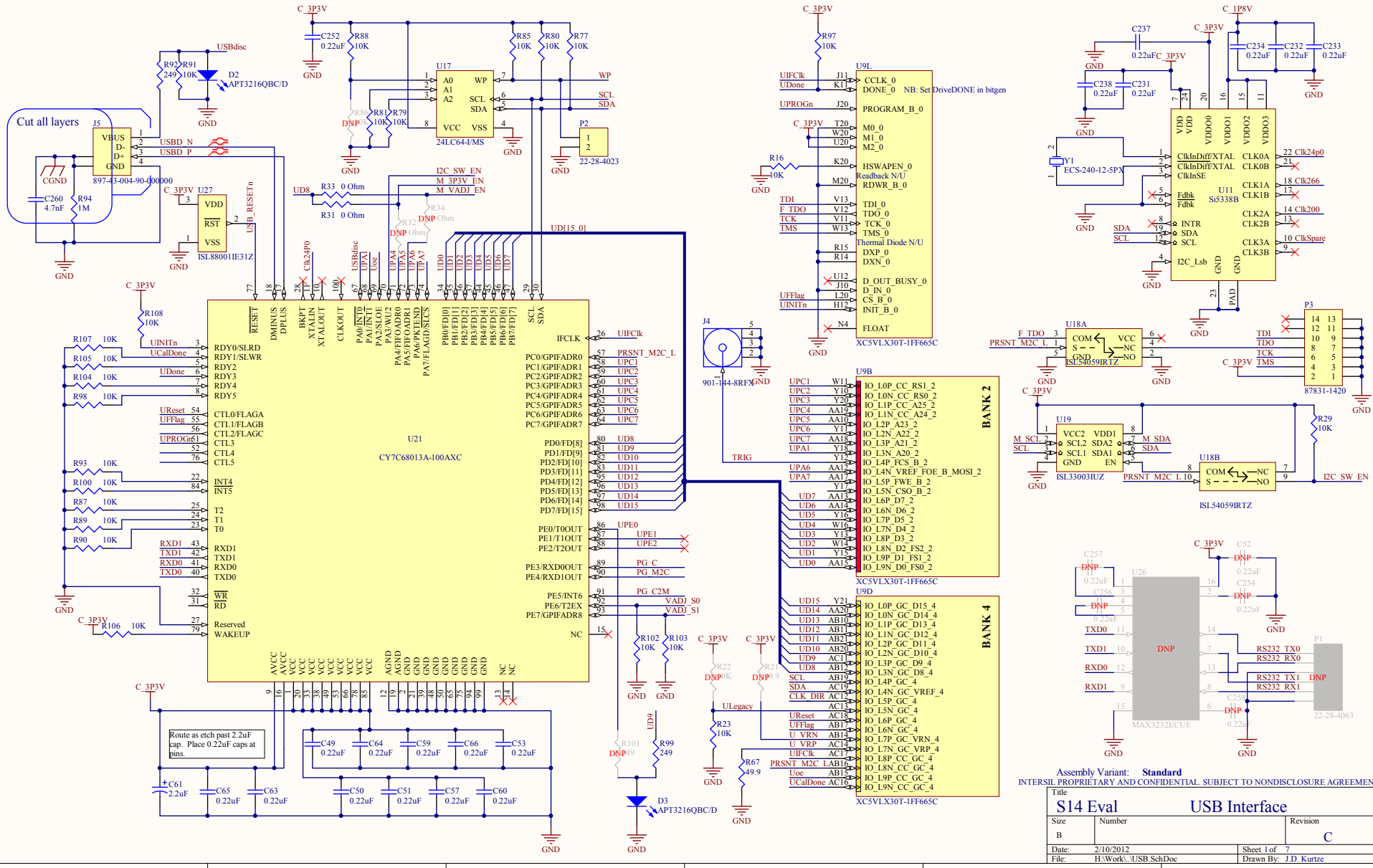
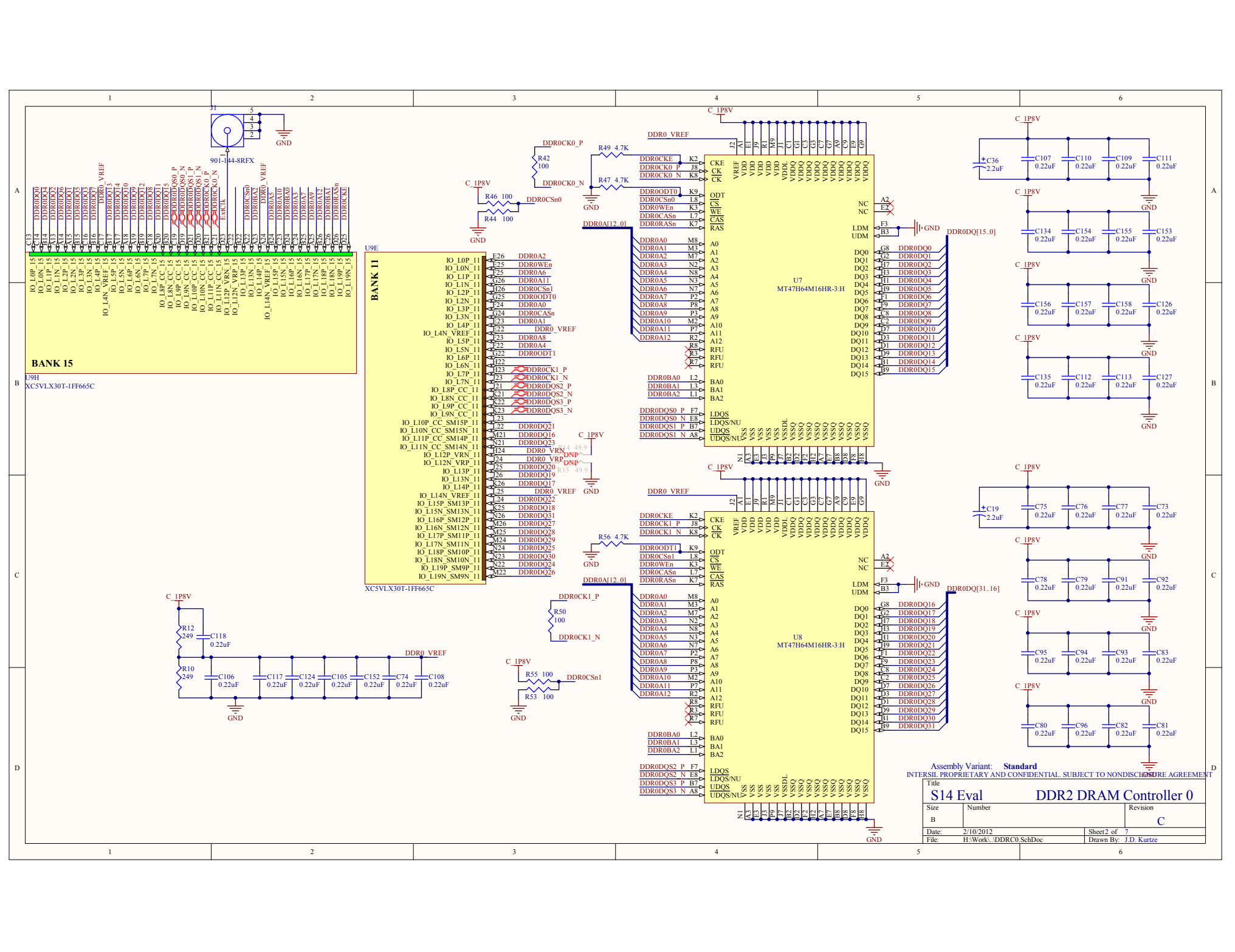
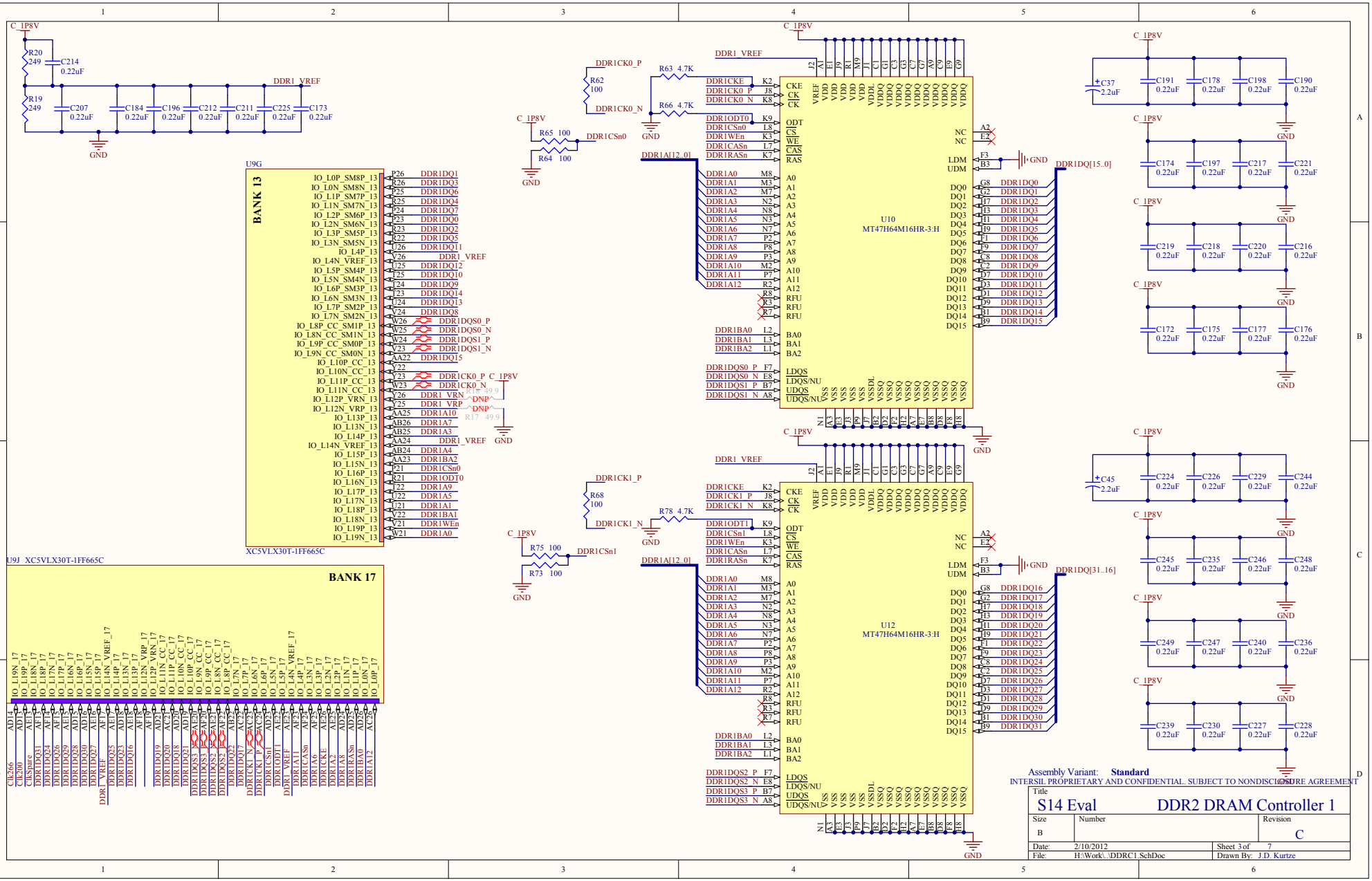
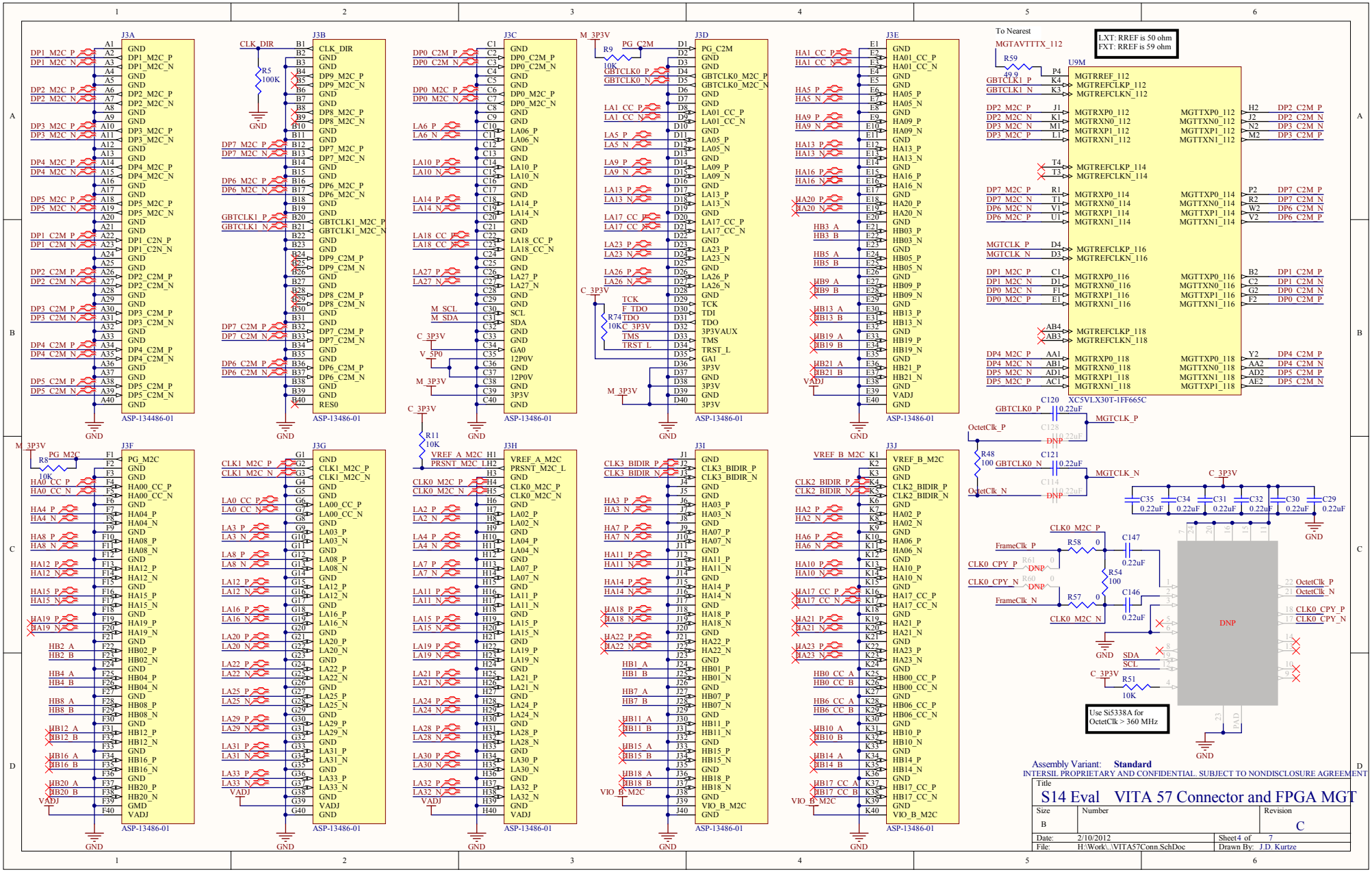
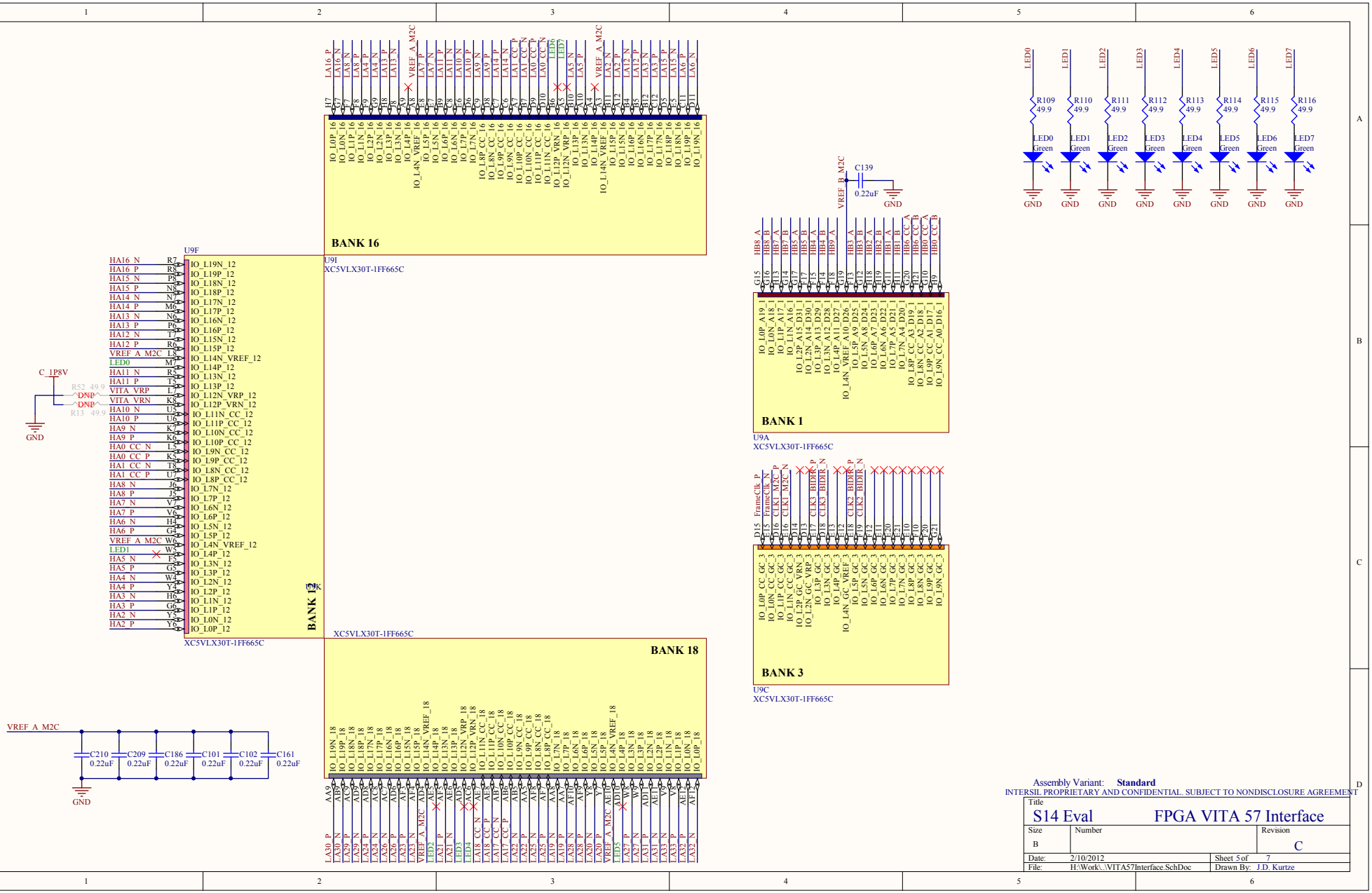
Preprogrammed U11 available as Si5338B-A01482-GM

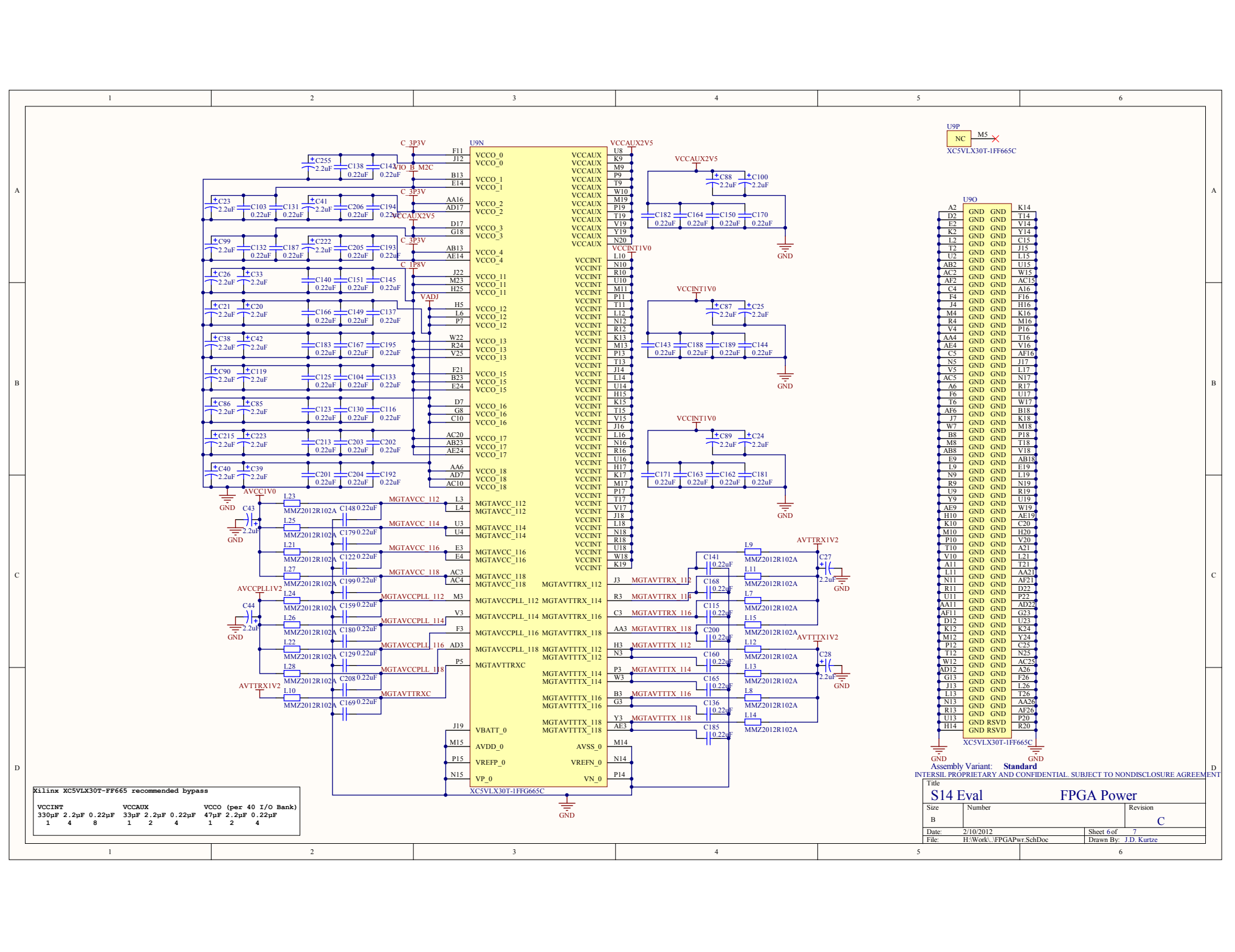


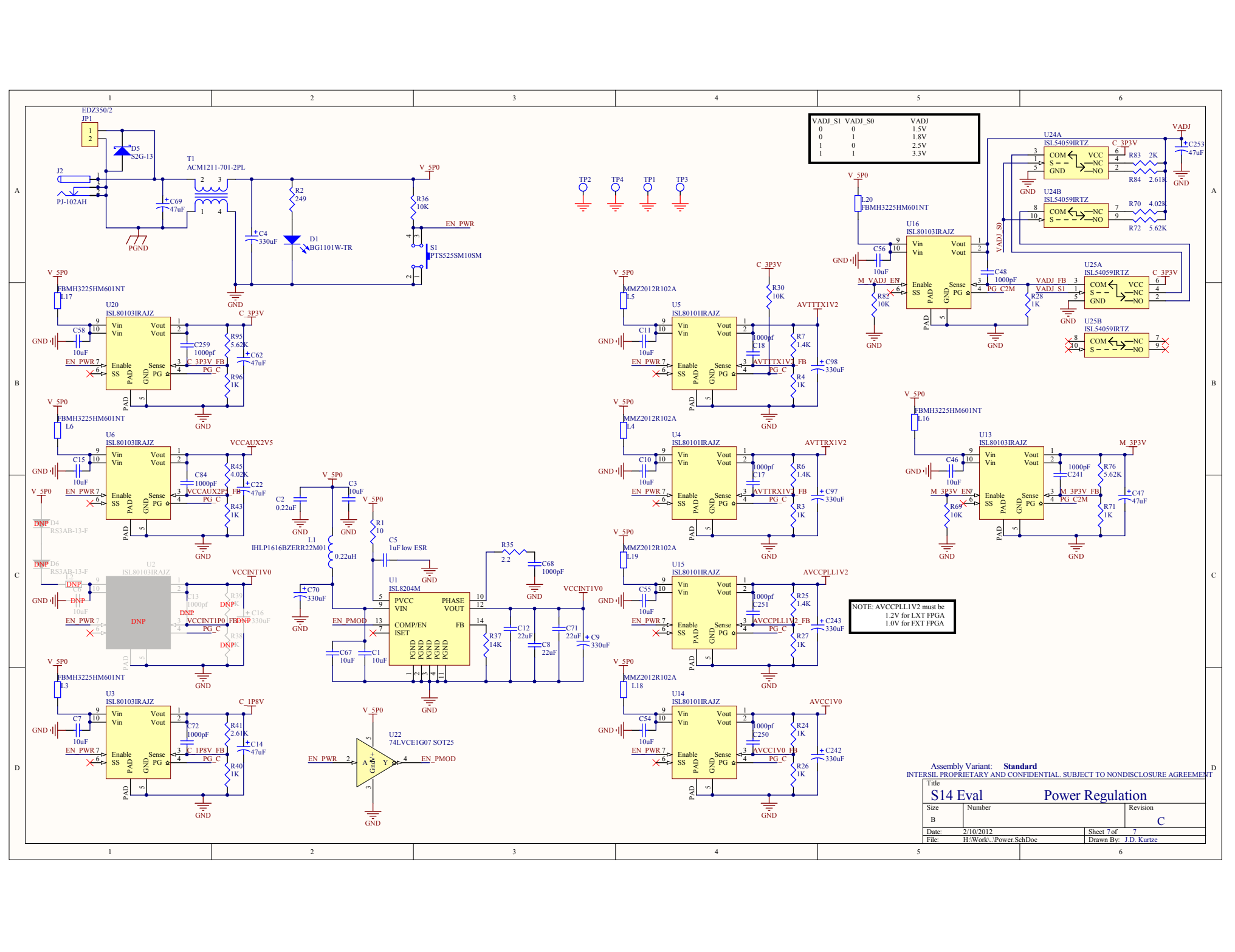

J1
901-144-8RFX
GND
BANK 15
U9H
XC5VLX30T-1FF665C
U9E
BANK 11
XC5VLX30T-1FF665C
U7
MT47H64M16HR-3:H
U8
MT47H64M16HR-3:H
C_1P8V
DDR0_VREF
DDR0CK0_P
DDR0CK0_N
DDR0CSn0
DDR0CSn1
DDR0CK1_P
DDR0CK1_N
DDR0A[12..0]
DDR0DQ[15..0]
DDR0DQ[31..16]
R42 100
R44 100
R46 100
R47 4.7K
R49 4.7K
R50 100
R53 100
R55 100
R56 4.7K
R10 249
R12 249
C106 0.22uF
C108 0.22uF
C118 0.22uF
C36 2.2uF
C19 2.2uF
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
S14 Eval
DDR2 DRAM Controller 0
Size B
Number
Revision C
Date: 2/10/2012
Sheet2 of 7
File: H:\Work\..\DDRC0.SchDoc
Drawn By: J.D. Kurtze


C_1P8V
R20 249
C214 0.22uF
R19 249
C207 0.22uF
C184 0.22uF
C196 0.22uF
C212 0.22uF
C211 0.22uF
C225 0.22uF
C173 0.22uF
DDR1_VREF
GND
U9G
BANK 13
XC5VLX30T-1FF665C
U9J XC5VLX30T-1FF665C
BANK 17
DDR1CK0_P
DDR1CK0_N
R62 100
R63 4.7K
R66 4.7K
R65 100
R64 100
DDR1CSn0
DDR1A[12..0]
DDR1DQ[15..0]
U10
MT47H64M16HR-3:H
DDR1CK1_P
DDR1CK1_N
R68 100
R78 4.7K
R75 100
R73 100
DDR1CSn1
DDR1DQ[31..16]
U12
MT47H64M16HR-3:H
C37 2.2uF
C45 2.2uF
C191 0.22uF
C178 0.22uF
C198 0.22uF
C190 0.22uF
C174 0.22uF
C197 0.22uF
C217 0.22uF
C221 0.22uF
C219 0.22uF
C218 0.22uF
C220 0.22uF
C216 0.22uF
C172 0.22uF
C175 0.22uF
C177 0.22uF
C176 0.22uF
C224 0.22uF
C226 0.22uF
C229 0.22uF
C244 0.22uF
C245 0.22uF
C235 0.22uF
C246 0.22uF
C248 0.22uF
C249 0.22uF
C247 0.22uF
C240 0.22uF
C236 0.22uF
C239 0.22uF
C230 0.22uF
C227 0.22uF
C228 0.22uF
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
S14 Eval
DDR2 DRAM Controller 1
Size B
Number
Revision C
Date: 2/10/2012
Sheet 3 of 7
File: H:\Work\..\DDRC1.SchDoc
Drawn By: J.D. Kurtze


J3A
J3B
J3C
J3D
J3E
J3F
J3G
J3H
J3I
J3J
ASP-134486-01
ASP-13486-01
GND
U9M
XC5VLX30T-1FF665C
MGTAVTTTX_112
LXT: RREF is 50 ohm
FXT: RREF is 59 ohm
Use Si5338A for OctetClk > 360 MHz
DNP
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
S14 Eval VITA 57 Connector and FPGA MGT
Size B
Number
Revision C
Date: 2/10/2012
Sheet 4 of 7
File: H:\Work\..\VITA57Conn.SchDoc
Drawn By: J.D. Kurtze


BANK 16
BANK 17
BANK 18
BANK 1
BANK 3
U9F
U9I
U9A
U9C
XC5VLX30T-1FF665C
C_1P8V
R52 49.9
R13 49.9
DNP
GND
VREF_A_M2C
C210 0.22uF
C209 0.22uF
C186 0.22uF
C101 0.22uF
C102 0.22uF
C161 0.22uF
VREF_B_M2C
C139 0.22uF
LED0 R109 49.9 LED0 Green
LED1 R110 49.9 LED1 Green
LED2 R111 49.9 LED2 Green
LED3 R112 49.9 LED3 Green
LED4 R113 49.9 LED4 Green
LED5 R114 49.9 LED5 Green
LED6 R115 49.9 LED6 Green
LED7 R116 49.9 LED7 Green
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
S14 Eval FPGA VITA 57 Interface
Size B
Number
Revision C
Date: 2/10/2012
Sheet 5 of 7
File: H:\Work\...\VITA57Interface.SchDoc
Drawn By: J.D. Kurtze


U9N
XC5VLX30T-1FFG665C
U9O
XC5VLX30T-1FF665C
U9P
NC
M5
XC5VLX30T-1FF665C
C_3P3V
VCCAUX2V5
VCCINT1V0
C_1P8V
VADJ
VIO_B_M2C
AVCC1V0
AVCCPLL1V2
AVTTRX1V2
AVTTTX1V2
GND
MGTAVCC_112
MGTAVCC_114
MGTAVCC_116
MGTAVCC_118
MGTAVCCPLL_112
MGTAVCCPLL_114
MGTAVCCPLL_116
MGTAVCCPLL_118
MGTAVTTRXC
MMZ2012R102A
Xilinx XC5VLX30T-FF665 recommended bypass
VCCINT
330µF 2.2µF 0.22µF
VCCAUX
33µF 2.2µF 0.22µF
VCCO (per 40 I/O Bank)
47µF 2.2µF 0.22µF
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
S14 Eval
FPGA Power
Size
B
Number
Revision
C
Date: 2/10/2012
Sheet 6 of 7
File: H:\Work\..\FPGAPwr.SchDoc
Drawn By: J.D. Kurtze


EDZ350/2
JP1
D5
S2G-13
T1
ACM1211-701-2PL
J2
PJ-102AH
C69
47uF
PGND
C4
330uF
R2
249
D1
BG1101W-TR
V_5P0
R36
10K
EN_PWR
S1
PTS525SM10SM
GND
TP2
TP4
TP1
TP3
VADJ_S1 VADJ_S0 VADJ
0 0 1.5V
0 1 1.8V
1 0 2.5V
1 1 3.3V
U24A
ISL54059IRTZ
C_3P3V
R83 2K
R84 2.61K
VADJ
C253
47uF
U24B
ISL54059IRTZ
R70 4.02K
R72 5.62K
VADJ_S0
L20
FBMH3225HM601NT
U16
ISL80103IRAJZ
C56
10uF
M_VADJ_EN
R82
10K
C48
1000pF
PG_C2M
VADJ_FB
VADJ_S1
R28
1K
U25A
ISL54059IRTZ
U25B
ISL54059IRTZ
L17
U20
ISL80103IRAJZ
C58
10uF
EN_PWR
C259
1000pF
C_3P3V_FB
PG_C
R95
5.62K
C62
47uF
R96
1K
L6
U6
ISL80103IRAJZ
VCCAUX2V5
C15
10uF
C84
1000pF
VCCAUX2P5_FB
R45
4.02K
C22
47uF
R43
1K
D4
RS3AB-13-F
D6
U2
ISL80103IRAJZ
VCCINT1V0
C6
10uF
C13
1000pF
VCCINT1P0_FB
R39
DNP
C16
330uF
R38
L3
U3
ISL80103IRAJZ
C_1P8V
C7
10uF
C72
1000pF
C_1P8V_FB
R41
2.61K
C14
47uF
R40
1K
C2
0.22uF
C3
10uF
L1
IHLP1616BZERR22M01
0.22uH
R1
10
C5
1uF low ESR
U1
ISL8204M
PVCC
VIN
PHASE
VOUT
COMP/EN
ISET
FB
EN_PMOD
PGND
R35
2.2
C68
1000pF
C70
330uF
C67
10uF
C1
10uF
R37
14K
C12
22uF
C8
22uF
C71
22uF
C9
330uF
U22
74LVCE1G07 SOT25
L5
U5
ISL80101IRAJZ
C11
10uF
C_3P3V
R30
10K
1000pf
C18
AVTTTX1V2_FB
PG_C
R7
1.4K
R4
1K
C98
330uF
AVTTTX1V2
L4
U4
ISL80101IRAJZ
C10
10uF
C17
AVTTRX1V2_FB
R6
1.4K
R3
1K
C97
330uF
AVTTRX1V2
L19
U15
ISL80101IRAJZ
C55
10uF
C251
AVCCPLL1V2_FB
R25
1.4K
R27
1K
C243
330uF
AVCCPLL1V2
L18
U14
ISL80101IRAJZ
C54
10uF
C250
AVCC1V0_FB
R24
1K
R26
1K
C242
330uF
AVCC1V0
NOTE: AVCCPLL1V2 must be
1.2V for LXT FPGA
1.0V for FXT FPGA
L16
U13
ISL80103IRAJZ
M_3P3V
C46
10uF
C241
M_3P3V_FB
R76
5.62K
R69
10K
R71
1K
C47
47uF
Assembly Variant: Standard
INTERSIL PROPRIETARY AND CONFIDENTIAL. SUBJECT TO NONDISCLOSURE AGREEMENT
Title
S14 Eval Power Regulation
Size B
Number
Revision C
Date: 2/10/2012
Sheet 7 of 7
File: H:\Work\..\Power.SchDoc
Drawn By: J.D. Kurtze