8x4 FIFO using BRAM
SLG47910

This application shows how to design 8x4 FIFO using the onboard Block RAM(BRAM). Simulation waveforms generated by GTKWave software can be used to verify the functionality of the design.

Contents

Terms and Definitions

FPGA	Field Programmable Gate Array
FIFO	First-In-First-Out Memory
BRAM	Block RAM
FPGA Core	Circuit Block that contains the digital array macro cells
ForgeFPGA Workshop	Top level FPGA display and control window
FPGA Editor	Main FPGA design and simulation window
CLB	Configuration Logic Block

References

For related documents and software, please visit

ForgeFPGA Low-density FPGAs | Renesas

Download our free ForgeFPGA™ Designer software [1] to open the. ffpga design files [2] and view the proposed circuit design.

[1] Go Configure Software Hub, Software Download and User Guide

[2] AN-FG-011 BRAM FIFO Design.ffpga, ForgeFPGA Design File

[3] SLG47910, Preliminary Datasheet

1. Introduction

This application shows how to use the SLG47910's embedded Block RAM (BRAM) to design an 8x4 FIFO. The 8x4 FIFO is clocked by two external clocks (wclk_in and rclk_in). CLBs are used to implement the EMPTY_FLAG and FULL_FLAG.

There are eight BRAM slices on the SLG47910 device with configurable depths and widths. The top-level BRAM placements are shown in Figure 1.This FIFO implementation uses BRAM_0 slice that is configured as a 512x8 SRAM but only four data bits (x4) are used.

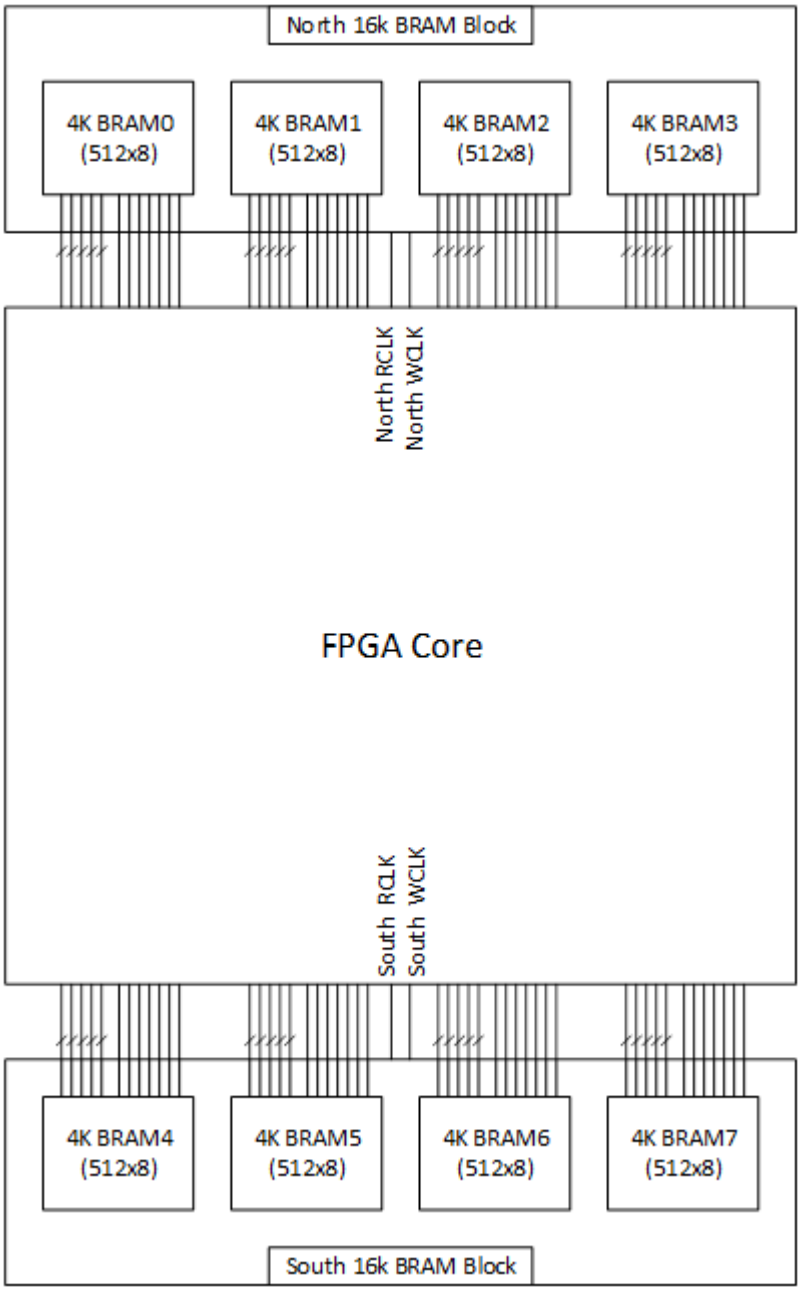

Figure 1 : FPGA Core and BRAM Blocksc

2. FIFO Description

In this design example the BRAM is configured as 512x8 by setting RATIO[1:0] = 2'b00. The address space has a depth of eight so only a small portion of the BRAM address space is used. Only DIN[3:0] and DOUT[3:0] are used during write and read cycles. The BRAM inputs and its description are shown in Figure 3 and Table 1. The BRAM clocks, WCLK and RCLK are driven by GPIOs. The FIFO block diagram is shown in Figure 2. The Write

Pointer and Read Pointer generate the addresses for the BRAM. The Flag Logic keeps track of when the FIFO is full or empty by comparing the difference between the write and read addresses.

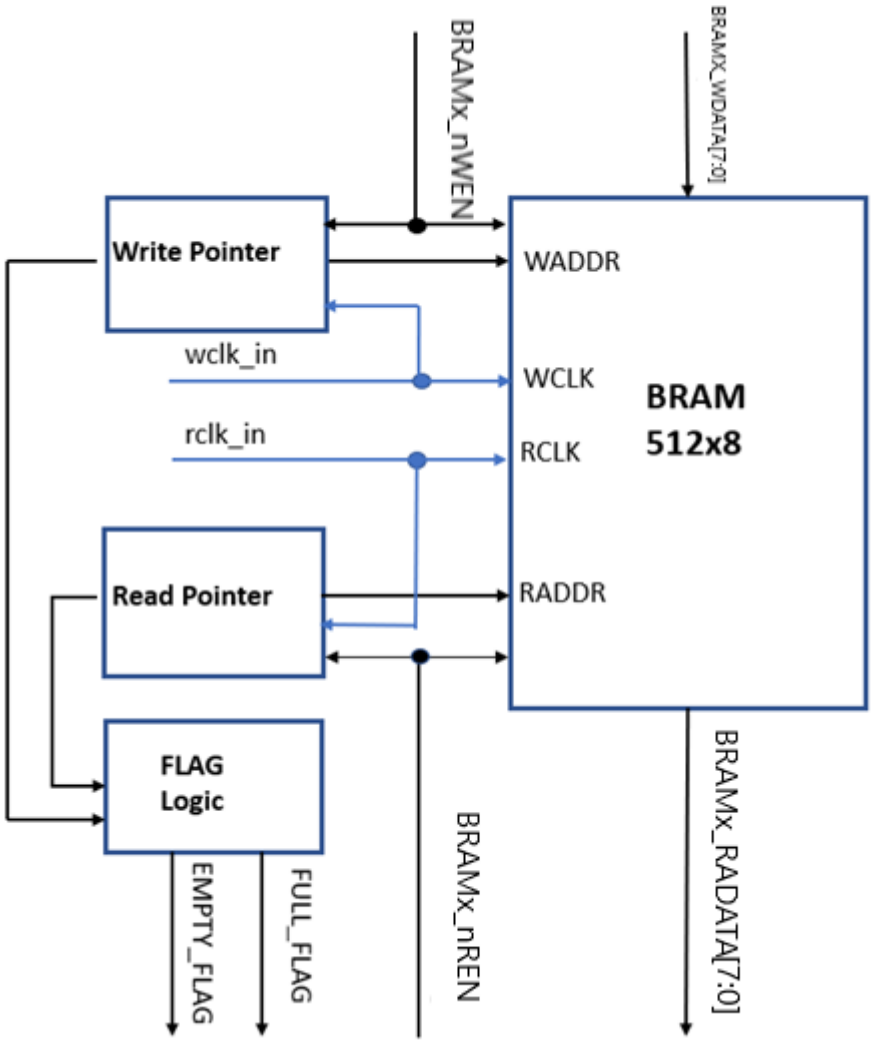

Figure 2: 5x4 FIFO with FULL & EMPTY FLAGs

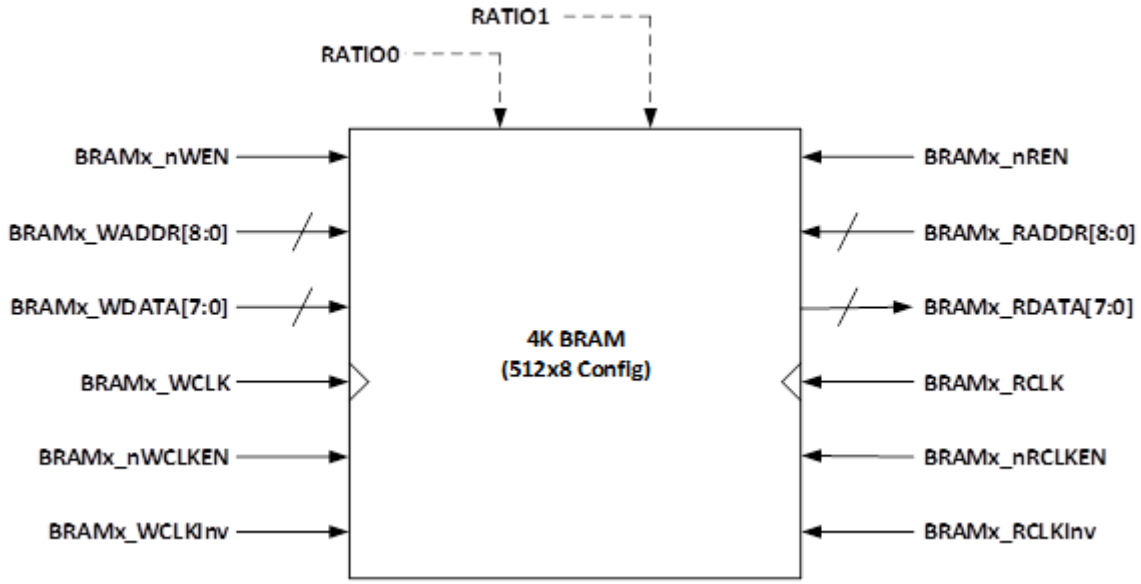

Figure 3: BRAM Slice Structure

Table 1: BRAM Slice Signal Description

Name	Direction	Description
BRAMx_nWEN	Input	Write Enable (active low)
BRAMx_WADDR[8:0]	Input	Write Address Bits; for anything deeper than 512, the unused DIN's can be repurposed as WADDR
BRAMx_WDATA[7:0]	Input	Data Input Bits
BRAMx_nWCLKEN	Input	Write Clock Enable (active low)
BRAMx_WCLKInv	Input	Write Clock Inversion Control
BRAMx_RCLKInv	Input	Read Clock Inversion Control
BRAMx_nRCLKEN	Input	Read Clock Enable (active low)
BRAMx_RDATA[7:0]	Output	Data Output Bits
BRAMx_RADDR[8:0]	Input	Read Address Bits; for anything deeper than 512, the unused DIN's can be repurposed as RADDR
BRAMx_nREN	Input	Read Enable (active low)
BRAMx_WCLK	Input	Write Clock (default Rising Edge, but with falling edge option)
BRAMx_RCLK	Input	Read Clock (default Rising Edge, but with falling edge option)
RATIO[1:0]	Input	Data Width Selection Bits 00: 512 x 8 01: 1024 x 4 10: 2048 x 2 11: 4096 x 1

3. Ingredients

- SLG47910 Device
- ForgeFPGA Development Board and power cables

- ForgeFPGA Socket Adaptor Board
- Latest Revision of the ForgeFPGA Workshop software

4. FIFO Verilog Code

The BRAM_FIFO design is available for download (FIFO using BRAM.ffpga). It contains the complete FIFO design using the BRAM module and the Digital array of the SLG47910 device. The desired BRAM is used by specifying the number BRAM0, BRAM1, etc. The nReset input resets the addresses and flag logic. The address space of the FIFO can be modified by adjusting the DEPTH parameter.

Shown below is the (*top*) module named FIFO_BRAM's input -output ports. The Verilog code for 8x4 FIFO using BRAM can be found in the complete design example. It is available for download (AN-FG-011 FIFO using BRAM.ffpga).

Multiple `always` block in the Verilog code allows the user to configure the read and the write clock of the BRAM according to their use.

```
(*top*) module FIFO_BRAM #(
  parameter DEPTH = 3
)(
   (* iopad_external_pin *)input nReset,
   (* iopad_external_pin, clkbuf_inhibit *)input wclk,
   (* iopad_external_pin, clkbuf_inhibit *) input rclk,
   (* iopad_external_pin *) input wclk_in,
   (* iopad_external_pin *) input rclk_in,
   (* iopad_external_pin *) output wclk_out,
   (* iopad_external_pin *) output rclk_out,
   (* iopad_external_pin *) input [3:0] DIN,
   (* iopad_external_pin *) input WE,
   (* iopad_external_pin *) input RE,
   (* iopad_external_pin *) output reg [3:0] DOUT,
   (* iopad_external_pin *) output DOUT0_oe,
   (* iopad_external_pin *) output DOUT1_oe,
   (* iopad_external_pin *) output DOUT2_oe,
   (* iopad_external_pin *) output DOUT3_oe,
   (* iopad_external_pin *) output reg FIFO_full,
   (* iopad_external_pin *) output reg FIFO_empty,
   (* iopad_external_pin *) output FIFO_full_oe,
   (* iopad_external_pin *) output FIFO_empty_oe,
   (* iopad_external_pin *) output [1:0] BRAM0_RATIO,
   (* iopad_external_pin *) output reg [7:0] BRAM0_DATA_IN,
   (* iopad_external_pin *) output reg BRAM0_WEN,
   (* iopad_external_pin *) output reg BRAM0_WCLKEN,
   (* iopad_external_pin *) output reg [8:0] BRAM0_WRITE_ADDR,
   (* iopad_external_pin *) input [3:0] BRAM0_DATA_OUT,
   (* iopad_external_pin *) output reg BRAM0_REN,
   (* iopad_external_pin *) output reg BRAM0_RCLKEN,
   (* iopad_external_pin *) output reg [8:0] BRAM0_READ_ADDR,
   (* iopad_external_pin *) output ext_en0, //external clock
   (* iopad_external_pin *) output ext_en1 //external clock
  );
```

5. Floorplan : CLB Utilization

From the below Figure 4, we can see a part of the floorplan for this application note. Also, on the left corner of the figure we can see a mini resource needed list.

From the Verilog code the user can observe that only BRAM_0 has been used for this application and all the other BRAM_[1:7] has been disabled. This can also be observed under the floorplan tab in the software and in Figure 5.

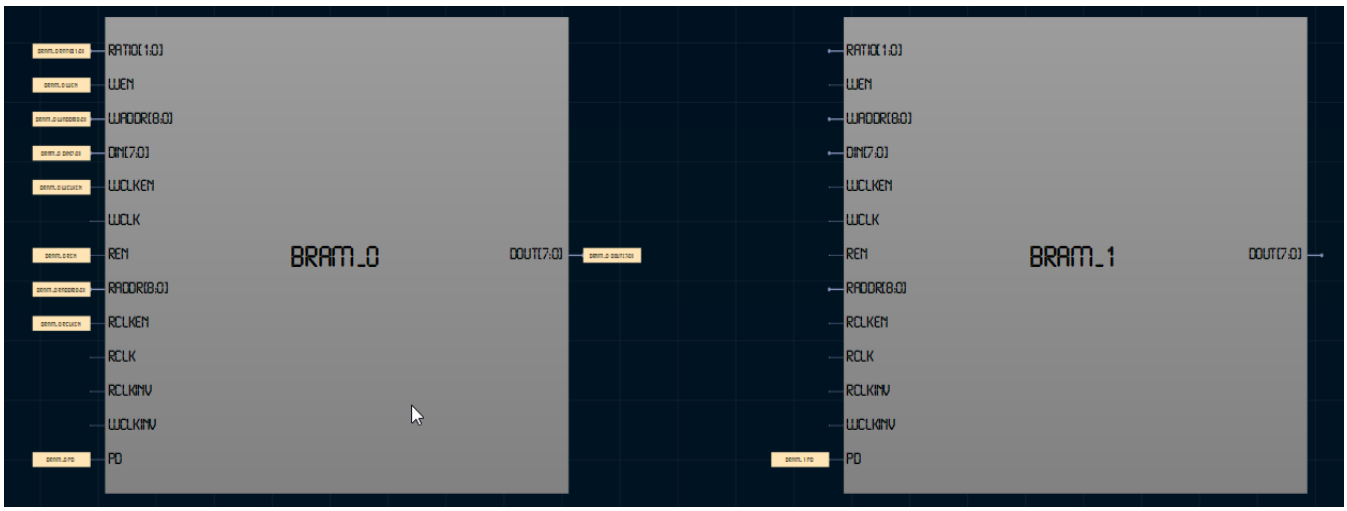

Figure 5 : BRAM_0 is being used and BRAM_1 is not being used

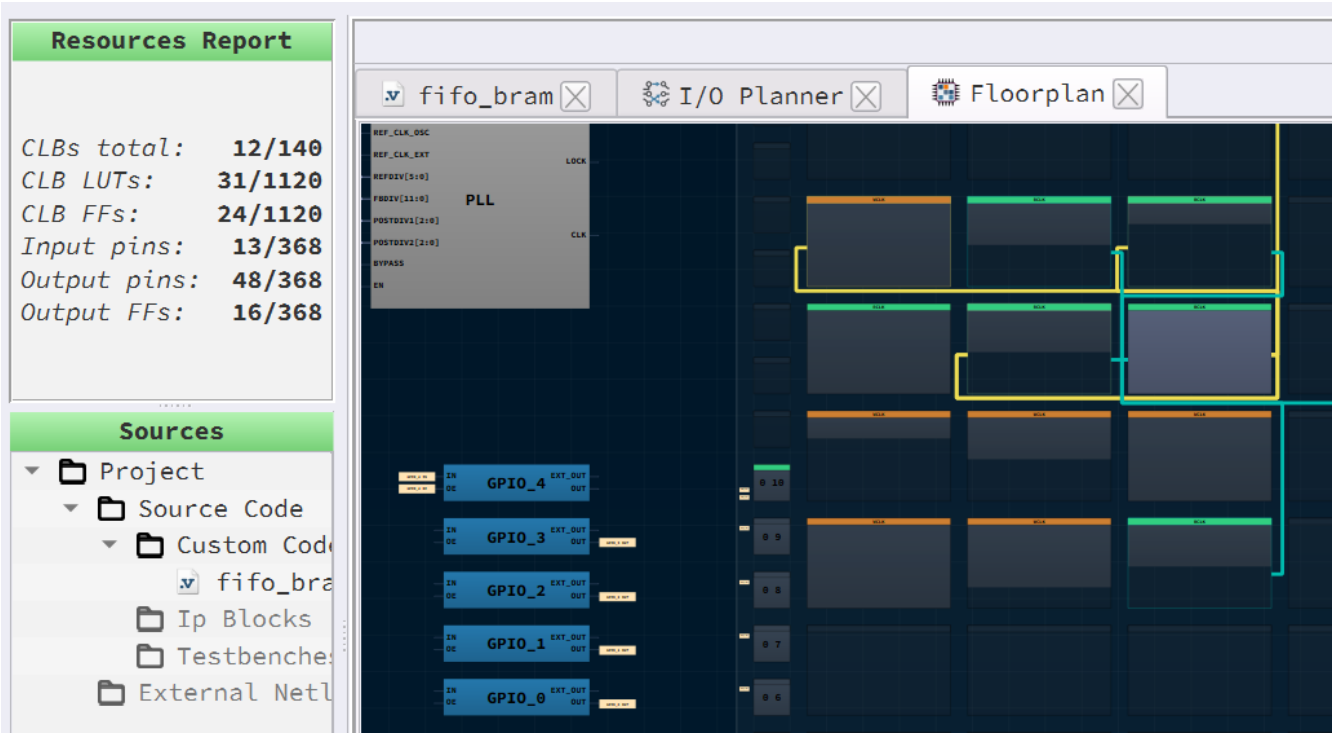

Figure 4 : Floorplan

6. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.

2. From the ForgeFPGA tool bar, select the FPGA Editor tab.

3. Enter the Verilog code into the HDL editor and save the code using the save button on the top left corner of the FPGA Editor.

4. Open the IO planner tab on the FPGA editor. Assign the IOs that are in the Verilog code to GPIO pins on the device and save. (Figure 6)

5. Next select the Synthesize button on the lower left side of the FPGA editor. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit steam was generated correctly.

6. Now click on the Floorplan tab and see the CLB utilization. Press the Ctrl and the mouse wheel to zoom-in. (Figure 4). Confirm that the IOs selected in the IO Planner (Figure 6) are shown in the floorplan. The IO Planner has been set in such a way that the board uses an external clock instead of the OSC clock on-board also that we use only BRAM_0 for this application and disable the other BRAMs on board.

POSITION	FUNCTION	PORT
IOB tile[0, 0] coord[0, 6] Input0	[PIN 13] GPIO0_IN	DIN[0]
IOB tile[0, 0] coord[0, 7] Input0	[PIN 14] GPIO1_IN	DIN[1]
IOB tile[0, 0] coord[0, 8] Input0	[PIN 15] GPIO2_IN	DIN[2]
IOB tile[0, 0] coord[0, 9] Input0	[PIN 16] GPIO3_IN	DIN[3]
IOB tile[0, 0] coord[0, 10] Output1	[PIN 17] GPIO4_OE	DOUT0_oe
IOB tile[0, 0] coord[0, 22] Output1	[PIN 18] GPIO5_OE	DOUT1_oe
IOB tile[0, 0] coord[0, 23] Output1	[PIN 19] GPIO6_OE	DOUT2_oe
IOB tile[0, 0] coord[0, 24] Output1	[PIN 20] GPIO7_OE	DOUT3_oe
IOB tile[0, 0] coord[0, 10] Output0	[PIN 17] GPIO4_OUT	DOUT[0]
IOB tile[0, 0] coord[0, 22] Output0	[PIN 18] GPIO5_OUT	DOUT[1]
IOB tile[0, 0] coord[0, 23] Output0	[PIN 19] GPIO6_OUT	DOUT[2]
IOB tile[0, 0] coord[0, 24] Output0	[PIN 20] GPIO7_OUT	DOUT[3]
IOB tile[0, 0] coord[31, 26] Output0	[PIN 24] GPIO9_OUT	FIFO_empty
IOB tile[0, 0] coord[31, 26] Output1	[PIN 24] GPIO9_OE	FIFO_empty_oe

Figure 6a: IO Planner

POSITION	FUNCTION	PORT
IOB tile[0, 0] coord[31, 27] Output0	[PIN 23] GPIO8_OUT	FIFO_full
IOB tile[0, 0] coord[31, 27] Output1	[PIN 23] GPIO8_OE	FIFO_full_oe
IOB tile[0, 0] coord[31, 24] Input0	[PIN 2] GPIO11_IN	RE
IOB tile[0, 0] coord[31, 25] Input0	[PIN 1] GPIO10_IN	WE
IOB tile[0, 0] coord[31, 12] Output0	DATA_AS_CLK0_EN	ext_en0
IOB tile[0, 0] coord[31, 12] Output1	DATA_AS_CLK1_EN	ext_en1
IOB tile[0, 0] coord[31, 11] Input0	FPGA_CORE_READY	nReset
CLK tile[0, 0] clk_side=E Input0	DATA_AS_CLK0	rclk
CLK tile[0, 0] clk_side=N Output0	REF_BRAM(0..3)_READ_CLK	rclk
IOB tile[0, 0] coord[31, 23] Input0	[PIN 3] GPIO12_IN	rclk_in
IOB tile[0, 0] coord[31, 11] Output0	REF_DATA_AS_CLK0	rclk_out
CLK tile[0, 0] clk_side=E Input1	DATA_AS_CLK1	wclk
CLK tile[0, 0] clk_side=N Output1	REF_BRAM(0..3)_WRITE_CLK	wclk
IOB tile[0, 0] coord[31, 22] Input0	[PIN 4] GPIO13_IN	wclk_in
IOB tile[0, 0] coord[31, 11] Output1	REF_DATA_AS_CLK1	wclk_out

Figure 6b: IO Planner

8. Once the user is satisfied with the design code, the user can Debug the design file. Close the FPGA Editor and go to the ForgeFPGA widow. Selecting the Debug tab will enable the debug controls. Double click on the VDD pin and set VDD= 1.2v. Then double click on VDDIO pin and set VDDIO= 1.8v.

9. In the ForgeFPGA Workshop window, select Change platform on the Debugging Controls tab. Choose the ForgeFPGA Development Platform then select Emulation. The Emulation button will toggle the design on and off.

11. Apply the desired inputs from GPIO[0-3] and observed the DOUT through GPIO[4-7]. GPIO8 will indicate if the FIFO is full and GPIO9 will indicate if the FIFO pipeline is empty. The user can observe waveforms through the inbuilt Logic Analyzer (Figure 8), or the user can connect the desired GPIOs to an oscilloscope to observe the waveforms.

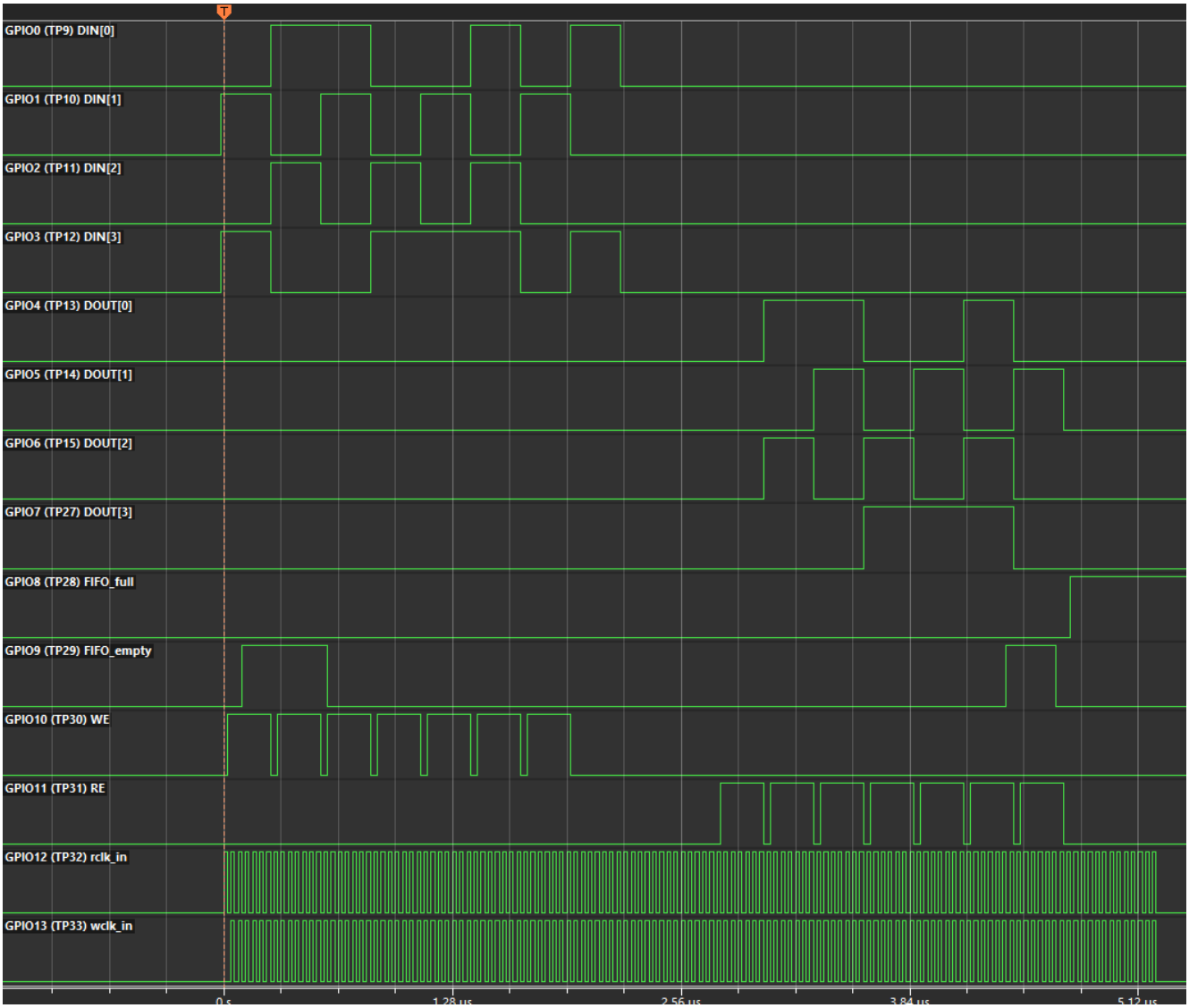

Figure 8: Output on Logic Analyzer

7. Conclusion

The procedure outlined in this application note can applied to any BRAM the user wants to use to implement this design. Similar procedure needs to be followed to implement the BRAM of different Ratio or use a different BRAM[1-3].Make changes at the appropriate place to observe the correct results. The FIFO using BRAM.ffpga design file is ready for download.

If interested, please contact the ForgeFPGA Business Support Team.

8. Revision History

Revision	Date	Description
1.00	Feb 15, 2023	Initial release.
2.0	Feb 23, 2024	Updated according to K1BB revision

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