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April 1st, 2010
Renesas Electronics Corporation

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H8/300H Tiny Series

64-Bit Binary Addition (ADD)

Introduction

Performs binary addition in this format:

augend (unsigned, 64 bits) + addend (unsigned, 64 bits) = sum (unsigned, 64 bits).

Target Device

H8/300H Tiny Series

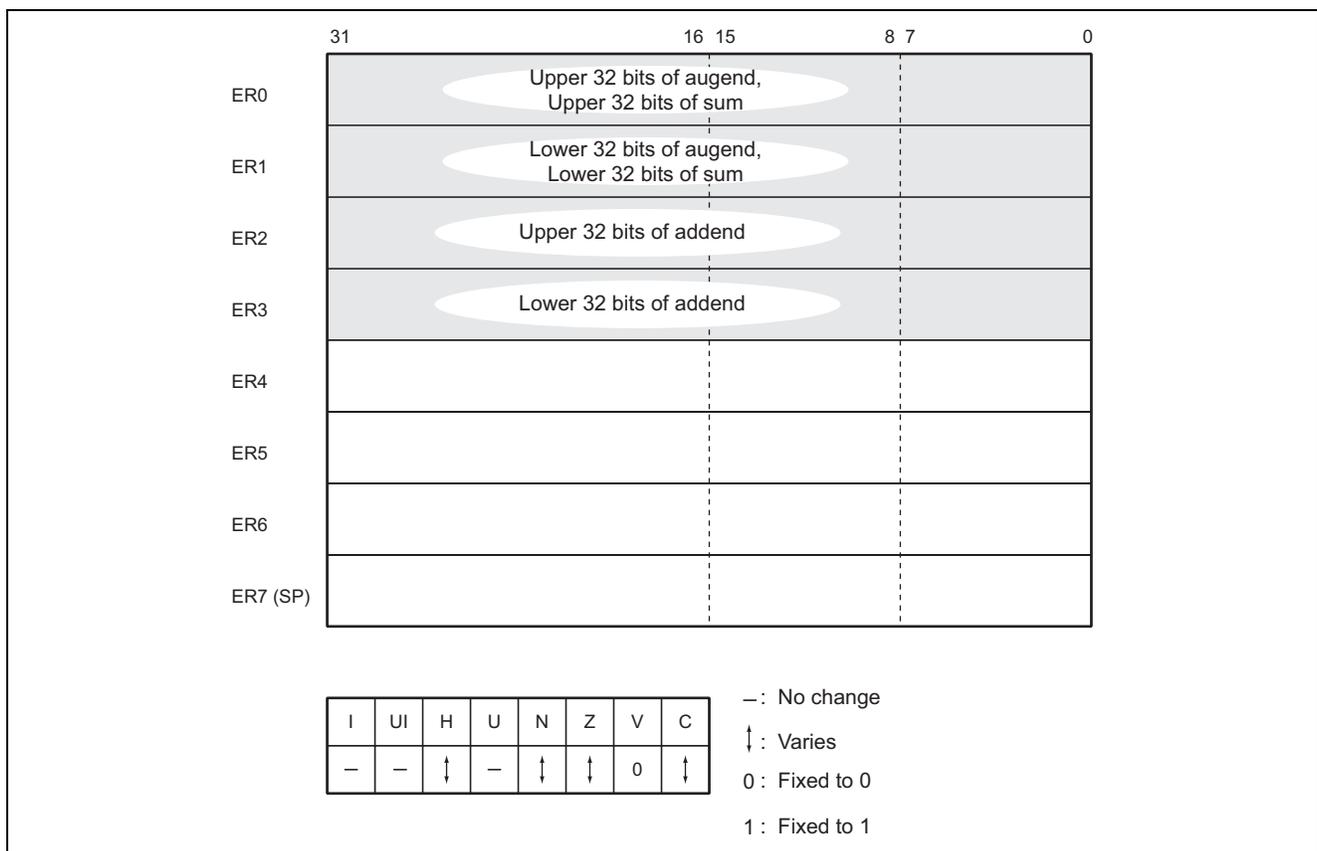
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1. Arguments

Contents		Storage Location	Data Length (Bytes)
Input	Upper 32 bits of the augend (unsigned, 64 bits)	ER0	4
	Lower 32 bits of the augend (unsigned, 64 bits)	ER1	4
	Upper 32 bits of the addend (unsigned, 64 bits)	ER2	4
	Lower 32 bits of the addend (unsigned, 64 bits)	ER3	4
Output	Upper 32 bits of the sum (unsigned, 64 bits)	ER0	4
	Lower 32 bits of the sum (unsigned, 64 bits)	ER1	4
	Presence of carry (yes = 1, no = 0)	C flag (CCR)	—

2. Changes to Internal Registers and Flags



3. Programming Specifications

Program memory (bytes)	18
Data memory (bytes)	0
Stack (bytes)	0
Number of cycles	26
Re-entrant	Yes
Relocatable	Yes
Interrupts during execution	Yes

4. Description

4.1 Description of Functions

- The arguments are as follows.
 - ER0: Set the upper 32 bits of the augend (unsigned 64 bits) as an input argument. The upper 32 bits of the sum (unsigned 64 bits) are also set here, as an output argument.
 - ER1: Set the lower 32 bits of the augend as an input argument. The lower 32 bits of the sum are also set here, set as an output argument.
 - ER2: Set the upper 32 bits of the addend (unsigned 64 bits) as an input argument.
 - ER3: Set the lower 32 bits of the addend as an input argument.
 - C flag (CCR): indicates whether a carry has occurred after the ADD subroutine has been executed.
 - C flag = 1: indicates a carry.
 - C flag = 0: indicates no carry.
- The following figure illustrates the execution of the ADD subroutine. When the input arguments are set as shown below, ADD sets the result of addition in ER0 and ER1.

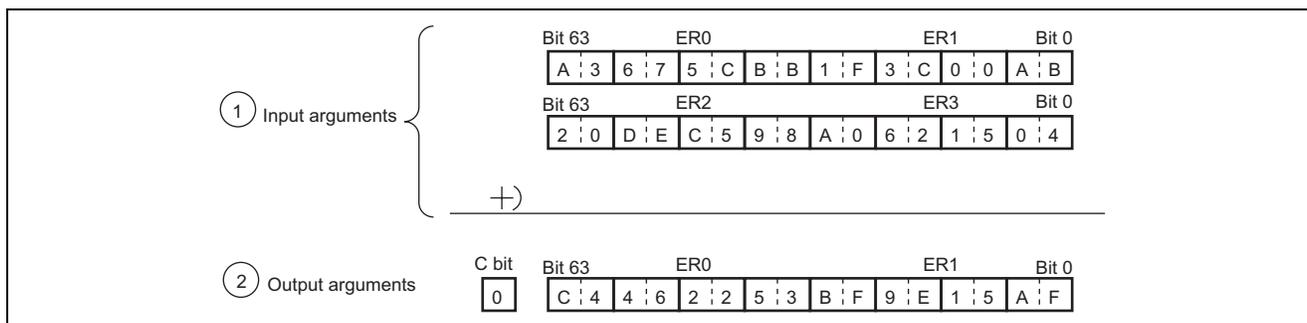


Figure 1 Example of ADD Execution

4.2 Usage Notes

Since the result of addition is placed in the registers used to set the augend, the augend is lost through the execution of ADD. If you will still require the augend, save it elsewhere in memory beforehand.

4.3 Description of Data Memory

No data memory is used by ADD.

4.4 Example of Usage

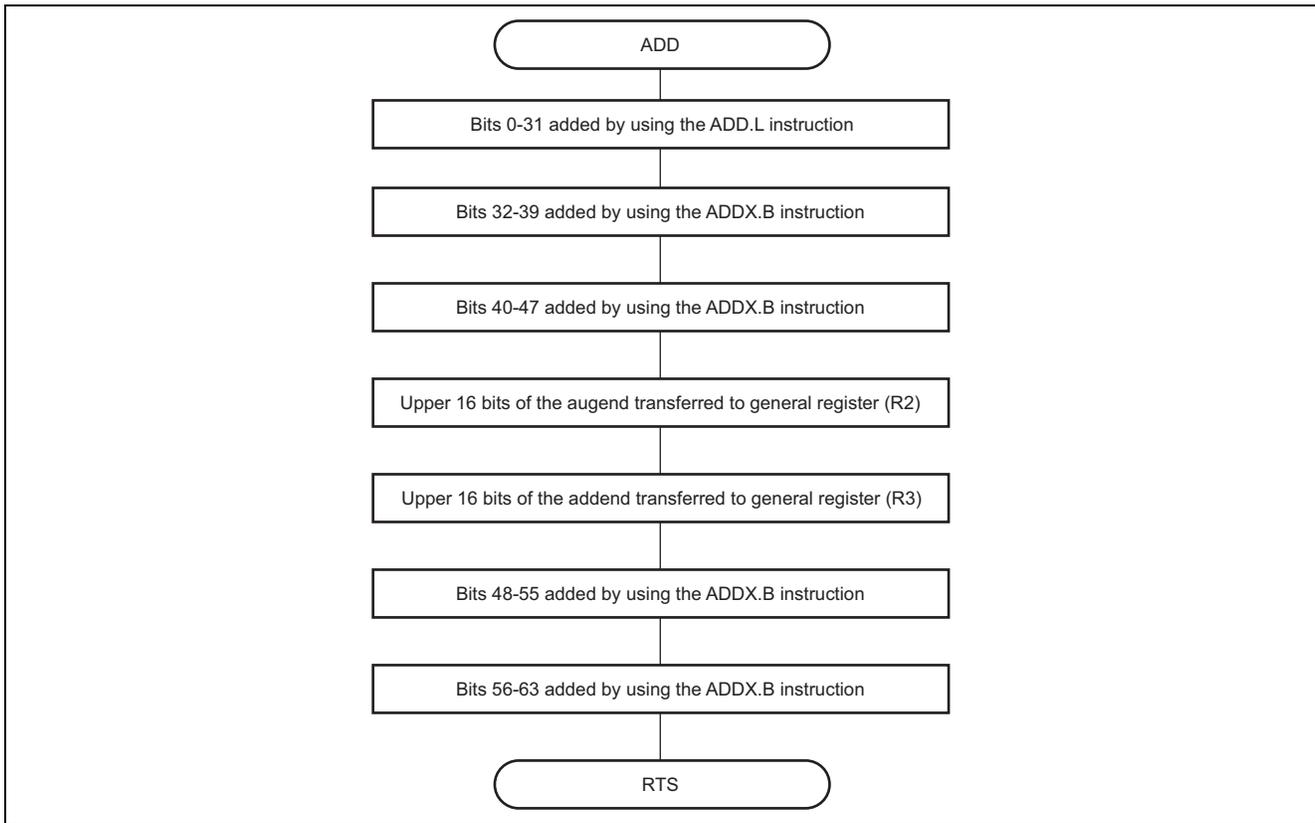
After setting the augend and addend, call the ADD subroutine.

WORK1	. RES. L 1	Reservation of the data memory area for setting of the upper 32 bits of the augend (unsigned, 64 bits) by the user program.
WORK2	. RES. L 1	Reservation of the data memory area for setting of the lower 32 bits of the augend by the user program.
WORK3	. RES. L 1	Reservation of the data memory area for setting of the upper 32 bits of the addend (unsigned, 64 bits) by the user program.
WORK4	. RES. L 1	Reservation of the data memory area for setting of the lower 32 bits of the addend by the user program.
	MOV. L @WORK1, ER0	Sets, in the input argument, the upper 32 bits of the augend specified by the user program.
	MOV. L @WORK2, ER1	Sets, in the input argument, the lower 32 bits of the augend specified by the user program.
	MOV. L @WORK3, ER2	Sets, in the input argument, the upper 32 bits of the addend specified by the user program.
	MOV. L @WORK4, ER3	Sets, in the input argument, the lower 32 bits of the addend specified by the user program.
	.		
	.		
	JSR @MOVE	Subroutine call of ADD
	BCS OVER	When a carry has occurred, branches to the routine for processing a carry.
OVER	Processing routine for carrying over		

4.5 Principles of Operation

1. Addition of bits 0-31 is carried out by using the ADD.L instruction.
2. The addition-with-carry instruction (ADDX.B) is used to add bits 32-63 in byte units from the lowest-order byte. Since bits 48-55 are in an extended register, to which the addition-with-carry instruction is not applicable, the addition with carry is performed after the data in these bits have been transferred to a general register.

5. Flowchart



6. Program Listing

```

1          1          ;*****
2          2          ;*
3          3          ;*      NAME      :      64 BIT BINARY ADDITION  (ADD)      *
4          4          ;*
5          5          ;*****
6          6          ;*
7          7          ;*      ENTRY      :      ER0          (UPPER 32 BIT AUGEND)      *
8          8          ;*
9          9          ;*
10         10         ;*      ER1          (LOWER 32 BIT AUGEND)      *
11        11         ;*      ER2          (UPPER 32 BIT ADDEND)      *
12        12         ;*      ER3          (LOWER 32 BIT ADDEND)      *
13        13         ;*      RETURNS   :      ER0          (UPPER 32 BIT SUM)      *
14        14         ;*      ER1          (LOWER 32 BIT SUM)      *
15        15         ;*      CARRY      (C=0;TRUE , C=1;OVERFLOW)      *
16        16         ;*
17        17         ;*****
18        18         ;
19        19         .CPU          300HA
20        20         .SECTION A, CODE, LOCATE=H'001000
21        21         ADD          .EQU          $          ;Entry point
22        22         00001000
23        23         ADD          ADD.L        ER3,ER1      ;Lower 48 bit binary addition
24        24         001000 0AB1
25        25         ADD          ADDX.B       R2L,R0L      ;
26        26         001002 0EA8
27        27         ADD          ADDX.B       R2H,R0H      ;
28        28         001004 0E20
29        29         MOV          MOV.W        E0,R2        ;Upper 16 bit binary addition
30        30         001006 0D82
31        31         MOV          MOV.W        E2,R3        ;
32        32         001008 0DA3
33        33         ADD          ADDX.B       R3L,R2L      ;
34        34         00100A 0EBA
35        35         ADD          ADDX.B       R3H,R2H      ;
36        36         00100C 0E32
37        37         MOV          MOV.W        R2,E0        ;
38        38         00100E 0D28
39        39         RTS
40        40         001010 5470
41        41         .END
42        42
43        43         *****
44        44         TOTAL   ERRORS      0
45        45         *****
46        46         TOTAL   WARNINGS   0

```

Note: The program listing included in this application note assumes compilation under the option for the advanced mode of H8/300H CPU. If you use this sample program with an H8/300H Tiny Series product, make the following change to the program code:

.CPU 300HA → .CPU 300HN

Revision Record

Rev.	Date	Description	
		Page	Summary
2.00	Feb.28.06	—	Format has been changed from Hitachi version to Renesas version.

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