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April 1st, 2010
Renesas Electronics Corporation

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Recommended PCB Layout for Anti-noise

The main differences are shown from number one to five in the Figure 2. The PCB layout should be designed in accordance with recommended one to achieve better performance. The reasons why the PCB layout on the left is recommended are elaborated in next part (3.2 Recommended layout).

The PCB layout are shown below:

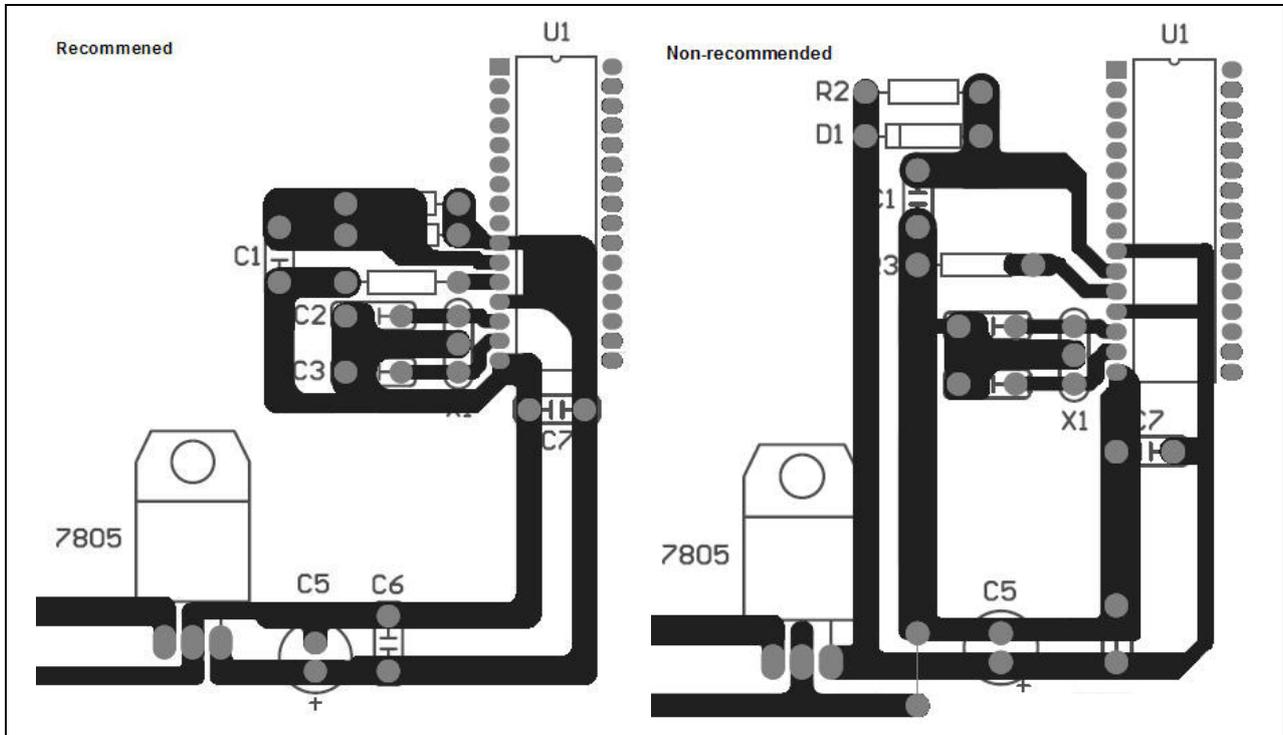


Figure 2 Recommended Layout (Left) and Not Recommended Layout (Right)

Note:

Both of the PCB layouts shown above have been tested.

Component package: DIP

PCB type: Single layer board without polygon

3.2 Recommended layout

Here are some PCB design principles to reduce the noise effect.

3.2.1 Oscillator circuit

To reduce the noise effect, the oscillator wirings pattern should be as short to MCU as possible. The wiring pattern of VSS line for oscillator and MCU should be separated from other peripheral's VSS pattern. Refer to Figure 2 (number 1 in the yellow circle).

<Reason>: Long wires may have an antenna effect to catch large noise. If noise enters the clock I/O pins, clock waveform may be deformed. This may cause a program failure or runaway. Also if the potential difference is caused by the noise between the oscillator VSS level and a MCU VSS level, the correct clock will not be input in the MCU.

3.2.2 Reset circuit

In the same way, the reset circuit should be as close to MCU as possible. Refer to Figure 2 (number 2 in the green circle).

<Reason>: The reset signal initializes the internal MCU state. If fine, noise-like pulses pass through the reset signal line, the MCU may not completely initialize (partially initialized). It is better to shorten the wiring for the reset circuit to reduce the noise influence.

3.2.3 CNVSS circuit

Use a 1k - 5k Ω serial connection to connect the CNVSS/VPP pin to the VSS pattern. Make the length of wiring pattern from the resistor to the CNVSS/VPP pin as short as possible. Refer to Figure 2 (number 3 in the pink circle).

<Reason>: If noise occurs in the CNVSS/VPP pin, the MCU may runaway.

3.2.4 Decoupling capacitor

Place the decoupling capacitor close to the MCU. Connect the capacitor across the VCC and the VSS pin in equal length. Refer to Figure 2 (number 4 in the orange circle).

<Reason>: If the MCU decoupling capacitor wiring is long, it should be noted that the line may become a noise antenna.

3.2.5 VSS wiring pattern

Wire the MCU VSS, the oscillator, the reset circuit and CNVSS pin in the same VSS branch. Refer to Figure 2 (number 5 in the brown circle).

<Reason>: If the potential difference is caused by the noise of two different VSS circuits, the program may generate a failure or runaway.

4. Anti-noise test of different layout

4.1 Test description

In this test, two types of PCB were used. One is designed according to the recommendations. The other is designed on the contra. The PCB layout around the MCU are shown above. The peripheral circuits on the two boards are the same. Equal noise interference is input to the two test boards through the power supply for one minute. The peak value of noise interfere is steps up in 100V increments from 100V to 4000V in every test.

On the target boards, there are two groups of LED lamps that blink to show the MCU status. All LED lamps will blink for five second after the MCU reset. Then the two groups of LED lamps will blink from “0000₂” to “1111₂” by “1₂”. One group is controlled by the main loop; the other group is controlled by the timer interrupt. These two groups of LED lamps will blink synchronously.

The MCU status can be evaluated by observing these LED lamps.

- If the MCU operates normally within one minute, the result is considered good and the table is filled with an “○”.
- If the MCU generates a phenomena (reset, program runaway or LED lamps blink asynchronously) within one minute, the result is considered not good and the table is filled with an “×”.

The diagram of test environment is shown below:

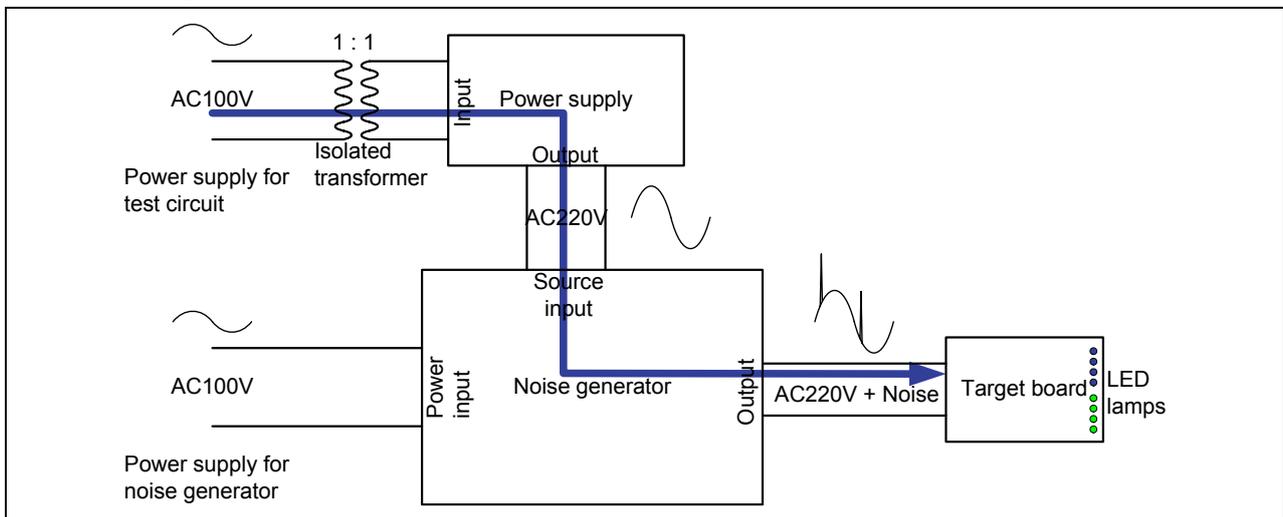
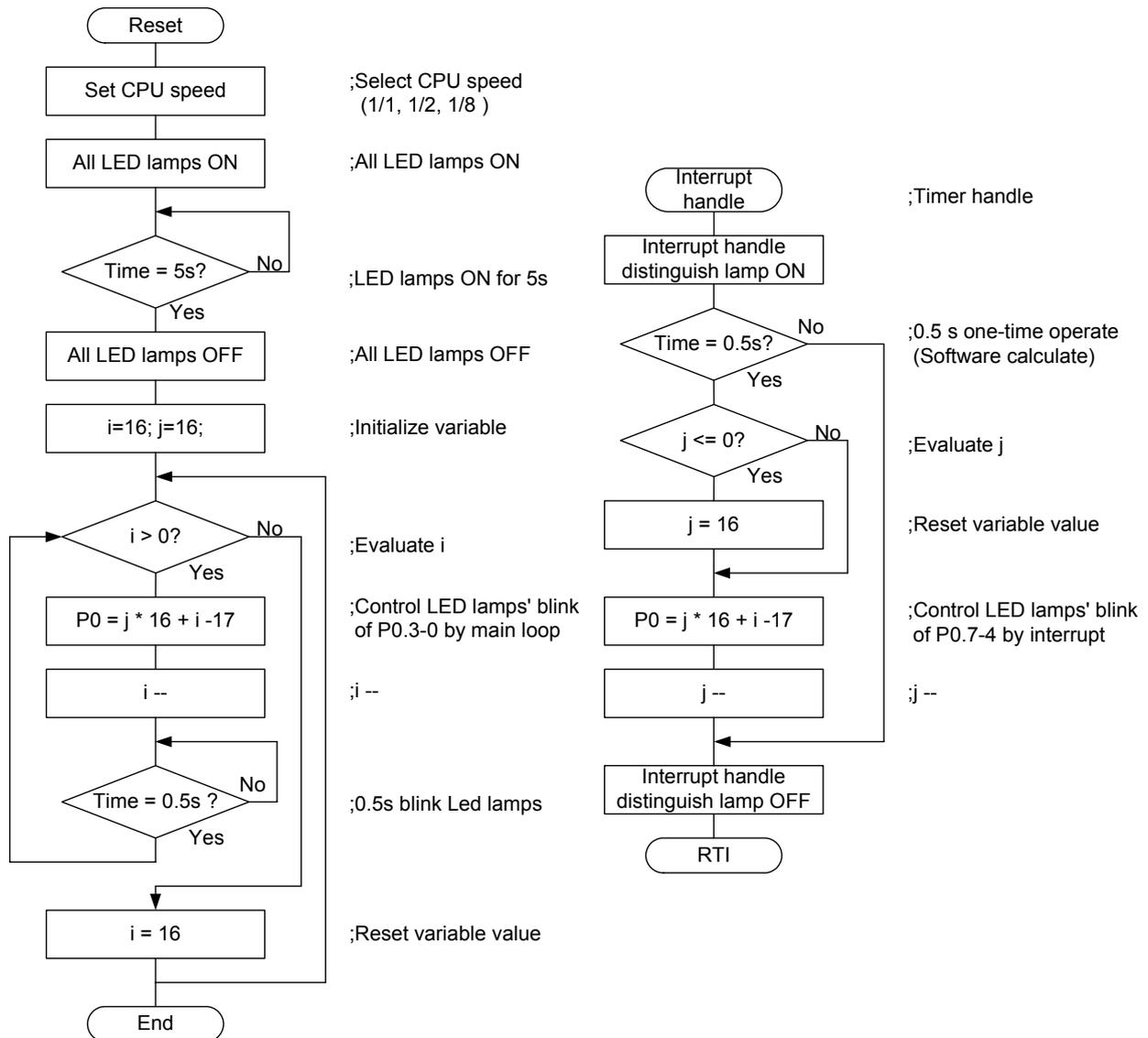


Figure 3 Diagram of Test Environment

4.2 Test conditions

- Test tools:
 - Power supply: CVFT1-200H
 - Noise generator: NoiseKen INS-4001
 - Target board: Recommended and non-recommended board
- Test conditions:
 - Target board power: 220 V 50 Hz
 - MCU type: M37544G2ASP
 - Oscillation frequency: 4 MHz
 - MCU speed: $f(xin)/1$, $f(xin)/2$ and $f(xin)/8$
 - MCU power source: 5 V
 - MCU decoupling capacitor: 0.1 uF
 - Noise period: 10 ms
 - Noise pulse width: 50 ns
 - Noise polarity: plus and minus
 - Noise peak value: 100 V to 4000 V (The maximum noise peak of the noise generator is 4000 V)
 - Test time: 1minute

4.3 Test program flow chart



4.4 Test results

Table 1: Test Results of Two PCB Layouts

Layout Polarity Voltage	Recommend Board Test Results						Non-Recommend Board Test Results					
	+			-			+			-		
4000	x	○	○	x	x	○	x	x	x	x	x	x
3900	x	○	○	x	x	○	x	x	x	x	x	x
3800	x (2)	○	○	x	x (2)	○	x	x	x	x	x	x
3700	○	○	○	x	○	○	x	x	x	x	x	x
3600	○	○	○	x	○	○	x	x	x	x	x	x
3500	○	○	○	x (2)	○	○	x	x	x	x	x	x
3400	○	○	○	○	○	○	x	x	x	x	x	x
3300	○	○	○	○	○	○	x	x	x	x	x	x
3200	○	○	○	○	○	○	x	x	x	x	x	x
3100	○	○	○	○	○	○	x	x	x	x	x	x
3000	○	○	○	○	○	○	x	x	x	x	x	x
2900	○	○	○	○	○	○	x	x	x	x	x	x
2800	○	○	○	○	○	○	x	x	x	x	x	x
2700	○	○	○	○	○	○	x	x	x	x	x	x
2600	○	○	○	○	○	○	x	x	x	x	x	x
2500	○	○	○	○	○	○	x	x	x	x	x	x
2400	○	○	○	○	○	○	x	x	x	x	x	x
2300	○	○	○	○	○	○	x	x	x	x (1)	x	x
2200	○	○	○	○	○	○	x	x	x	x (2)	x	x
2100	○	○	○	○	○	○	x	x	x	x (2)	x	x
2000	○	○	○	○	○	○	x	x	x	x (2)	x	x
1900	○	○	○	○	○	○	x	x	x	x (2)	x (1)	x
1800	○	○	○	○	○	○	x	x	x	x (2)	○	x
1700	○	○	○	○	○	○	x (1)	x	x	x (2)	○	x
1600	○	○	○	○	○	○	x (2)	x	x	x (2)	○	x
1500	○	○	○	○	○	○	x (2)	x	x (1)	x (2)	○	x (1)
1400	○	○	○	○	○	○	x (2)	x (1)	○	x (2)	○	○
1300	○	○	○	○	○	○	x (2)	○	○	x (3)	○	○
1200	○	○	○	○	○	○	x (2)	○	○	○	○	○
1100	○	○	○	○	○	○	x (2)	○	○	○	○	○
1000	○	○	○	○	○	○	x (3)	○	○	○	○	○
900	○	○	○	○	○	○	○	○	○	○	○	○
800	○	○	○	○	○	○	○	○	○	○	○	○
700	○	○	○	○	○	○	○	○	○	○	○	○
600	○	○	○	○	○	○	○	○	○	○	○	○
500	○	○	○	○	○	○	○	○	○	○	○	○
400	○	○	○	○	○	○	○	○	○	○	○	○
300	○	○	○	○	○	○	○	○	○	○	○	○
200	○	○	○	○	○	○	○	○	○	○	○	○
100	○	○	○	○	○	○	○	○	○	○	○	○
Voltage CPU Speed	1/1	1/2	1/8	1/1	1/2	1/8	1/1	1/2	1/8	1/1	1/2	1/8

Note:

Voltage: Noise value (Higher value shows higher anti-noise capability)

Polarity: Noise polarity added to target board power source

CPU speed: Clock division ratio selection: f(xin)/1, f(xin)/2 and f(xin)/8

○: Normal MCU operation

x (1): Reset cannot be released; x (2): Reset → restart → reset; x (3): Main loop error or runaway

4.5 Test conclusions

The test results show the anti-noise performance of the boards tested. Resistance to noise interference on the recommended board is about 4000 V (the maximum value of the noise generator), and that on the not-recommended board is below 2000 V.

Conclusions obtained from this test are as follows:

- Higher anti-noise performance is achieved by designing a PCB layout according to the recommendations.
- For the same CPU speed, a high frequency oscillator with a high clock division ratio should be used to achieve good anti-noise performance.

Note:

Keep the MCU away from high voltage noise, even if it is designed on the recommended PCB layout. The test results are available only to distinguish the effects noise has on different types of layouts and do not represent MCU performance.

5. Improve the Non-recommended board

After the above test, modifications were made on some circuit bases on the non-recommended board and tested again under same conditions.

In this test, the non-recommended PCB board was provisionally modified to improve anti-noise performance. In developing a product, if possible, the PCB layout should be redesigned according to the recommended layout to achieve good performance.

5.1 Modification of the Non-recommended board

Modified items are listed below:

- Oscillator circuit: Cut off the original wiring pattern which connects to the VSS and connect the oscillator to the MCU VSS with a jumper to shorten the VSS wiring pattern of the oscillator circuit. Refer to the modification in the yellow section in the Figure 4.
- Reset circuit: Remove the components of the reset circuit and weld those components to the back side of the board at the short distance. Refer to the modification in the green section in the Figure 4.
- CNVSS circuit: Remove the CNVSS resister and weld it to the back side of the board to shorten the distance of the VSS wiring. Refer to the modification in the pink section in the Figure 4.
- VSS wiring pattern: Connect the VSS wiring of the MCU, the oscillator, the reset circuit and the CNVSS pin to the same VSS branch. Refer to the modification in the brown section in the Figure 4.

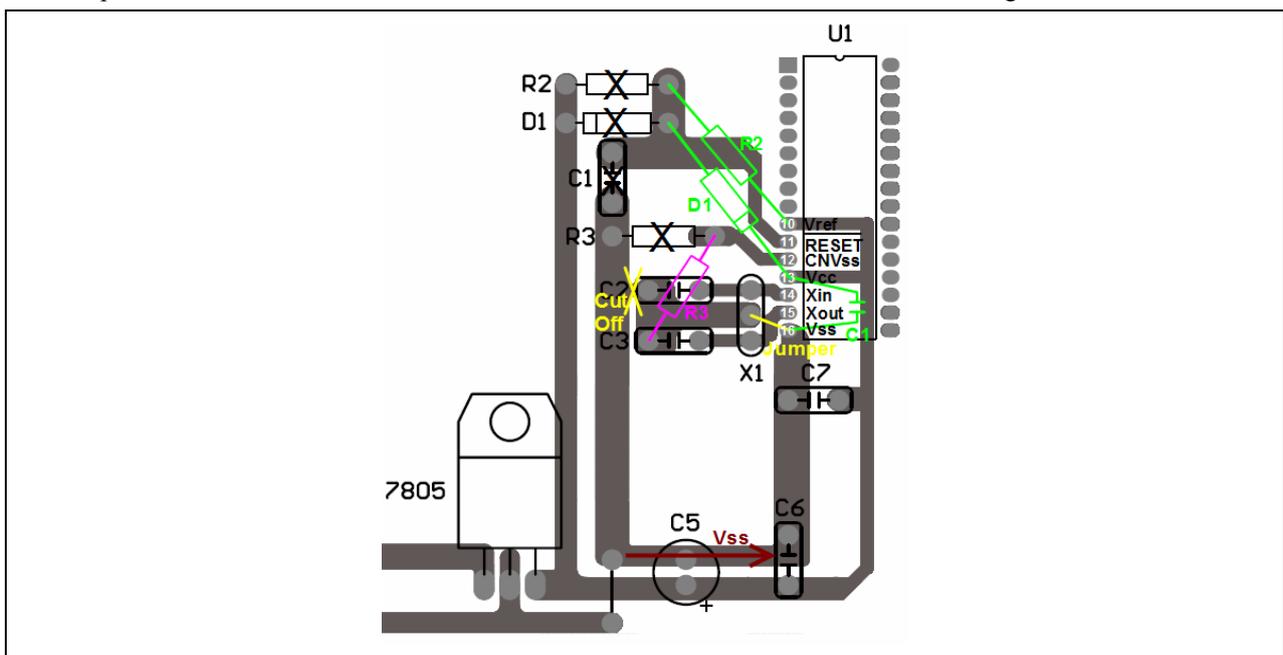


Figure 4 Improve the Non-recommended Board

5.2 Test results of modified board

Table 2 Comparison between Before and After Modification

Non-recommended Layout	After Modification						Before Modification					
	Polarity +			Polarity -			Polarity +			Polarity -		
Voltage												
4000	x	○	○	x	x	x	x	x	x	x	x	x
3900	x	○	○	x	x	x	x	x	x	x	x	x
3800	x	○	○	x	x	x	x	x	x	x	x	x
3700	x	○	○	x	x	x	x	x	x	x	x	x
3600	x	○	○	x	x	x	x	x	x	x	x	x
3500	x	○	○	x	x	x	x	x	x	x	x	x
3400	x	○	○	x	x (2)	x	x	x	x	x	x	x
3300	x	○	○	x	○	x (2)	x	x	x	x	x	x
3200	x	○	○	x	○	○	x	x	x	x	x	x
3100	x	○	○	x	○	○	x	x	x	x	x	x
3000	x	○	○	x	○	○	x	x	x	x	x	x
2900	x	○	○	x	○	○	x	x	x	x	x	x
2800	x (2)	○	○	x	○	○	x	x	x	x	x	x
2700	○	○	○	x (2)	○	○	x	x	x	x	x	x
2600	○	○	○	○	○	○	x	x	x	x	x	x
2500	○	○	○	○	○	○	x	x	x	x	x	x
2400	○	○	○	○	○	○	x	x	x	x	x	x
2300	○	○	○	○	○	○	x	x	x	x (1)	x	x
2200	○	○	○	○	○	○	x	x	x	x (2)	x	x
2100	○	○	○	○	○	○	x	x	x	x (2)	x	x
2000	○	○	○	○	○	○	x	x	x	x (2)	x	x
1900	○	○	○	○	○	○	x	x	x	x (2)	x (1)	x
1800	○	○	○	○	○	○	x	x	x	x (2)	○	x
1700	○	○	○	○	○	○	x (1)	x	x	x (2)	○	x
1600	○	○	○	○	○	○	x (2)	x	x	x (2)	○	x
1500	○	○	○	○	○	○	x (2)	x	x (1)	x (2)	○	x (1)
1400	○	○	○	○	○	○	x (2)	x (1)	○	x (2)	○	○
1300	○	○	○	○	○	○	x (2)	○	○	x (3)	○	○
1200	○	○	○	○	○	○	x (2)	○	○	○	○	○
1100	○	○	○	○	○	○	x (2)	○	○	○	○	○
1000	○	○	○	○	○	○	x (3)	○	○	○	○	○
900	○	○	○	○	○	○	○	○	○	○	○	○
800	○	○	○	○	○	○	○	○	○	○	○	○
700	○	○	○	○	○	○	○	○	○	○	○	○
600	○	○	○	○	○	○	○	○	○	○	○	○
500	○	○	○	○	○	○	○	○	○	○	○	○
400	○	○	○	○	○	○	○	○	○	○	○	○
300	○	○	○	○	○	○	○	○	○	○	○	○
200	○	○	○	○	○	○	○	○	○	○	○	○
100	○	○	○	○	○	○	○	○	○	○	○	○
Voltage / CPU Speed	1/1	1/2	1/8	1/1	1/2	1/8	1/1	1/2	1/8	1/1	1/2	1/8

Note:

Voltage: Noise value (Higher value shows higher anti-noise capability)

Polarity: Noise polarity added to target board power source

 CPU speed: Clock division ratio selection $f(xin)/1$, $f(xin)/2$ and $f(xin)/8$

○: Normal MCU operation

× (1): Reset cannot be released; × (2): Reset → restart → reset; × (3): Main loop error or runaway

5.3 Recommendations for improved PCB board

After modifications are made to the circuits on the non-recommended board, the results of anti-noise performance improves drastically but fell short of that of the recommended board. Given these result, it is recommended that in developing a product, the PCB should be redesign based on the recommended layout.

Note the following precautions for designing the PCB layout.

- Oscillator circuit wiring pattern: Use the shortest wiring pattern to connect oscillator, capacitor and MCU.
- Reset circuit wiring pattern: Place the reset circuit as close to the MCU as possible.
- CNVSS wiring pattern: Use a serial connection to connect a resistor to the CNVSS pin and the MCU VSS with the shortest wiring possible.
- Wiring pattern of VSS: Place the VSS wiring pattern of the oscillator, reset, and CNVSS circuits in the same VSS branch and separate them from other VSS wiring patterns.

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Revision Record

Rev.	Date	Description	
		Page	Summary
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