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April 1st, 2010
Renesas Electronics Corporation

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7542 Group

Key Scan

1. Abstract

The following article introduces and shows an example of how to use the Key Scan on the 7542 Group device.

2. Introduction

The application explained in this document applies to the following MCU and parameter(s):

Applicable MCU: 7542 Group

Oscillation frequency: 8 MHz

This sample program may include operations of unused bit functions for the convenience of the SFR bit layout. Set the values according to the operational conditions of the user system.

3. Contents

3.1 Key Scan

Outline:

- Key matrix of 4×4 is input.

Specifications:

- Scan output: P04 to P07
- Key input: P00 to P03
- “L” scan at every 2.5 ms
- Fixed key input: Fixed when matching three times
- When pressing two keys simultaneously, key input is disabled.

Figure 3.1 shows the Connection Diagram, Tables 3.1 and 3.2 show the Used RAM Definitions and Flag Definitions, Figure 3.2 shows the Relevant Register Settings, and Figure 3.3 and 3.4 show the Control Procedure.

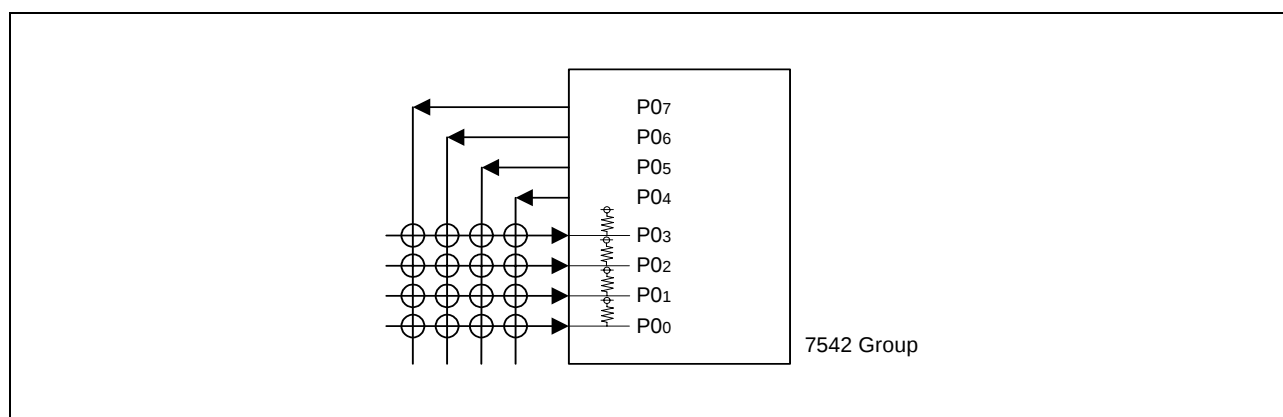


Figure 3.1 Connection Diagram

Table 3.1 Used RAM Definitions

Address (H)	Label Data Type	Initial Value	Size (Byte)	Description	Min (H)	Max (H)	Flag
0040	WORK	00H	1	Multipurpose buffer	00	FF	–
0041	WORK2	00H	1	Multipurpose buffer 2	00	16	–
0042	C_KEY	00H	1	Number of pressed keys	00	16	–
0043	KEY_SCAN_NOW	00H	4	Key input buffer	00	0F0F0F0F	–
0047	KEY_NO_BUF0	00H	1	Previous key input number	00	FF	–
0048	KEY_NO_BUF1	00H	1	Key input number before previous key input number	00	FF	–
0049	KEY_NO	00H	1	Fixed key input number	00	FF	–
004A	F_KEY	00H	1	Key flag	00	02	√

Table 3.2 Flag Definitions

Address(H)	004A	Label Data Type	F_KEY	File Name	FUNC_KEY2.A74
Bit Symbol	Bit Position	Initial Value	Contents	Bit Pattern	Meaning of Bit Pattern
F_KEY_OFF	b7 ☐ ☐ ☐ ☐ ☐ ☐ ☒ ☐ b0	0	Key input OFF flag	00000000B 00000010B	Key OFF Key ON

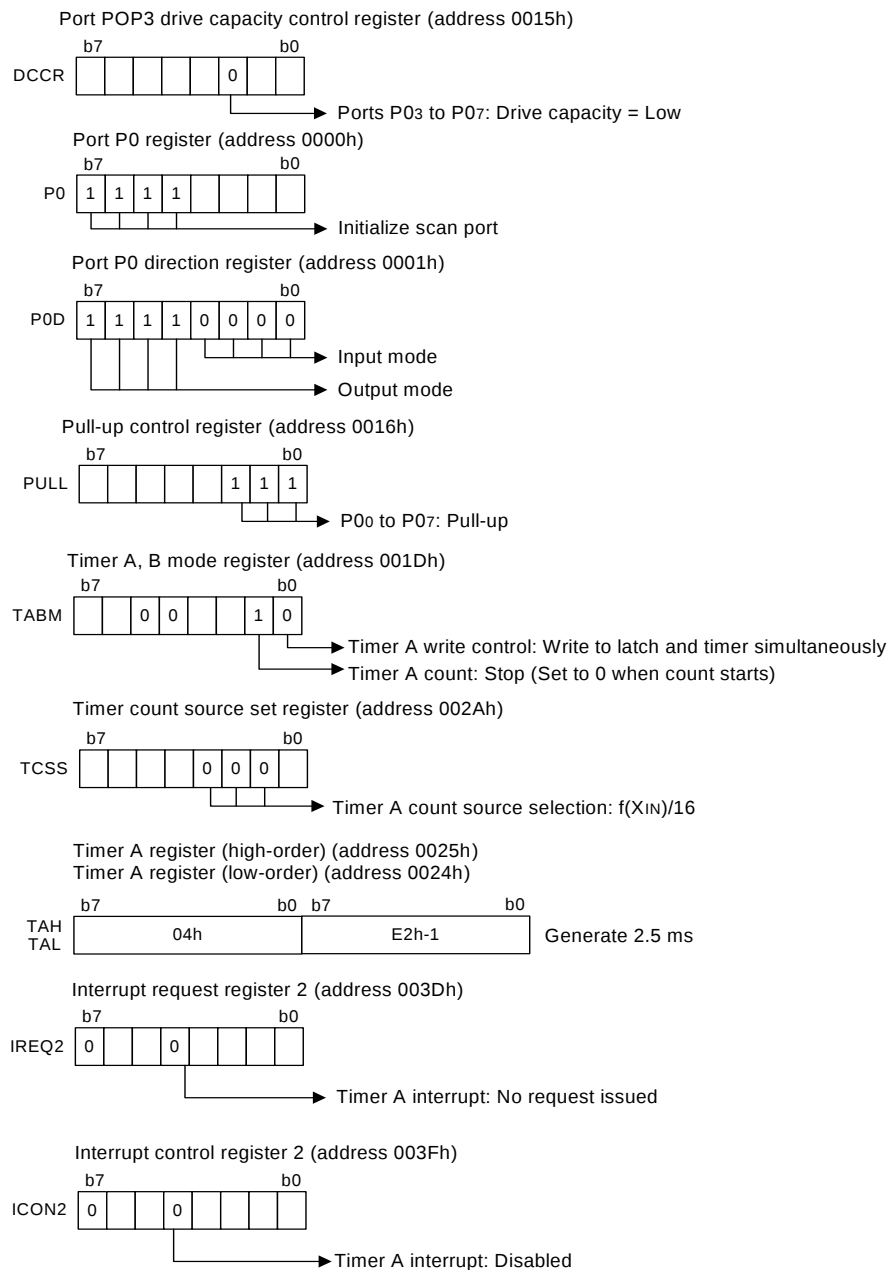
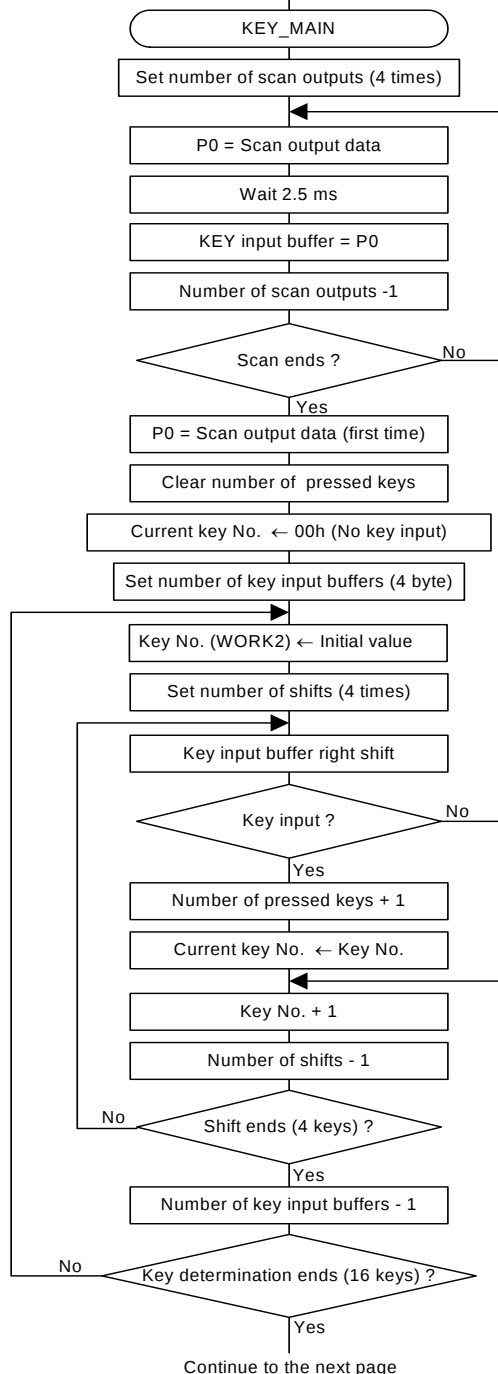


Figure 3.2 Relevant Register Settings

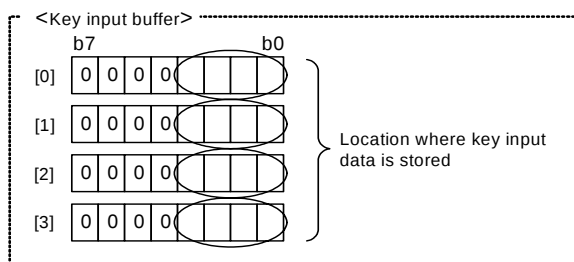
DCCR	(address 0015h), bit 2	← 0
P0	(address 0000h)	← 1111XXXXb
P0D	(address 0001h)	← 11110000b
PULL	(address 0016h)	← XXXXX111b
ICON2	(address 003Fh), bit 4	← 0
TABM	(address 001Dh)	← XX00XX10b
TCSS	(address 002Ah)	← XXX000XXb
TAL	(address 0024h)	← E2h-1
TAH	(address 0025h)	← 04h
IREQ2	(address 003Dh), bit 4	← 0
TABM	(address 001Dh), bit 1	← 0

- X: Not used in this application.
Set to 0 or 1 according to use.
- P04 to P07: Drive capacity = Low
- P00 to P03: Input mode
- P04 to P07: Output mode
- Pins P00 to P03: Pull-up
- Timer A interrupt disabled
- Set timer A write control, stop count
- Set timer A count source
- Generate 2.5 ms
- No timer 1 interrupt request issued
- Timer A count starts



- Scan output
P0 = 01110000b (first time)
P0 = 10110000b (second time)
P0 = 11010000b (third time)
P0 = 11100000b (fourth time)

- Mask data in output mode (P04 to P07), invert bits and store them in key input buffer (4 bytes) sequentially.



- Shift data of key input buffer to one bit right and determine number of pressed keys and their key numbers.
- Shift key input buffer to the right and determine in what number of bit data is set.

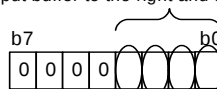


Figure 3.3 Control Procedure (1)

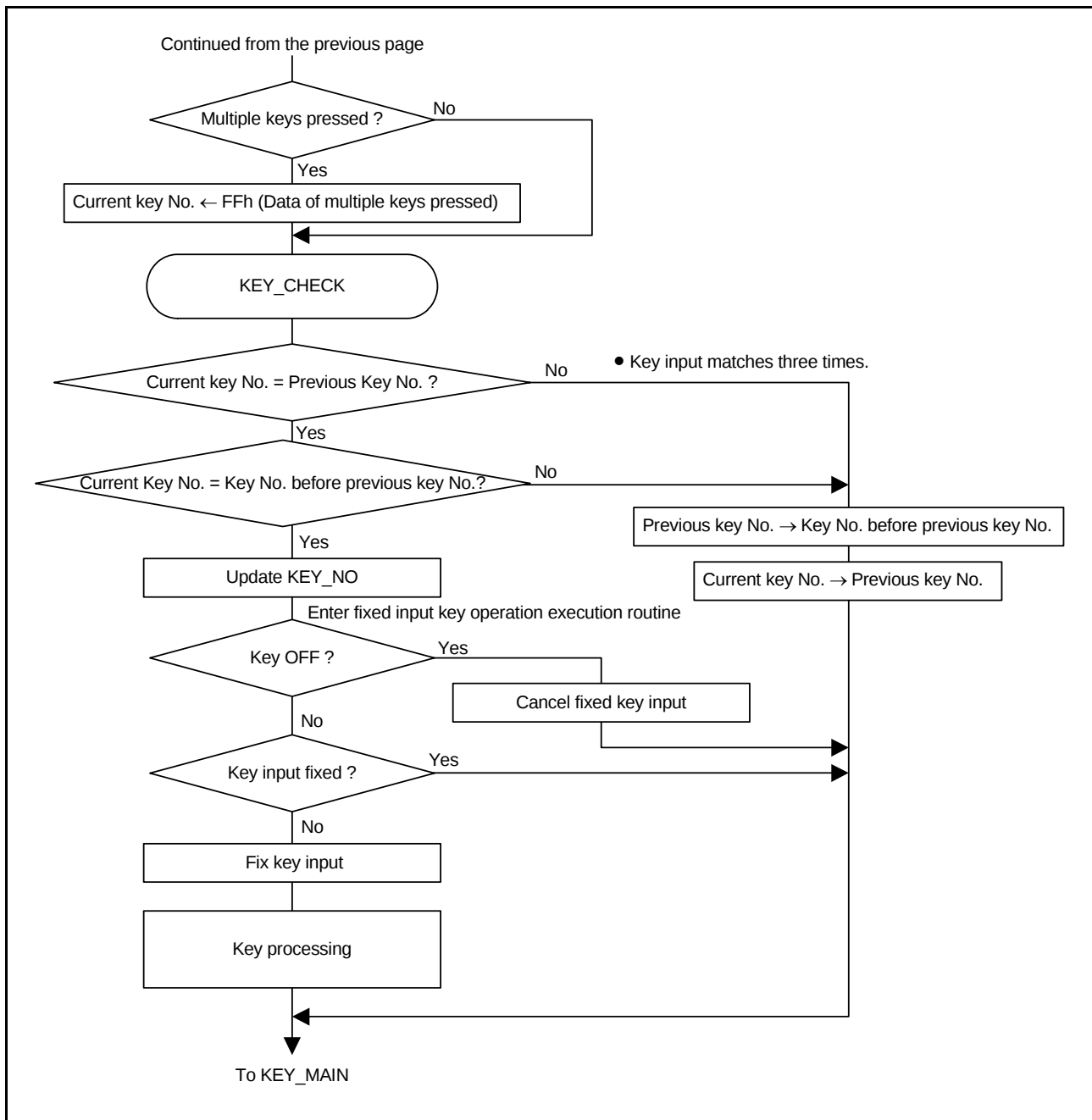


Figure 3.4 Control Procedure (2)

4. Sample Programming Code

Download a sample program from the Renesas Technology website.
To download, click "Application Notes" in the left side menu on the page of the 7542 Group.

5. Reference Document

Datasheet
7542 Group Datasheet
Download the latest version from the Renesas Technology website.

Technical News/Technical Update
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Website and Support

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REVISION HISTORY	7542 Group Key Scan
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 23 2007	–	First Edition issued

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