

## Introduction

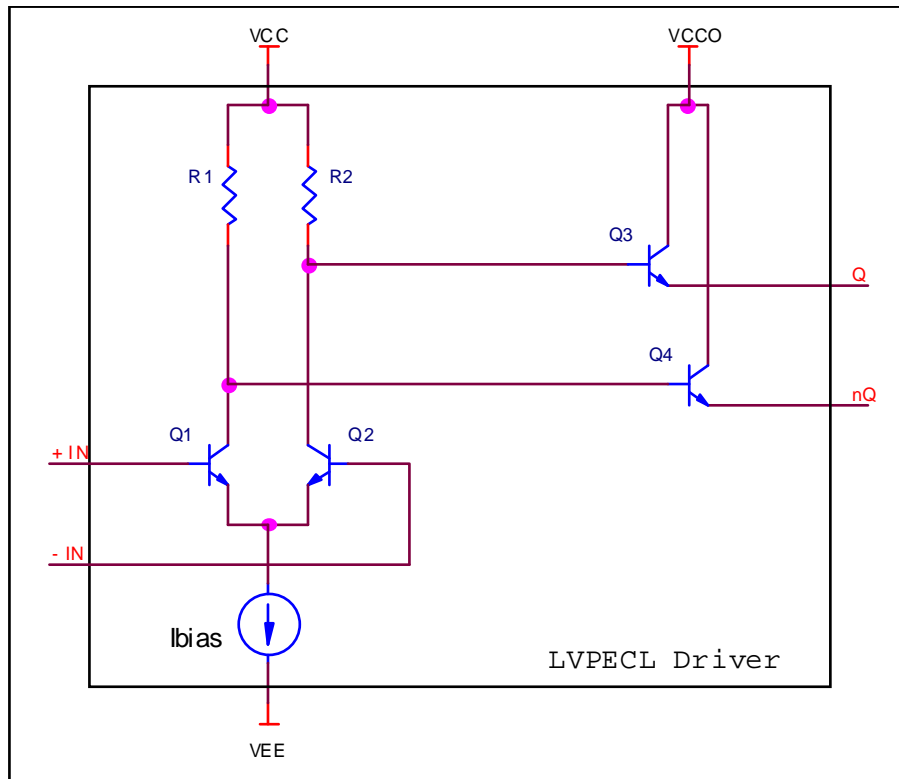
LVPECL is an established high frequency differential signaling standard that requires external passive components for proper operation. For DC coupled logic, these external components bias both the LVPECL driver into conduction and terminate the associated differential transmission line. However, the considerable circuit design flexibility available for achieving these two requirements can be a source of confusion for designers using LVPECL for the first time. They are often confronted with an array of termination options and no basis upon which to make a selection.

This note approaches the topology and selection of component values in a systematic manner, beginning with the structure of the output driver, and the standard VCC-2V bias and termination network. The characteristics and limitations of this termination are discussed in depth, and alternate T and PI terminations—which use fewer components, less power and are more flexible in pcb layout—are introduced and characterized. Additional related topics that frequently occur are also covered, including converting mixed 3.3 and 2.5V LVPECL with IDT PCIk and Clk receivers, proper utilization of clock receivers with internal terminations, LVPECL to LVDS conversion, attenuator design, and selection of bias and coupling capacitors for AC terminations.

## The LVPECL Driver

The LVPECL driver is typically implemented as an open emitter driver, as shown in Figure 1.

**Figure 1. Equivalent Schematic of an Open Emitter LVPECL Driver**



Three things can immediately be noted in [Figure 1](#):

- 1) The output transistors are not turned on; therefore the driver will not produce an output.
  - a. In order for Q and nQ to switch, each must be loaded with a DC path to ground.

- b. If the output is not to be used the Q and nQ pins can be floated to ensure the outputs are turned off, minimizing power and reducing noise.
- 2) The emitter currents of Q and nQ are determined by the selection of external pull down resistors. Different values for these resistors adjust for different VCCO voltages and trade power dissipation off against switching time and peak-peak signal swing.
- 3)  $V_{CCO} = V_{CC}$ ;  $V_{CCO}$  cannot be set independent of  $V_{CC}$  to accommodate clock receivers using different supply voltages. If  $V_{CCO} > V_{CC}$ , then the gate will consume excess power as the base-collector junction bias increases. If  $V_{CCO} < V_{CC}$ , the output transistors can saturate resulting in significant bandwidth loss.

Differential output LVPECL drivers are capable of operating at gigahertz frequencies, which requires that the associated LVPECL receivers are connected to the drivers through transmission lines. These transmission lines in turn require proper termination to preserve signal integrity. There are many different termination schemes for the LVPECL drivers; this application note covers the standard DC coupled terminations as well as biasing LVPECL drivers for AC coupling.

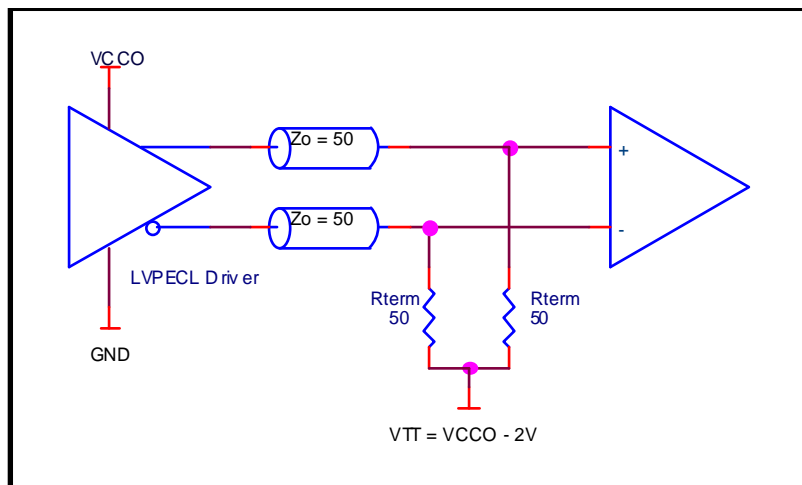
The following termination approaches are only general recommendations under ideal conditions. Board designers can select terminations based on ease of component placement and driver power vs. performance trade-offs, but should also verify signal integrity through simulations that include trace length, layer routing, and vias.

## DC Coupled LVPECL Terminations

### Standard Termination

The standard DC coupled LVPECL termination is shown below in [Figure 2](#). This termination scheme is used throughout the electronics industry for device characterization at  $V_{CCO} = 3.3V$  and  $2.5V$ . The three requirements for the standard termination are: 1) to provide the 50 ohm termination impedance for both the Q and nQ clock signals at the LVPECL receiver, 2) realize the  $V_{TT}$  termination voltage of  $V_{CCO} - 2.0V$  and 3) be DC coupled to both bias the output transistors and support data.

**Figure 2. Industry Standard LVPECL Termination**



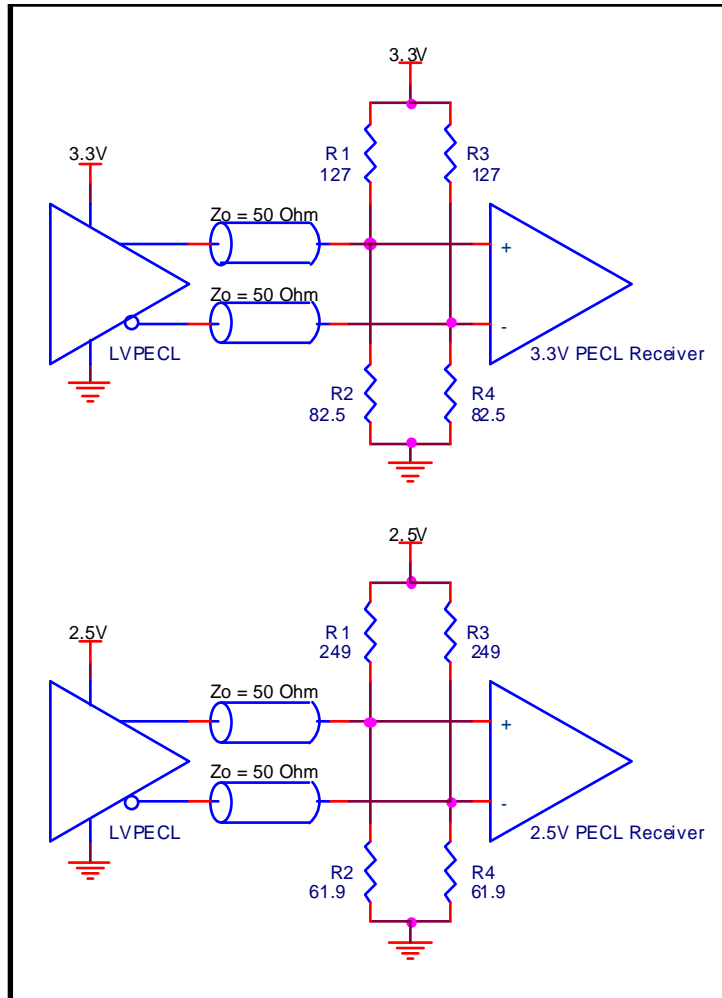
The definition of  $V_{TT}$ ,  $V_{CCO} - 2.0V$ , was determined originally with ECL, which was the precursor to PECL. The  $V_{TT}$  voltage was set by a tolerance analysis across temperature, device processing, supply voltage and resistance to ensure that the output transistors operate at a minimum 2mA emitter current. This requirement maintains the high speed switching property of ECL/LVPECL when loaded in 50 ohms.

The drawback of this termination scheme is that it requires an additional power supply  $V_{TT}$  where  $V_{TT} = 1.3V$  if  $V_{CCO} = 3.3V$ , or,  $0.5V$  if  $V_{CCO} = 2.5V$ .

## Thevenin Equivalent Termination

In practice, the VTT supply is most commonly eliminated with the terminations of Figure 3 below, where both the VTT voltage and the 50 ohm termination resistor are both simultaneously realized for the Q output as the Thevenin equivalent of the R1 and R2 bias string; similarly with R3 and R4 for the nQ output.

**Figure 3. 3.3V and 2.5V Thevenin Equivalent LVPECL Terminations**



Four resistors are used to implement the three LVPECL termination requirements; generating one VTT voltage and two 50 ohm termination impedances. This extra component can be taken advantage of in two ways:

- 1) To set the Q and nQ termination voltages differently, for example to  $VCC - 2.0V \pm 25mV$ . The 50 mV differential mismatch in the termination voltages will suppress oscillations in the clock receiver if the clock driver is not switching. This input offset does incur a duty cycle error that may be important, particularly for those applications that use both clock edges.
- 2) The Q and nQ transmission lines can be fully independent. This means that if the LVPECL outputs are not to be used as a differential pair, then the Q and nQ outputs can be routed completely independently. This allows for effectively a 1:2 fanout buffer, though with the nQ signal inversion. In this application the logic threshold reference embedded in the differential pair is either not required due to AC coupling, or is provided externally from a threshold voltage reference supply, typically designated as VBB. This advantage does however incur the penalty that the differential signal swing at the receiver is cut in half.

There are five disadvantages of the Thevenin termination:

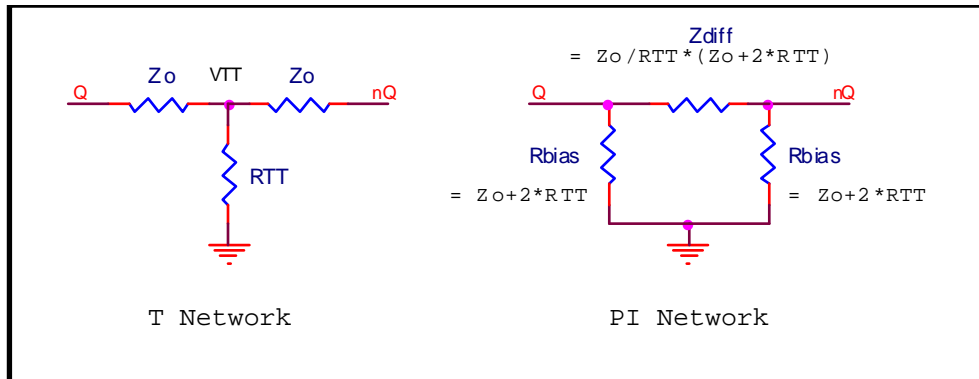
- 1) The bias string incurs its own power penalty in addition to the output driver emitter currents, about 80 mW per output pair on a 3.3V supply.
- 2) There is no remaining degree of freedom in the termination to accommodate variations in VCCO, temperature and device processing.
- 3) A fraction of the variations in VCCO are fed forward to the Thevenin equivalent VTT voltage by the bias voltage divider; 39% for VCCO=3.3V and 20% for VCCO=2.5V. Therefore control of the emitter currents, particularly for the logic low output, is not as effective as the standard VTT=VCC-2.0V termination.
- 4) For a differential termination, only three resistors are actually required to realize one VTT voltage and two 50 ohm termination impedances.
- 5) For each of the Q and nQ signals, the two resistors connected to the clock receiver terminal add layout complexity and a performance penalty due to additional parasitic capacity over a single resistor.

### T and PI Terminations

In the majority of applications, the two advantages of the Thevenin termination are not required and their five disadvantages are significant. In this case, the use of coupled transmission lines and the T (Tee) or PI resistor networks of [Figure 4](#) is preferred for three reasons:

- The standard VCCO-2.0V termination controls both VTT and therefore the output transistor emitter currents regardless of any variation in the VCCO voltage. The Thevenin termination can only do so at one VCCO voltage because any variation in the VCCO voltage is not translated directly; instead it is divided down by the bias string. Therefore since the Thevenin termination cannot control the emitter currents over VCCO variations, other networks that control these currents better are to be considered.
- The LVPECL receiver never directly senses VTT; the receiver senses the emitter follower output voltages directly. The VTT voltage is only a means to the end of controlling emitter currents—important because the emitter currents control the LVPECL output swing and switching speed.
- The output emitter currents are more tightly controlled with the T and PI networks because of the greater amount of negative feedback on the output transistor emitters. A detailed comparison of the T termination vs the Thevenin termination, particularly for control of output transistor currents and power reduction, is in the section [Appendix: Comparison of T and Thevenin LVPECL Terminations](#).

**Figure 4. T and PI LVPECL Termination Networks**



The T network allows for the LVPECL emitter currents and the differential impedance to be defined directly. This can be demonstrated by first setting  $Q=nQ$  and solving for the equivalent common mode resistance,  $R_{cm} = Z_o/2 + R_{TT}$ . Given the common mode voltage and the value of  $R_{cm}$ , the average emitter current for the LVPECL output transistors can be selected and the value of  $R_{TT}$  calculated for a given VCCO. Second, set  $Q = -nQ$  which immediately results in the differential impedance,  $R_{diff} = 2 * Z_o$ . With resistor values of the T network, resistor values for the PI network can be generated with the standard T-PI (Wye-Delta) transform, as is shown in [Figure 4](#).

As discussed in [Appendix: Comparison of T and Thevenin LVPECL Terminations](#), the actual bias currents depend on the specific device voltage tolerances and the variation in VCCO voltage. Three cases of VCCO voltage tolerance and processing tolerance based on the IDT ICS853S006i are shown in [Table 1](#) below; nominal processing and voltage, nominal processing and -5% VCCO and both processing tolerance and -5% VCCO.

The most important factor to be considered is the emitter current of the logic 0 transistor because the fastest switching speed occurs when the output transistors conducts current at the logic 0 state. The table shows resistor selection options for the logic 0 bias current and the average bias current of an LVPECL output pair with the associated values of Rbias, Zdiff and RTT. For the Vcc = 2.5V case, maintaining the emitter bias current greater than zero on -5% Vcc requires that Ibias to be 17mA at nominal Vcc. This is an indication of why LVPECL is limited to 2.5V.

**Table 1: Output Transistor Bias Current vs Bias Resistors for T and PI Terminations**

Case	Vcco	VOUT_h	VOUT_l	Ibias min (mA)	Avg Ibias (mA)	RTT	Rbias	Zdiff
Nominal	3.3	2.35	1.65	2	10.9	87	220	130
-5% VCCO	3.164	2.21	1.51	2	11.1	75	200	130
-5% VCCO, worst case processing, -40 to +85 deg	3.164	2.07	1.29	1	11.6	68	187	137
Nominal	2.5	1.55	0.85	2	12.7	43	130	160
-5% VCCO	2.375	1.43	0.73	2	13.3	36	120	174
-5% VCCO, worst case processing, -40 to +85 deg	2.375	1.29	0.50	1	15.8	24	100	200

## Applications of T Terminations

In exactly the same manner, consider the equivalent T network placed at the output of the LVPECL gate.  $Z_{diff}$ , which is composed of the series combination of two  $Z_o$  resistors with the  $R_{TT}$  center tap resistor, is pushed to the clock receiver. For the T network though the  $R_{TT}$  resistor must also go with the  $Z_o$  resistors; no component remains at the clock driver. The common mode voltage across  $R_{TT}$  is  $V_{TT}$ , where  $V_{TT}$  is practically the same as  $V_{TT} = V_{CC} - 2.0V$ ; hence the reason for selecting the name  $R_{TT}$ . Further the parasitic capacity associated with  $R_{TT}$  does not affect differential mode signal integrity for the same reason; it is located at an AC virtual ground at the  $V_{TT}$  potential.

Examples of the T network depending on whether or not the 50 ohm termination resistors are integrated into the LVPECL receiver are shown below in [Figure 5](#) and [Figure 6](#).

**Figure 5. 3.3V and 2.5V External T Terminations**

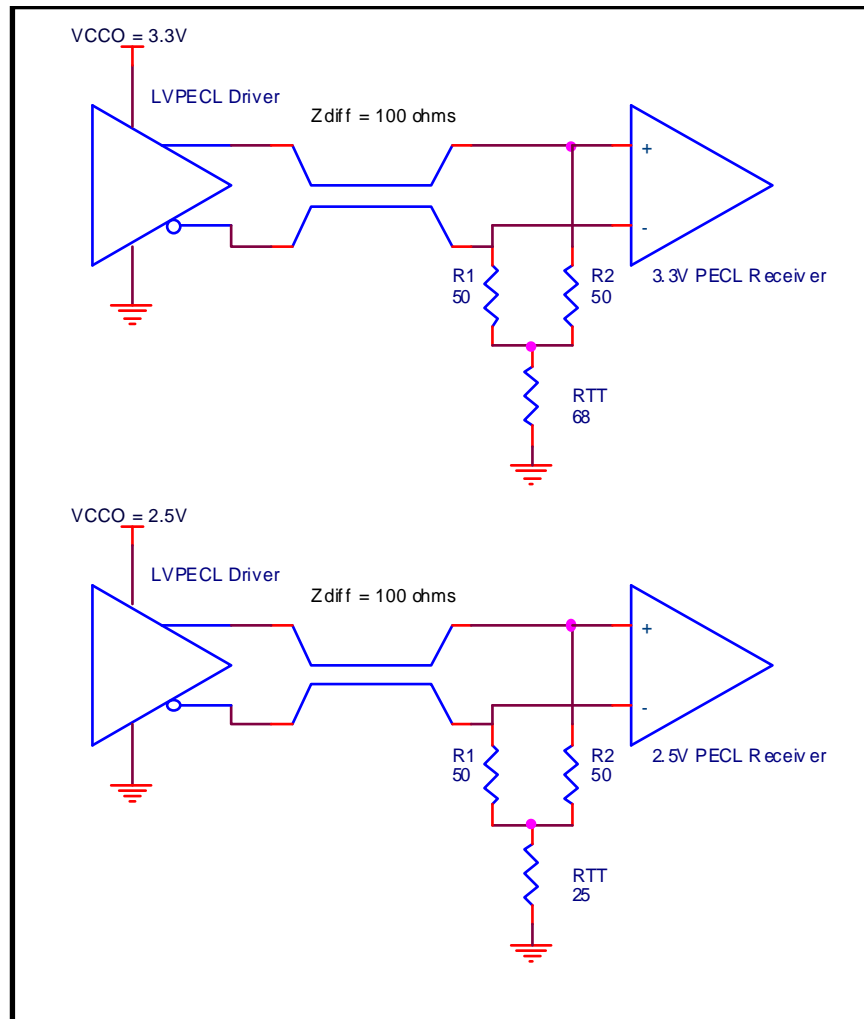
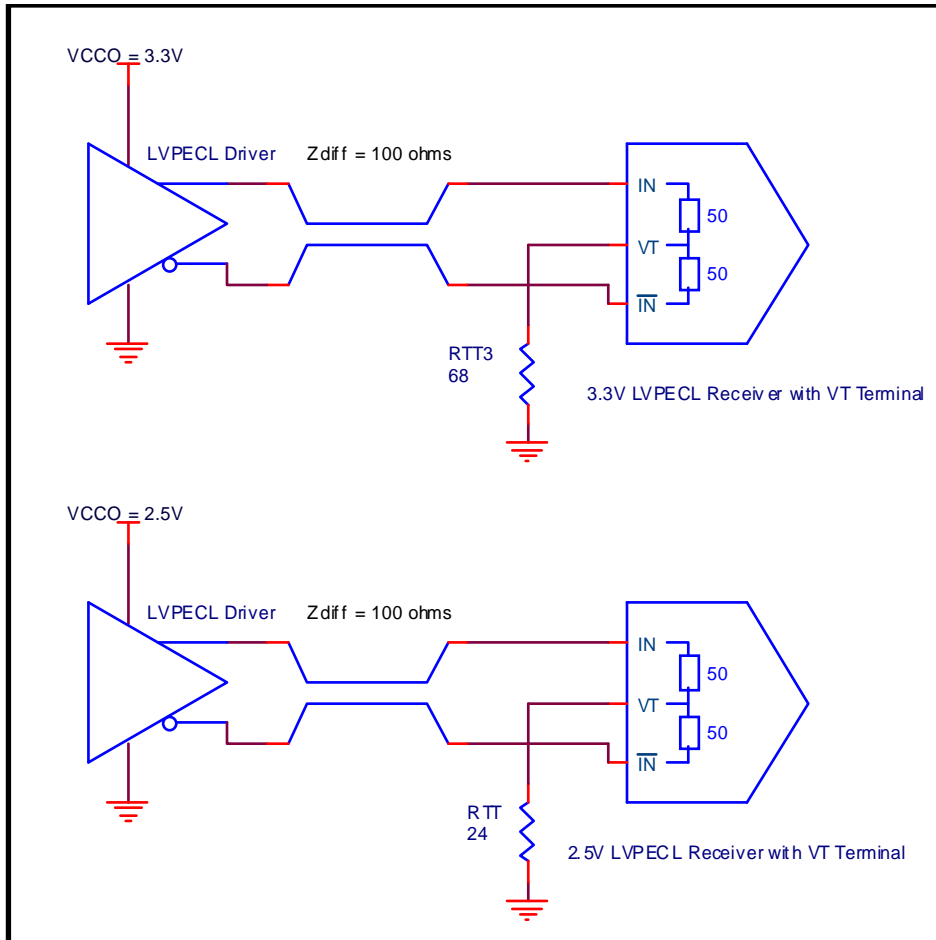


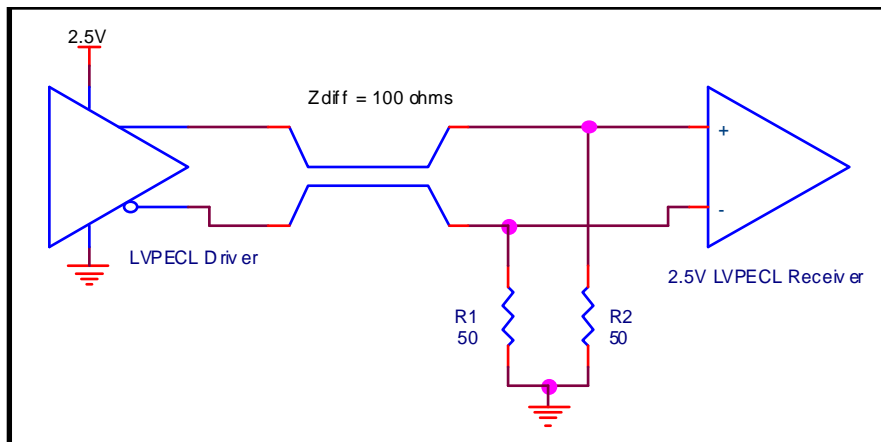
Figure 6. 3.3V and 2.5V T Terminations for Receivers with a VT Terminal



**Direct 2.5 V Termination**

In [Figure 7](#) below, the direct 2.5V termination is a simplification of the 2.5V T termination in which RTT has been set to zero. This simplification comes at the expense of higher power dissipation in the driver.

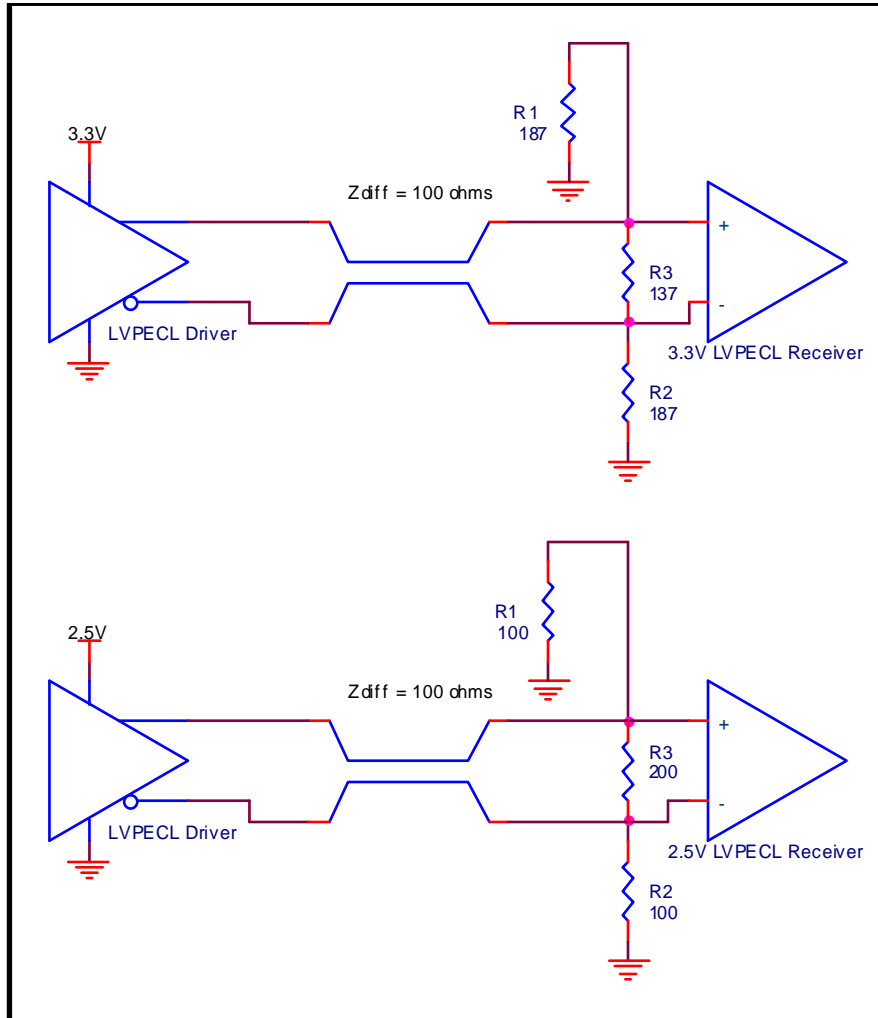
Figure 7. Direct 2.5V LVPECL Termination



## Applications of PI Terminations

Specific forms of the PI network are shown below in Figure 8. Note that the shunt resistors R3 are greater than 100 ohms. Unlike the T termination, this precludes use of the PI termination with receivers with built-in 100 ohm shunt terminations.

**Figure 8. Figure 8 - 3.3V and 2.5V External PI Terminations**



## LVDS-Like Termination

The standard T and PI terminations realize a differential impedance of 100 ohms to terminate a coupled pair of transmission lines where part of the differential impedance is the Rbias resistors. In the LVDS-like network, the Rbias resistors are placed at the LVPECL driver instead of at the receiver. In this configuration the Rbias resistors no longer are part of the load termination and their influence on the output impedance of the output driver is minimal as they are in parallel with the low output impedance output transistor. Therefore Rbias values are selected so that they can sink the full  $Z_{diff}$  termination current without cutting off the logic 0 transistor. Consequently the Rbias values must be reduced relative to the PI termination. This requires recalculating the Rbias resistors, summarized in [Table 2](#) below.



**Table 2: Output Transistor Bias Current vs Bias Resistors for LVDS-like termination**

Case	Vcco	VOUT_h	VOUT_l	Ibias min (mA)	Avg Ibias (mA)	Rbias	Zdiff
Nominal	3.3	2.35	1.65	2	10.9	180	100
-5% VCCO	3.164	2.21	1.51	2	11.1	162	100
-5% VCCO, worst case processing, -40 to +85 deg	3.164	2.07	1.29	1	11.6	140	100
Nominal	2.5	1.55	0.85	2	12.7	91	100
-5% VCCO	2.375	1.43	0.73	2	13.3	82	100
-5% VCCO, worst case processing, -40 to +85 deg	2.375	1.29	0.50	1	15.8	56	100

**Applications of LVDS-Like Terminations**

The LVDS-like termination can be used with clock receivers with or without internal shunt 100 ohm terminations as shown in [Figure 9](#) and [Figure 10](#).

**Figure 9. 3.3V and 2.5V LVDS-Like Terminations for Receivers without a VT Terminal**

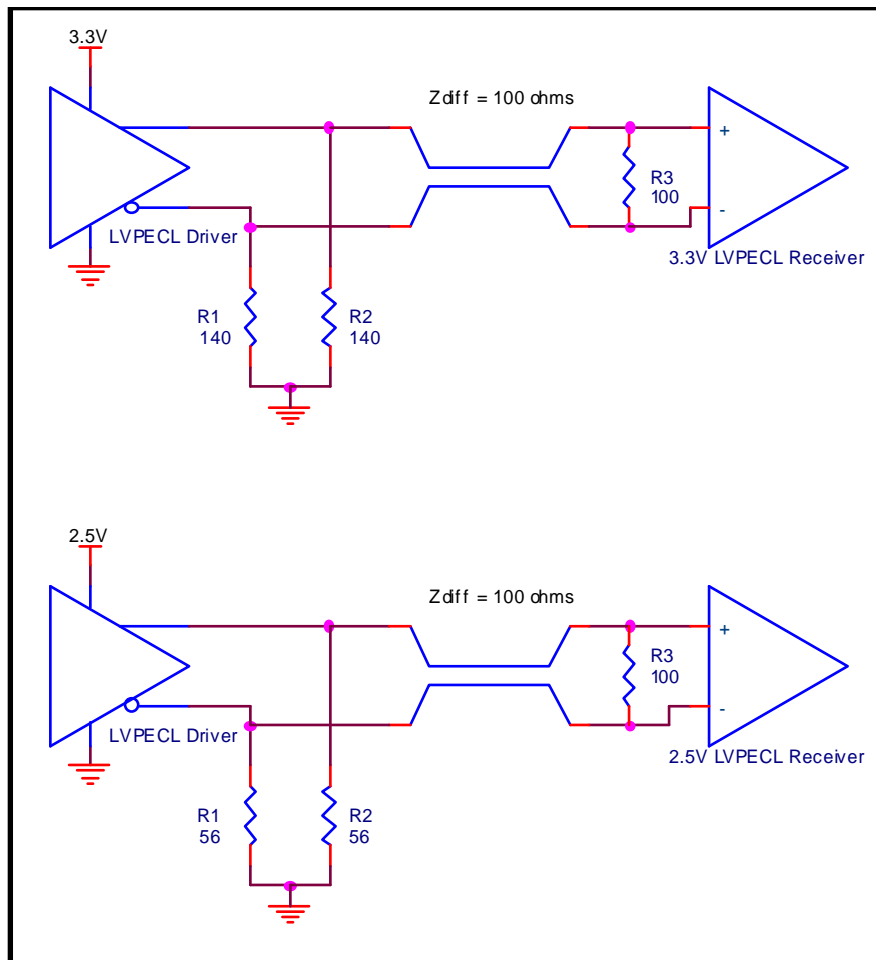
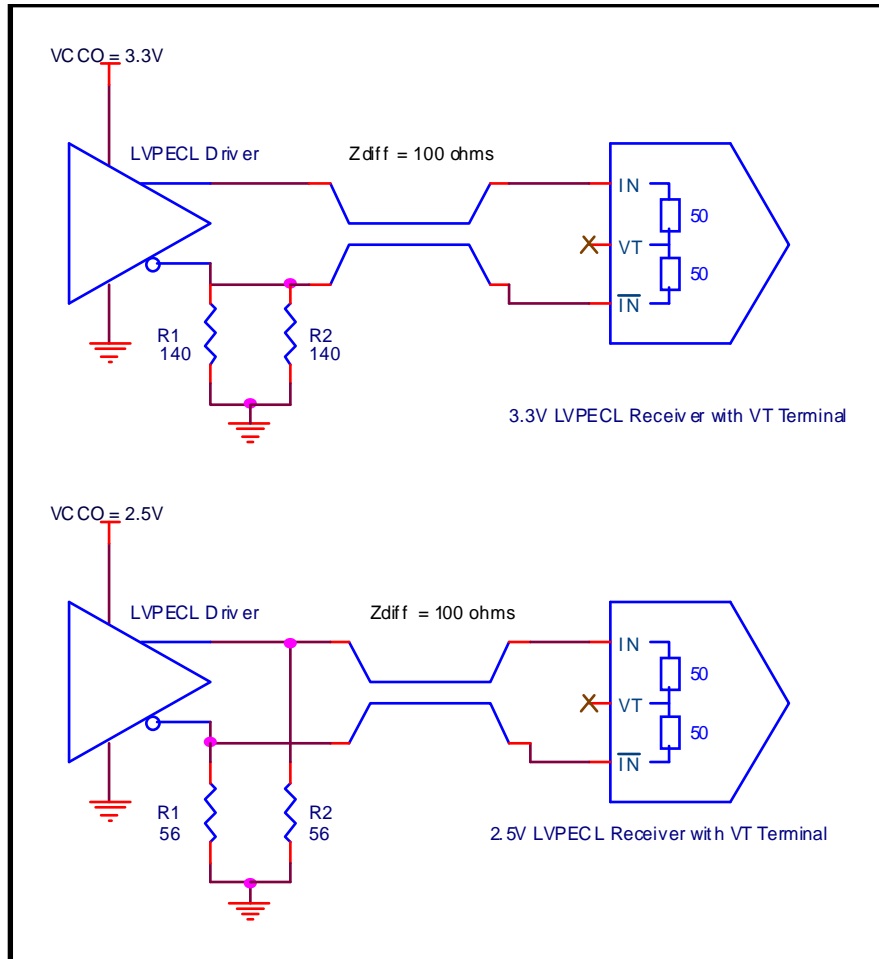


Figure 10. 3.3V and 2.5V LVDS-Like Terminations for Receivers with a VT Terminal



### Layout for PI, T and LVDS-like Terminations

The T and PI terminations are easier to layout than the four resistor Thevenin equivalent termination as there are only three resistors and no VCC connections necessary. The PI termination is easier to layout than the T because the two Rbias resistors are located on either side of the differential transmission line instead of between them, as is the case of RTT. On the other hand, the T termination only places one resistor parasitic capacity on each transmission line terminus. These terminations are preferred with large fan out LVPECL devices, for example a 1:22 fan out buffer. In this case no resistors have to be placed at the driver itself.

The LVDS-like termination splits the termination network between the LVPECL driver and receiver which is clearly most advantageous when terminating multiple LVPECL signals on a single package, such as a BGA; leaving two resistors at the LVPECL driver for each LVPECL pair reduces the layout complexity at the receiving ports. The Q and nQ outputs still have the Rbias resistors, but there is only one resistor per transmission line. This makes it easy to place the bias resistors on the same side of the PCB as the LVPECL driver, which is a significant signal integrity advantage. The extra parasitic associated with Rbias over and above that of the transmission line inputs is not a significant problem; these parasitics are driven directly by the low impedance emitter follower outputs.

In some cases it may be difficult to fit all the pull down bias resistors of the LVDS-like termination at the clock driver. Another option is to alternate PI or T terminations with LVDS-like to balance layout congestion between the driver and the various clock receivers.

The designer must also be mindful of the fact that microstrip and stripline transmission lines laid out in multilayer boards do not provide the shielding of coax. For long runs of low jitter clocks it is highly recommended to avoid routing other signals in such a

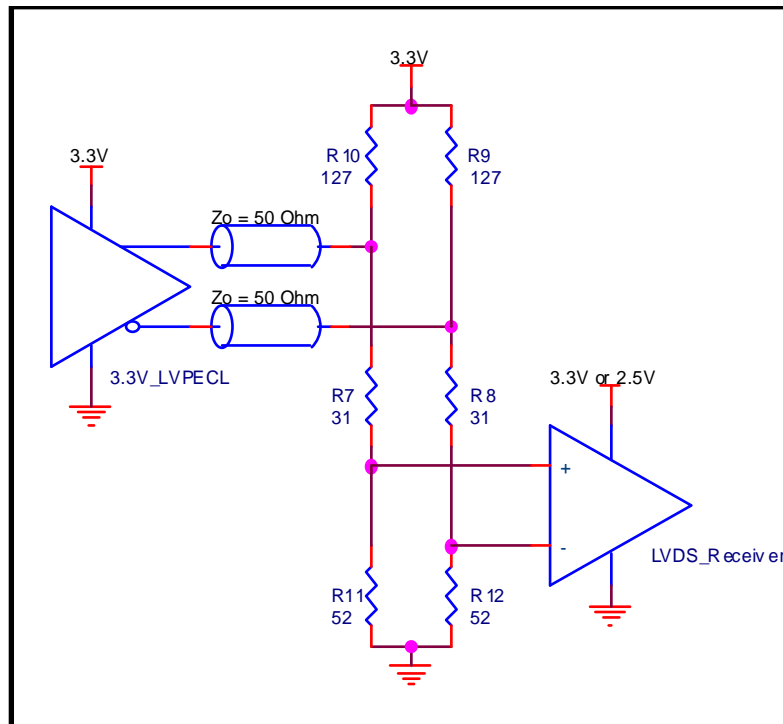
manner as to cross couple into the clock lines. For example, it is not recommended to rely on the common mode rejection of differential routing when routing sub-picosecond jitter clocks and route other high frequency signals either parallel to or crossing over clock lines. A second significant source of jitter is internal transmission line discontinuities introduced by vias used to change layers. These vias create reflected waves within the transmission line in addition to those caused by mis-termination at the clock receiver and by deviations of the nominal transmission line impedance through PCB manufacturing tolerances.

### 3.3V LVPECL to LVDS DC Termination

It is possible to retain DC coupling and both level translate and attenuate the LVPECL signal to be compatible with LVDS receivers. The only caveat is that the LVDS receiver be capable of accepting the variations in the LVPECL signal swing and common mode voltage. A circuit that will nominally translate and attenuate a 3.3V LVPECL signal to LVDS while presenting a 50 ohm termination to the LVPECL driver is shown in Figure 11 below.

The termination is a minor change to the 3.3V LVPECL termination of Figure 3. The exact values are calculated from assuming a particular LVPECL driver, the 853S006, whose nominal common mode output driver voltage is 1.96V. This voltage is translated to the 1.2V common mode LVDS level by the divider. This divider also reduces the LVPECL swing, but the reduction factor is the same as that of the common mode translation. Applying this translation factor to the maximum 1V peak-peak swing of LVPECL, the maximum swing at the LVDS receiver is  $1V * 52/83 = 626mV$  peak-peak. This is to be compared to the maximum LVDS single ended swing of 450 mV peak-peak. For LVPECL drivers with different common mode voltages, these values can be adjusted accordingly.

Figure 11. 3.3V LVPECL to LVDS Translation and Termination



### 3.3V LVPECL and 2.5V LVPECL Inter-conversion with IDT Clk and PClk Receivers

IDT Clk/nClk PClk receivers utilize an N type input differential amplifier and the PClk/nPCLk receivers use P type input transistors. The common mode range of N channel inputs includes ground but not VCC; conversely PClk inputs common mode range includes VCC but not ground. These properties allow for VCC translation with standard DC coupled LVPECL terminations as shown below.

Figure 12 translates between a 3.3V LVPECL output and a 2.5V LVPECL receiver. The 3.3V to 2.5V conversion is permissible even in the extreme corner case of +5% 3.3V supply for the driver, -5% supply of the receiver and maximum 1V peak-peak swing for the driver because the PClk inputs can be driven as much as 0.3V above VCC=2.5V.

Figure 12. 3.3V LVPECL to 2.5V LVPECL Conversion

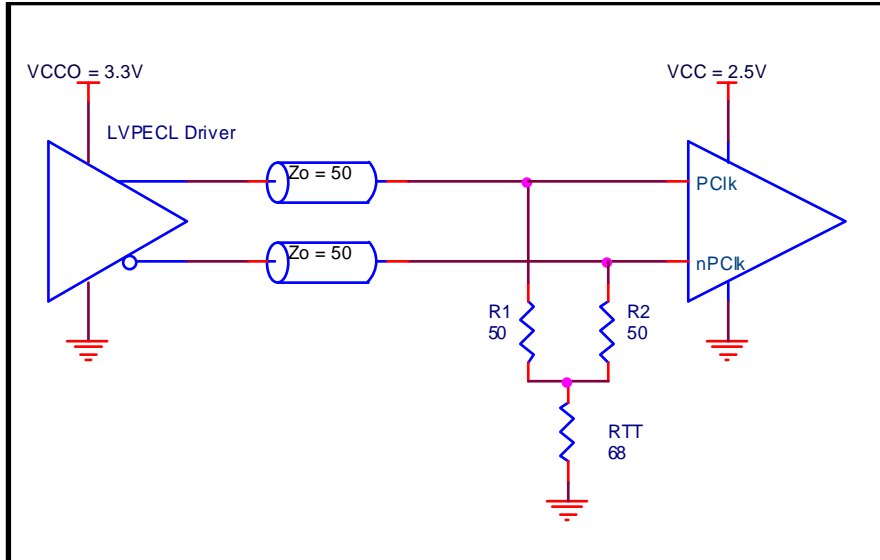
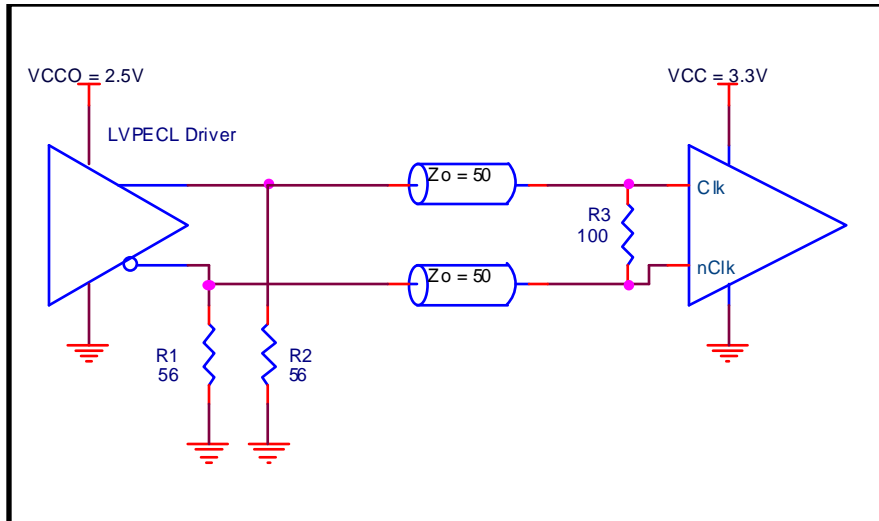


Figure 13 shows the straight forward case of using the extended common mode input range of the IDT Clk/nClk receiver when powered from 3.3V, which includes ground. The 2.5V LVPECL signal swing is fully contained within the common mode range of the Clk/nClk receiver.

Figure 13. 2.5V LVPECL to 3.3V LVPECL Conversion



### Summary of DC Termination Characteristics

For the majority of applications in which a voltage offset at the receiver to suppress receiver oscillation is not necessary and the LVPECL outputs will be received as differential pairs, the various terminations of Figure 5, Figure 8 and Figure 9 are preferred to the Thevenin termination on the basis of better output current control over variations in VCCO and device processing variations, lower power consumption both when active and when powered down, as well as layout simplicity. For a more detailed analysis of these two terminations that justifies this preference, refer to the section [Appendix: Comparison of T and Thevenin LVPECL Terminations](#), which compares the Thevenin termination to the T termination in much greater detail.

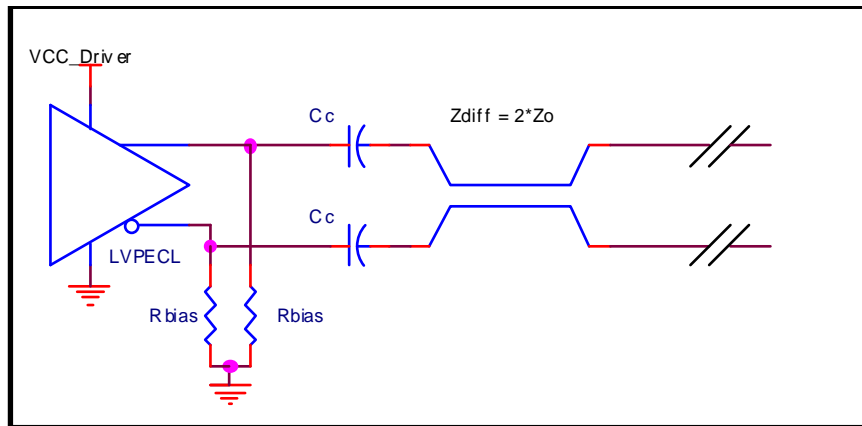
The reader should also keep in mind the trade-off between LVPECL driver current and switching time performance, which is due to the fact that LVPECL outputs operate in voltage mode. This option is not available in other signaling families that operate the driver in current mode, such as standard HSCL, LVDS and CML.

If in an application there are LVPECL drivers that may not require switching time performance to support very high clock or data rates, then the bias resistors can be increased in accordance with [Table 1 Output Transistor Bias Current vs Bias Resistors for T and PI Terminations](#). This may be very useful in high fan out drivers for example. If the emitter current is increased, the driver power dissipation is increased, signal swing is increased and switching time is reduced.

### LVPECL Bias for AC Coupled Terminations

Very often LVPECL clock drivers must be AC coupled to a receiver of a different logic family with a different switching threshold voltage. In this case, the functions of DC biasing the driver and providing termination impedance are separated. The LVPECL output must still be DC biased but the use of blocking capacitors requires that a bias to set the voltage at the receiver inputs within the receiver common mode range and the transmission line termination impedance are to be provided at the receiver. The external components are shown in [Figure 14](#).

**Figure 14. LVPECL Driver Bias for AC Coupled Loads**



Therefore for the driver, the only design task is to determine the pull down resistors necessary to ensure that the LVPECL output emitter followers are biased. Use the Rbias resistor values of [Table 2](#); these values were calculated based on setting the output transistor emitter current at the switching threshold. The value of Cc is calculated based on the frequency of the clock and the magnitude of the impedance at the clock frequency.

Coupling capacitor Cc selection is based on the amount of parasitic reactance that the cap is allowed to introduce into the signal path. If this maximum impedance is arbitrarily set at less than or equal to 0.2 ohms, then [Table 3](#) can be drawn up to associate standard cap values and their corresponding frequency ranges. If 0.2 ohms is viewed as excessively conservative for the application, this table can be scaled accordingly. Further a larger cap can be used for a given frequency range to minimize the total number of cap values in the Bill of Materials.

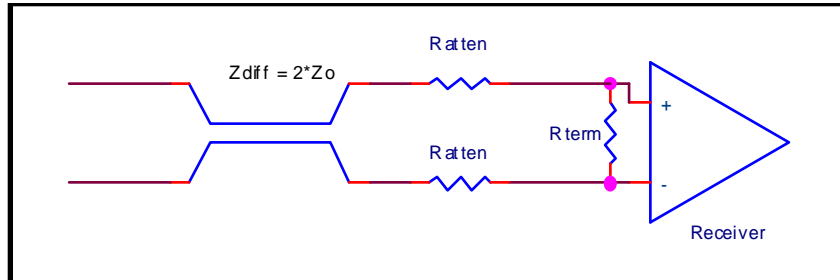
**Table 3: Standard Coupling Cap values vs Frequency**

Clock Freq Range (MHz)		Cc (pF)	Clock Freq Range (MHz)		Cc (nF)	Clock Freq Range (MHz)		Cc (µF)
Min	Max		Min	Max		Min	Max	
3700	5400	220	370	600	2.2	38	54	0.022
2500	3700	330	250	370	3.3	26	38	0.033
1700	2500	470	170	250	4.7	18	26	0.047
1200	1700	680	120	170	6.8	12	18	0.068
800	1200	1000	80	120	10	8	12	0.10

## Attenuator Pad Design

Occasionally it is necessary to attenuate the LVPECL swing to accommodate receivers that require an input swing smaller than the LVPECL swing. General design practices suggest placing the attenuator at the receiver, especially if a low jitter clock is to be routed a distance in an electrically noisy environment.

**Figure 15. Simple Receiver Attenuator**



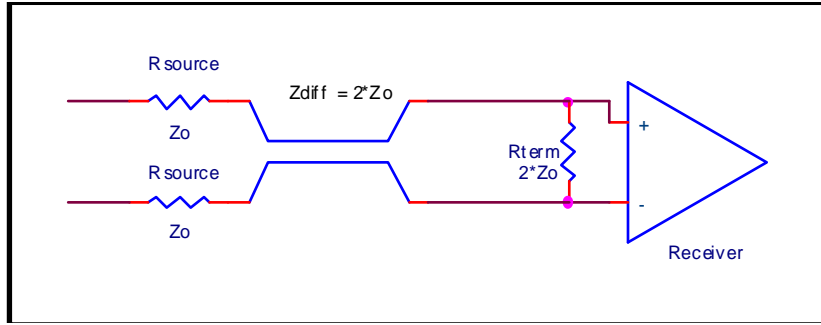
The example of [Figure 15](#) illustrates the approach for the simplest attenuator. If the receiver incorporates a  $2 \cdot Z_o$  shunt termination, then the value of the external  $R_{term}$  resistor can be increased to achieve the correct total shunt resistance across the terminals of the receiver. A range of attenuations realized with standard resistor values are shown in [Table 4](#) below.

**Table 4: Receiver Attenuators for 50 ohm Transmission Lines**

Attenuation (dB)	$R_{atten}$	$R_{term}$	$Z_o$ Realized
-0.9	4.7	88.7	49.1
-1.5	8.2	84.5	50.5
-2.1	10.5	78.7	49.9
-2.5	12.7	75	50.2
-3.1	14.7	69.8	49.6
-3.5	16.5	66.5	49.8
-3.9	18.2	63.4	49.9
-4.4	20.0	60.4	50.2
-5.0	22.1	56.2	50.2
-5.6	23.7	52.3	49.9
-6.0	24.9	49.9	49.9

If layout considerations at the receiver force the attenuator to be placed at the driver, the low impedance of the LVPECL output driver allows for 6 dB or less of attenuation by placing series resistors equal to  $Z_o$  ohms or less at the LVPECL driver pins. Adding this resistor will actually improve signal integrity because adding source resistance up to 50 ohms is approaching the ideal of both source and load termination of the transmission line. [Figure 16](#) below shows an example of a 6dB attenuator implemented at the LVPECL driver, where it is assumed that the driver is biased for an LVDS-like network, that is with pull down resistors to ground directly on the LVPECL outputs.

Figure 16. 6db Attenuator



### Appendix: Comparison of T and Thevenin LVPECL Terminations

This appendix compares the relative performance of the LVPECL terminations of Figure 3 and Figure 5 under device and VCCO variations using the following three criteria.

- 1) VTT Stability vs VCCO
- 2) Q and nQ current
- 3) Power consumption

The conclusion is that the three resistor T termination of Figure 5 is preferred over the four resistor Thevenin termination of Figure 3. The same stability advantages of the T termination occur with the PI can be seen with a similar calculation. It will be seen that the T termination provides better operating point stability for the Q and nQ transistors than the Thevenin termination because the common mode RTT resistor of the T termination provides more feedback on the operating points of the Q and nQ transistors.

To demonstrate the performance of each of these terminations to the three comparison criteria, we select the 853S006 as a representative LVPECL output device for VOH and VOL variation. The Table 4B excerpt below is from the NOVEMBER 15, 2011 data sheet.

Figure 17. ICS853S006i LVPECL DEC Characteristics

ICS853S006i Data Sheet

LOW SKEW, 1-T0-6, DIFFERENTIAL-TO-2.5V, 3.3V LVPECL/ECL FANOUT BUFFER

Table 4B. LVPECL DC Characteristics, VCC = 3.3V; VEE = 0V, TA = -40°C to 85°C

Symbol	Parameter	-40°C			25°C			85°C			Units
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
VOH	Output High Voltage; NOTE 1	2.18	2.37	2.41	2.21	2.35	2.42	2.24	2.34	2.41	V
VOL	Output Low Voltage; NOTE 1	1.405	1.56	1.68	1.425	1.55	1.65	1.44	1.55	1.65	V
VSWING	Peak-to-Peak Output Voltage Swing	625	800	870	690	800	870	730	800	852	mV

NOTE: Input and output parameters vary 1:1 with VCC.  
 NOTE 1: Outputs terminated with 50Ω to VCCO - 2V.

It does not matter for the purposes of comparing termination networks that the max and min values of VOH and VOL do not occur in one specific device but rather across the population of devices in the characterization sample. The focus is on the bias stability of these two terminations so it is only necessary to use this table to calculate a plausible set of variations of VOH and VOL from the 853S006 LVPECL output driver to stand in for all LVPECL drivers.

The min and max values of VOH and VOL were calculated from the p-p swing and the common mode output voltage. The values of VOH and VOL across all temperatures are used directly and the values of VPP (VSWING) were calculated only for comparison to the data sheet table.

Lastly since the LVPECL swing is  $V_{CC}=V_{CCO}$  referenced, the data of data sheet Table 4B is to be shifted 1:1 by the change in  $V_{CC}$  from 3.3V. Using these assumptions the following two tables are calculated to demonstrate the relative stability of the Q and nQ driver currents and the total power consumed for  $\pm 5\%$  change in  $V_{CC}$ .

**Table 5: Thevenin and T LVPECL Termination;  $V_{CCO} = 3.465V$ ,  $R_{TT} = 77$**

	Thevenin Termination			T Termination		
	Min	Typ	Max	Min	Typ	Max
$V_{OH}$ $V_{OL}$	2.21 1.43	2.35 1.55	2.42 1.65	2.21 1.65	2.35 1.55	2.42 1.65
$V_{PP}$ $V_{CM}$	0.79 1.82	0.80 1.95	0.77 2.04	0.63 1.82	0.80 1.95	0.87 2.04
$V_{TT}$ $V_{CCO}-V_{TT}$	1.30 2.00	1.30 2.00	1.30 2.00	1.37 1.93	1.47 1.83	1.54 1.76
$I_{OH}$ $I_{OL}$	18.04 2.40	20.83 4.90	22.23 6.89	16.76 1.06	17.56 1.56	17.68 2.28
$I_{bias} = (I_{oh}+I_{ol})/2$	10.22	12.86	14.56	8.91	9.56	9.98
Power (mW)						
Q and nQ	67.5	84.9	96.1	58.8	63.1	65.8
Termination Network	103.7	103.7	103.7	0.0	0.0	0.0
<b>Total</b>	171.2	188.6	199.8	58.8	63.1	65.8

**Table 6: Thevenin and T LVPECL Termination;  $V_{CCO} = 3.135V$ ,  $R_{TT} = 77$**

	Thevenin Termination			T Termination		
	Min	Typ	Max	Min	Typ	Max
$V_{OH}$ $V_{OL}$	2.05 1.26	2.19 1.39	2.26 1.49	2.05 1.26	2.19 1.39	2.26 1.49
$V_{PP}$ $V_{CM}$	0.79 1.65	0.80 1.79	0.77 1.87	0.79 1.65	0.80 1.79	0.77 1.87
$V_{TT}$ $V_{CCO}-V_{TT}$	1.24 1.90	1.24 1.90	1.24 1.90	1.25 1.89	1.35 1.79	1.41 1.72
$I_{OH}$ $I_{OL}$	16.06 0.42	18.84 2.91	20.24 4.90	15.95 0.25	16.75 0.75	16.87 1.47
$I_{bias} = (I_{oh}+I_{ol})/2$	8.24	10.88	12.57	8.10	8.75	9.17
Power (mW)						
Q and nQ	51.6	68.2	78.8	50.8	54.9	57.5
Termination Network	93.6	93.6	93.6	0.0	0.0	0.0
<b>Total</b>	145.2	161.8	172.4	50.8	54.9	57.5

The following observations should be made for each of the first three items of the comparison list:

- 1) Both terminations do not implement the standard  $V_{CC} - 2.0V$  LVPECL termination voltage over temperature and supply voltage variation, which in these two cases are 1.3V and 1.135V.



- a) The VTT voltage for the T termination ranges from 1.54V to 1.25V, compared to the Thevenin termination VTT range of 1.3V and 1.24V.
  - b) The Thevenin termination VTT voltage does track the ideal VCC-2.0V VTT more closely than that of the T termination, but the 105mV difference across the 50 ohm equivalent load impedance causes the VCC = 3.135V IOL low currents to drop by more than 2mA relative to the VCC = 3.3V IOL low currents. This is because VTT is formed by a voltage divider so that VTT does not drop one for one with VCC.
- 2) Comparing the Thevenin termination and the T termination for typical VOH and VOL over temperature and processing, the bias current (IOH+IOL)/2, of the T termination exhibits far less variation.
    - a) The emitter currents of the output transistor pair are stabilized by the increased negative feedback applied at the output transistor emitters through RTT and the 50 ohm termination resistors.
    - b) The greatest variation for either termination occurs when VCCO is 3.3135 V since then the variation in the VOH and VOL are greatest in proportion to VCCO. The variation in the Thevenin average current is -24.5%/+15.5% whereas the T termination variation is -7.4%/+4.8%. Further the T termination average current can be adjusted by changing RTT. There is no such flexibility in the Thevenin termination.
  - 3) In the two tables there is a line item for the termination power. This accounts for the fact that the Thevenin termination dissipates power in the resistive divider even if each LVPECL output is not connected to its respective terminator. **The total power accounting must include this idle bias power.** The T termination does not incur this penalty because the VTT voltage is derived directly from IOH and IOL. The signal integrity of the Thevenin termination is not adversely impacted by its power penalty relative to the T termination, but the designer should be mindful of the line item for every LVPECL termination in a design's power budget.

There are three takeaways from this comparison:

1. Changes in VTT from the standard do not exercise the common mode range of the LVPECL receiver, the common mode range of VOH and VOL does.
2. The LVPECL receiver does not sense VTT. The significance of VTT is only that it is to be set such that the VOL transistor is not cut off for best switching time performance. Any termination that controls these currents as well or better than the standard LVPECL termination will suffice.
3. The benefits of the T termination are less variation in power consumption over VCCO and device variation. More consistent switching time performance follows because both of these advantages are due to better control over emitter currents.

## Appendix: Alternative Calculation of the RTT Termination Resistor

It is possible to calculate an exact value for RTT to provide the standard Vcc-2.0V Thevenin termination voltage as shown in [Figure 18](#) below. The calculation is a straight forward application of KCL.

$$\left( \frac{V_{OH} - [V_{CC} - 2]}{Z_O} + \frac{V_{OL} - [V_{CC} - 2]}{Z_O} \right) * R_{TT} = [V_{CC} - 2]$$

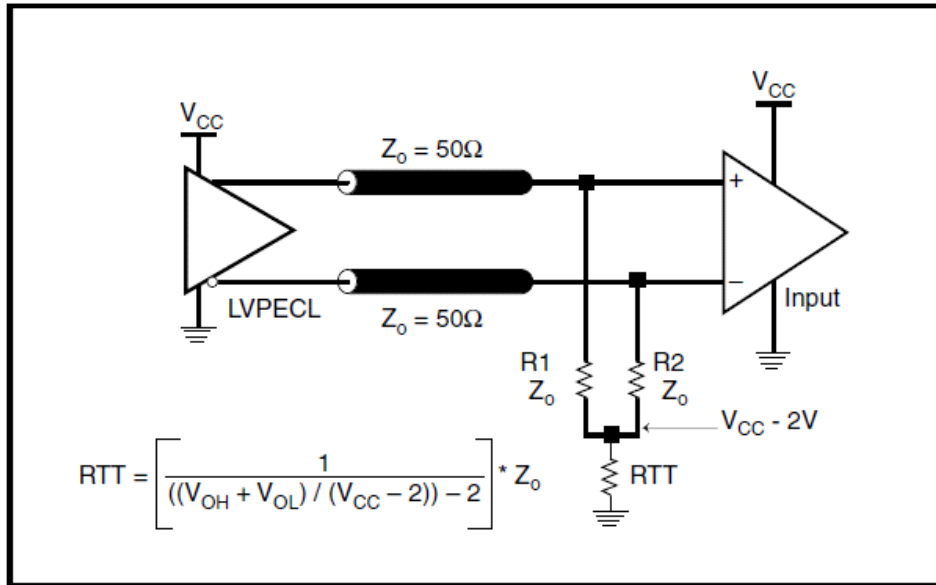
$$(V_{OH} + V_{OL} - 2 * [V_{CC} - 2]) * R_{TT} = Z_O * [V_{CC} - 2]$$

$$R_{TT} = \frac{Z_O}{\left( \frac{V_{OH} + V_{OL} - 2}{V_{CC} - 2} \right)}$$

The practical problem with this approach is that the value of RTT depends on VOH and VOL, which in turn directly depend on VCC in a manner different from that of the term VCC-2.0V. Therefore a corresponding value of RTT must be calculated for each value of VCC. Not only is this not practical, it is not necessary since the performance of the LVPECL emitter follower outputs for power consumption and rise/fall time do not depend on the VTT being exactly VCC-2.0V as discussed in [Appendix: Comparison of T and Thevenin LVPECL Terminations](#).

One of the main advantages of the PI and T terminations is that they place more negative feedback on the emitter follower outputs and therefore provide for greater stability of the output transistor currents than the Thevenin termination can provide. Instead the design approach for the PI and T networks is to select the nominal bias current through the output transistors to get the appropriate trade-off between power, switching speed and output amplitude across power supply variations.

**Figure 18. Exact Calculation of  $R_{TT}$  to Realize  $V_{TT} = V_{CC} - 2.0V$**





## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:  
[www.renesas.com/contact/](http://www.renesas.com/contact/)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.