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H8/300L Super Low Power Series

Addition of Multiple-Precision BCD Numbers (ADDD2)

Introduction

The software ADDD2 adds a multiple-precision binary-coded decimal (BCD) number to another multiple-precision BCD number and places the result in the data memory where the augend was placed.

Target Device

H8/38024

Contents

1. Arguments

Description		Memory area	Data length (bytes)
Input	Augend and addend byte count	R0L	1
	Start address of augend	R3	2
	Start address of addend	R4	2
Output	Start address of the result of addition	R3	2
	Error	Z flag (CCR)	—
	Carry	C flag (CCR)	—

2. Changes to Internal Registers and Flags

R0	R1	R2	R3	R4	R5	R6	R7
×	×	×	○	×	×	—	—

I	U	H	U	N	Z	V	C
—	—	×	—	×	○	×	○

Legend
—: No change
×: Undefined
○: Result

3. Specifications

Program memory (bytes)
44
Data memory (bytes)
0
Stack (bytes)
0
Clock cycle count
7680
Reentrant
Possible
Relocation
Possible
Interrupt
Possible

4. Notes

The clock cycle count (7680) in the specifications is for addition of 255 bytes to 255 bytes.

5. Description

5.1 Details of functions

1. The following arguments are used with the software ADDD2:
   - R0L: Sets, as an input argument, the byte count of an augend and an addend in 2-digit hexadecimals.
   - R3: Sets the start address of the augend in the data memory area. The start address of the result of addition is placed in this register after execution of the software ADDD2.
   - R4: Sets, as an input argument, the start address of the addend in the data memory area.
   - Z flag (CCR): Indicates an error in data length as an output argument.
     - Z flag = 0: The data byte count (R0L) was not 0.
     - Z flag = 1: The data byte count (R0L) was 0 (indicating an error).
   - C flag (CCR): Indicates whether there is or isn't a carry, as an output argument, after execution of the software ADDD2.
     - C flag = 0: There is no carry in the result of addition.
     - C flag = 1: There is a carry in the result of addition (see figure 2).

2. The following figure illustrates the execution of the software ADDD2. When the input arguments are set as shown in (1), the result of addition is placed in the data memory area as shown in (2).

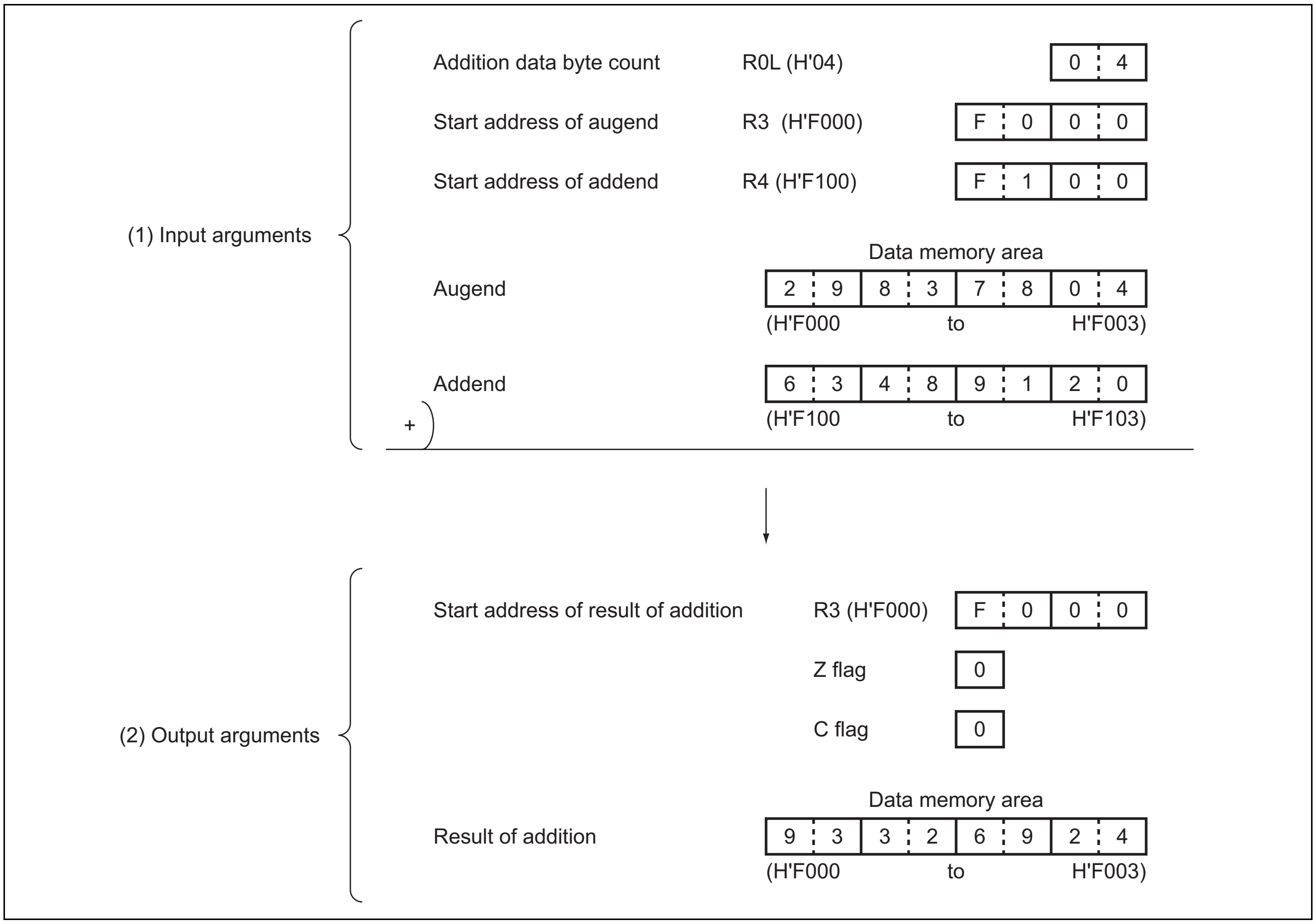


Figure 1 Example of Software ADDD2 Execution

Figure 2 shows an example of addition where a carry has been produced.

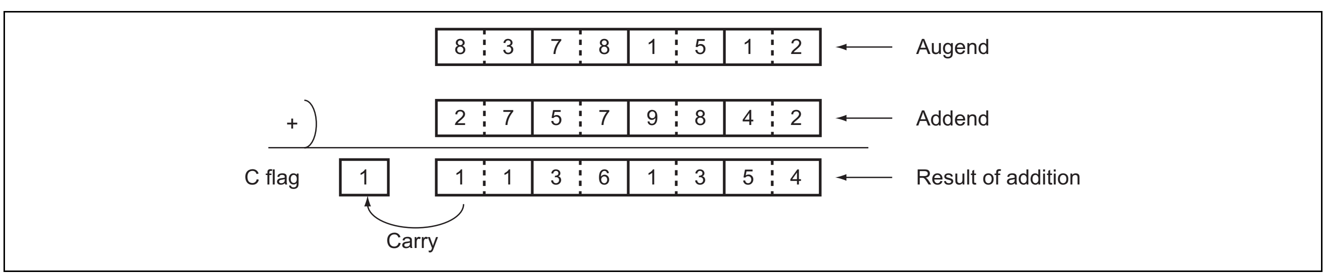


Figure 2 Example of Addition with a Carry

5.2 Notes on usage

1. When the upper bits are not used (see figure3), set them to 0. The software ADDD2 performs byte-based addition; when 0 are not set in the unused upper bits, a correct result cannot be obtained because the addition is done on the numbers including indeterminate data.

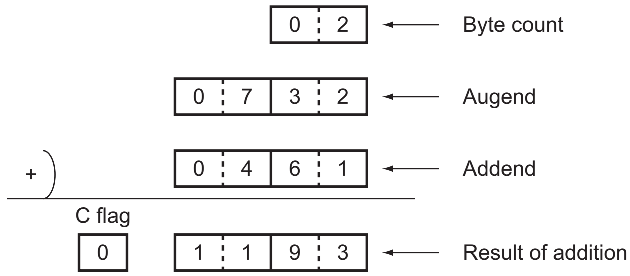


Figure 3 Example of Addition with Upper Bits Unused

2. After execution of the software ADDD2, the augend will be lost because the result is placed in the data memory area where the augend was set. When the augend is still needed after software ADDD2 execution, save it in memory.

5.3 Data memory

The software ADDD2 uses no data memory.

5.4 Example of usage

This is an example of adding 8 bytes of data. Set the start addresses of a byte count, an augend, and an addend in the registers and call the software ADDD2 as a subroutine.

```
WORK1    .RES.B    1              ---------- Reserve a data memory area in which the user program places
                                             a byte count.

WORK2    .RES.B    8              ---------- Reserve a data memory area in which the user program places
                                             an 8-byte (16-digit BCD) augend.

WORK3    .RES.B    8              ---------- Reserve a data mermoy area in which the user program places
                                             an 8-byte (16-digit BCD) addend.
           .
           .
           .
         MOV.B     @WORK1, R0L    ------- Place in the input argument (R0L) the byte count
                                          set by the user program.

         MOV.W     #WORK2, R3     ------- Place in the input argument (R3) the start address
                                          of the augend set by the user program.

         MOV.W     #WORK3, R4     ------- Place in the input argument (R4) the start address
                                          of the addend set by the user program.

         JSR       @ADDD2         ------- Call the software ADDD2 as a subroutine.

         BCS       OVER           ------- Branch to the carry processing routine
                                          when a carry has occurred in the result of addition.
           .
           .
           .
OVER     Carry processing routine
```

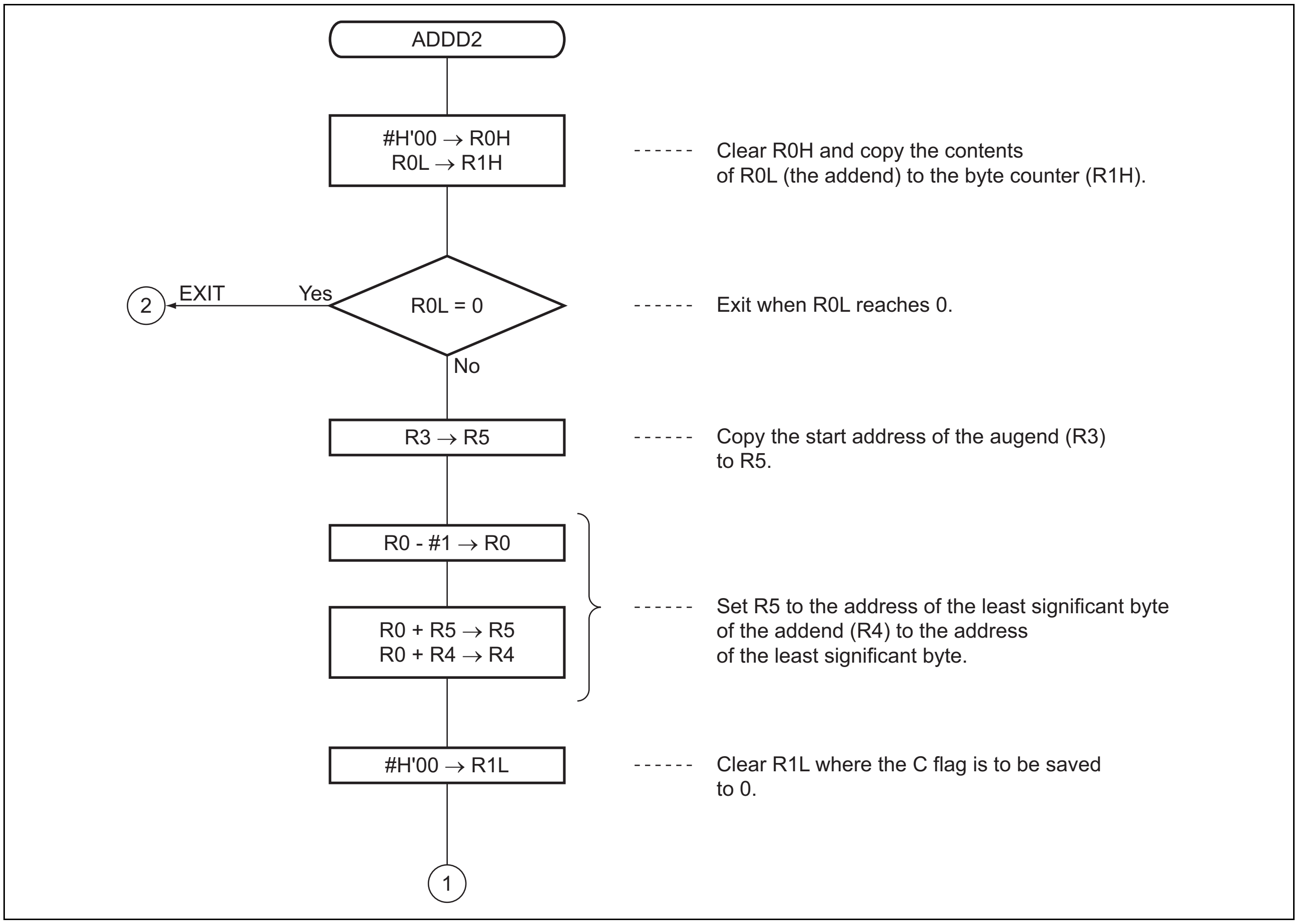
5.5 Operation

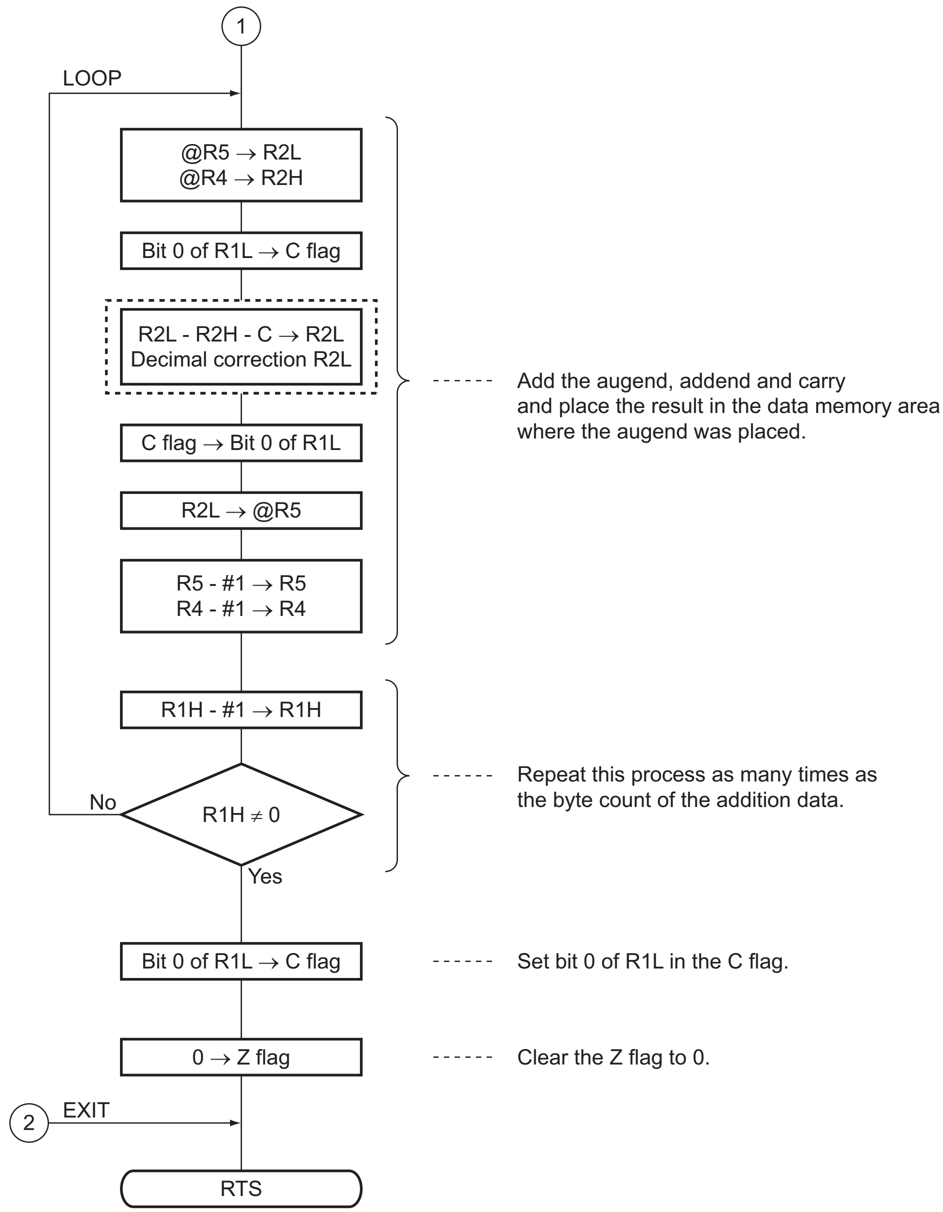
1. Since the augend and addend data are placed in registers, 2 digits in 1 byte, addition of multiple-precision BCD numbers can be done by performing a series of 1-byte add instructions (ADDX.B) with decimal-correct instructions (DAA).
2. The address of the lowest byte of the data memory area for the augend is placed in R3, and the address of the lowest byte of the data memory area for the addend in R4.
3. R1L that is used for saving the C flag is cleared.
4. The augend and addend are loaded to R2L and R2H respectively, byte by byte, starting at their lowest byte and then the operation given by equation 1 is executed:

   R2L (augend) + R2H (addend) + C → R2L
   Decimal correction of R2L → R2L ------- equation 1
   R2L → @R3

   where the C flag indicates a carry that may be produced in the result of addition of the lower bytes.
5. The result of step (4) is placed in the data memory area for the augend.
6. R3, R4, and R0L are decremented each time the operation of steps 4 and 5 has been finished. This processing is repeated until R0L reaches 0.

6. Flowchart


ADDD2
#H'00 → R0H
R0L → R1H
Clear R0H and copy the contents of R0L (the addend) to the byte counter (R1H).
EXIT
Yes
R0L = 0
Exit when R0L reaches 0.
No
2
R3 → R5
Copy the start address of the augend (R3) to R5.
R0 - #1 → R0
R0 + R5 → R5
R0 + R4 → R4
Set R5 to the address of the least significant byte of the addend (R4) to the address of the least significant byte.
#H'00 → R1L
Clear R1L where the C flag is to be saved to 0.
1



Note: ADDD2 is the same as ADD2, SUB2 and SUBD2 except for the stop surrounded by dotted lines.

7. Program List

```
*** H8/300 ASSEMBLER VER 1.0B ** 08/18/92 10:02:42
PROGRAM NAME =
                               ;*****************************************************************
                               ;*
                               ;*      00 - NAME  :MULTIPLE-PRECISION DECIMAL ADDITION
                               ;*                  (ADDD2)
                               ;*
                               ;*****************************************************************
                               ;*
                               ;*      ENTRY      :R0L (BYTE COUNTER OF ADDTION DATA)
                               ;*                  R3 (START ADDRESS OF AUGEND)
                               ;*                  R4 (START ADDRESS OF ADDEND)
                               ;*
                               ;*      RETURNS    :R3 (START ADDRESS OF RESULT)
                               ;*                  Z flag OF CCR (Z=0;TRUE,Z=1;FALSE)
                               ;*                  C flag OF CCR (C = 0;TRUE,C = 1;OVERFLOW)
                               ;*
                               ;*****************************************************************
                               ;
ADDD2_co C   0000                      .SECTION            ADDD2_code,CODE,ALIGN=2
                     .EXPORT   ADDD2
                               ;
ADDD2_co C         00000000    ADDD2   .EQU $              ;Entry point
ADDD2_co C   0000  F000                MOV.B    #H'00,R0H  ;Clear R0H
ADDD2_co C   0002  0C81                MOV.B    R0L,R1H    ;Clear R1H
ADDD2_co C   0004  4724                BEQ      EXIT       ;Branch if Z=1 then exit
ADDD2_co C   0006  0D35                MOV.W    R3,R5
ADDD2_co C   0008              MAIN
ADDD2_co C   0008  1B00                SUBS.W   #1,R0      ;Decrement R0
ADDD2_co C   000A  0905                ADD.W    R0,R5      ;Set end address to summand pointer
ADDD2_co C   000C  0904                ADD.W    R0,R4      ;Set end address to addend pointer
ADDD2_co C   000E  F900                MOV.B    #H'00,R1L  ;Clear R1L
ADDD2_co C   0010              LOOP
ADDD2_co C   0010  685A                MOV.B    @R5,R2L    ;Load summand data
ADDD2_co C   0012  6842                MOV.B    @R4,R2H    ;Load addend data
ADDD2_co C   0014  7709                BLD      #0,R1L     ;Bit load bit 0 of R1L
ADDD2_co C   0016  0E2A                ADDX.B   R2H,R2L    ;R2H + R2L + C -> R2L
ADDD2_co C   0018  0F0A                DAA      R2L        ;Decimal adjust R1L
ADDD2_co C   001A  6709                BST      #0,R1L     ;Store C falg to bit 0 of R1L
ADDD2_co C   001C  68DA                MOV.B    R2L,@R5    ;Store struct
ADDD2_co C   001E  1B05                SUBS.W   #1,R5      ;Decrement summand pointer
ADDD2_co C   0020  1B04                SUBS.W   #1,R4      ;Decrement addend pointer
ADDD2_co C   0022  1A01                DEC.B    R1H        ;Decrement R1H
ADDD2_co C   0024  46EA                BNE      LOOP       ;Branch if Z=0
                               ;
ADDD2_co C   0026  7709                BLD      #0,R1L     ;Load bit 0 of R1L to C flag
ADDD2_co C   0028  06FB                ANDC.B   #H'FB,CCR  ;Clear Z flag of CCR
ADDD2_co C   002A              EXIT
ADDD2_co C   002A  5470                RTS
                               ;
                                       .END
*****TOTAL ERRORS 0
*****TOTAL WARNINGS 0
```

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