Zilker Labs System Design Checklist

Introduction

Digital-DC™ power design allows for optimal configuration, parametric monitoring and increased efficiency while reducing the number of power supply components. Zilker Labs DC-DC conversion/management devices bring Digital-DC technology to a wide range of power supply design needs. System requirements and implementation considerations must be analyzed to maximize the performance of a DC-DC conversion. The PCB design also should be scrutinized to optimize performance. With the benefits of Digital-DC technology, the configuration of the conversion device can further optimize the design. Use this document as a check list during design and bring-up. This document is useful as a guide at the beginning of a design as well as a review/verification list at the end of a design process.

System level considerations

System Requirements

- ☐ Rail identification and number assignment (Rail DDC ID)
- ☐ Design optimization goals
  - o Efficiency, PCB area, transient response, cost, or some combination? (optimizing for one component may force design tradeoffs in other areas)
- ☐ Input Voltage
  - o Specify Vin nominal, min and max (UV and OV levels)
  - o Designs accommodating a wide input range may compromise peak performance at any specific input voltage.
  - o Current limitations on Vin (Iin)
- ☐ Output Voltage
  - o Specify nominal output voltage, margin range and UV/OV levels.
  - o Total output tolerance budget:
    - DC voltage regulation accuracy (output variation based on initial setpoint, line/load regulation, and temperature).
    - Ripple tolerance range. It is recommended to design the circuit for ≤ 1% peak ripple in order to optimize the transient response.
    - Voltage deviation due to load (output current) transients.
  - o Inductor DCR current sensing mode is limited to Vout ≤ 4.0V.
  - o Pre-bias requirements
  - o Different Vin/Vout combinations will force different criteria for power train components.
  - o Designs accommodating a wide output voltage range may compromise peak performance at any specific output voltage.
- ☐ Output current
  - o Specify maximum output current required
    - Consider average and peak over current fault settings
  - o Specify output current transient requirements
    - Amplitude and rate
  - o The accuracy of the current sensing element should be considered
    - Inductor DCR or FET RDSon

- ☐ Operating temperature range
  - Ambient, junction, or PCB temp range?
  - Is there any airflow?
- ☐ Switching frequency
  - Zilker Labs devices can operate over a wide range of switching frequencies. The power train circuitry must be designed for a specific frequency range in order to maintain consistent performance results (efficiency, stability, transient response, etc)
  - External SYNC signal available?
    - Required for current share operation
- ☐ Tracking required?
  - Does this rail need to track another voltage? (The VTRK pin is used as an analog input; the voltage applied to this pin must be ≤ 5V)
  - Does it need to track at 50% or 100% of the external voltage?
  - Does it need to track only during ramps, or continuously?
- ☐ Sequencing required?
  - Is re-configurable sequencing needed?
    - Is it desired that each rail starts its ramp at a specific time following the assertion of the EN pin?
      - All EN pins must be connected together
      - The user must configure a soft start ramp delay and ramp time for each voltage rail.
    - Is event-based sequencing needed? (A given rail must wait for the prior rail to be regulating prior to starting its initial ramp)
      - Each rail must be configured with a specific DDC ID
    - Will an external device be used to drive EN pins and monitor PG pins?
- ☐ Current sharing
  - Maximum current per phase
  - Refer to AN2034 for configuration

Schematic Design Considerations

- ☐ Use a Zilker Labs example schematic or previous design (refer to EVB data sheet)
- ☐ For Vin < 4.5V, connect VDD to VR directly
- ☐ Device pin-strap: Maximum desired output voltage
- ☐ Device pin-strap: SMBus addressing
- ☐ SMBus pull-up resistors to logic rail
- ☐ SMBus access header
- ☐ DDC bus grouping and pull-up to logic rail
  - o Common all rails to DDC bus for group coordination
  - o Provide standby logic pull-up with/before applying VDD
- ☐ SYNC (switching clock) source and circuit grouping
  - o Common SYNC to all devices and drive from local source
- ☐ Apply recommended decoupling to regulator pins (e.g. VR and V25)
- ☐ Apply external temperature element near current sensing element
  - o Temperature compensation of current measurements
- ☐ Output capacitance to meet ripple requirement
  - o Selection and placement
- ☐ Output capacitance for transient response
- ☐ Input capacitance, decoupling for ripple/transient energy
- ☐ FET and inductor selection for efficiency and thermal requirements
- ☐ H/W enable (EN pin) or PMBus enable?
  - o Common EN pin and use SEQUENCE feature
- ☐ H/W margin (MGN pin) or PMBus margin?
- ☐ Use PG indicator pin?
  - o Not necessary when using SEQUENCE and PMBus monitoring
- ☐ Inductor DCR or FET RDSon current sense?
  - o DCR method more accurate and repeatable
- ☐ Sensitive traces
  - o VSENSE polarity
  - o ISENSE polarity
  - o XTEMP polarity
  - o SGND, DGND and PGND routing
- ☐ Consider series component in high-side FET gate drive
- ☐ Consider RMS and peak gate drive requirement
- ☐ Voltage tracking required (VTRK pin)?
- ☐ Apply fundamental switching power supply design considerations

PCB Layout Design Considerations

- ☐ Zilker Labs example layout or previous design (refer to EVB data sheet)
- ☐ Refer to Zilker Labs layout guidelines (AN2010)
  - o Fundamental switching power supply design considerations
  - o Reduce exposure to SW node and gate drive ringing
  - o Correct application of boost circuit components
- ☐ Design accurate shape for Zilker Labs devices
  - o Include epad in solder mask
  - o Include epad in solder paste mask
- ☐ Verify device pin-strap: Maximum desired output voltage
- ☐ Verify device pin-strap: SMBus addressing
- ☐ Verify SMBus pull-up resistors to logic rail
- ☐ Verify SMBus access header
- ☐ Current calibration: characterization method and procedure
- ☐ Verify DDC bus grouping and pull-up to logic rail
  - o Common all rails to DDC bus for group coordination
  - o Provide standby logic pull-up with/before applying VDD
- ☐ Verify SYNC (switching clock) source and circuit grouping
  - o Common SYNC to all devices and drive from local source
- ☐ Verify recommended decoupling to regulator pins (e.g. VR and V25)
- ☐ Verify output capacitance to meet ripple requirement
  - o Selection and placement
- ☐ Verify output capacitance for transient response
- ☐ Verify input capacitance, decoupling for ripple/transient energy
- ☐ Verify FET and inductor selection for efficiency and thermal performance
- ☐ Verify enable can be held low until configuration at production
- ☐ Sensitive traces
  - o VSENSE, routing and polarity
  - o ISENSE, routing and polarity
  - o XTEMP, routing and polarity
- ☐ Verify FET gate drive routing
- ☐ Verify Thermal design

PMBus Configuration File Considerations (PowerPlan)

- ☐ Follow the recommended configuration file method as described in:
  - o AN2031 - Writing Configuration Files
- ☐ Apply sequence and enable delay/ramp time settings
- ☐ Consider fault response settings (shutdown or retry)
- ☐ Consider VOUT_COMMAND setting
- ☐ Enter compensation and NLR settings
- ☐ Measure and enter current calibration values
  - o IOUT_CAL_GAIN, IOUT_CAL_OFFSET, MFR_CONFIG, TEMPCO_CONFIG
- ☐ Enter external temperature measurement settings
  - o MFR_CONFIG, TEMPCO_CONFIG
- ☐ Add the MFR_xxxx commands to provide descriptive information
  - o Information will be in the file and in each configured device
- ☐ Is MFR_SERIAL present, and configuration will be converted to ZLHLD format?
  - o Ensure that MFR_SERIAL is the fifth command line in the configuration file (see AN2036 for more details)
- ☐ Consider the enable method, hardware or PMBus?
  - o Broadcast Enable required? (PMBus enable only)
- ☐ Using Command Protection via PRIVATE_PASSWORD in Default Store?
  - o Refer to recommended file structure in AN2031
  - o Is desired Private Password EXACTLY 9 characters in length?
  - o Does UNPROTECT string protect commands STORE_DEFAULT_ALL and RESTORE_FACTORY, in addition to commands desired to be protected?
- ☐ Using Command Protection via PRIVATE_PASSWORD in User Store?
  - o Refer to recommended file structure in AN2031
  - o Is desired Private Password EXACTLY 9 characters in length?
  - o Does UNPROTECT string protect commands STORE_DEFAULT_ALL, RESTORE_FACTORY, STORE_USER_ALL, and RESTORE_DEFAULT_ALL, in addition to commands desired to be protected?
- ☐ Using Command Protection via PUBLIC_PASSWORD in User Store?
  - o Refer to recommended file structure in AN2031
  - o Is desired Public Password EXACTLY 4 characters in length?
- ☐ Comment well for future reference

Design Bring-up Considerations

- ☐ Enables pulled low on power up
- ☐ Devices configured before enabled
- ☐ Optimize compensation for stability/transient performance
- ☐ Verify SW and BST pins remain within operating specifications
  - o relative and absolute potential

References

[1] AN2013 – *ZL2005 and PMBus ™*, Zilker Labs, Inc., 2006.

Revision History

Date	Rev. #	
August 2008	1.0	Initial Release
Aug 2008	1.1	Added PASSWORD and serial number considerations under config file section.
May 2009	1.2	Assigned file number AN2037 to app note as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content.

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.0