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April 1st, 2010
Renesas Electronics Corporation

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M32C/83 Group

Clocked Serial I/O Function by using Intelligent I/O Group 0 and 1

1.0 Abstract

This app-note describes the clock serial I/O (synchronous serial I/O) operation of Intelligent I/O Group 0 and 1 (IIO Group 0 and 1).

2.0 Introduction

This application note is applied to the M32C/83 Group microcomputer only.

3.0 Detailed Description

This application example offers features of the serial I/O shown in Table 1. The transmit data is output from pin ISTxDi. The transfer clock is output from pin ISCLKi, the receive data is input from pin ISRxDi. Here symbol i represents the IIO Group number. When IIO Group 0 (and Group 1) is used, symbol i becomes 0 (and 1 respectively).

Table 1 Clocked Serial I/O Option Features and Selected Features

Item	Definition	Selection in this example
Transfer Clock Selection	Internal Clock	Yes
	External Clock	
Data Format	LSB First	Yes
	MSB First	
Polarity Selection of pins TxD and RxD	Non Reverse Output	Yes
	Reverse Output	
Transmit Interrupt Factor	When register GiTB becomes empty	
	When the transmission is completed	Yes

(1) Transfer speed definition when using Channel 0

This example uses Channel 0 in the wave generation function. Select "Use the output of the communication function" for this operation. Base Timer is reset when the set value of register GiP00 matches the content of Base Timer. The transfer speed (the period of the transfer clock) is defined by the following equation. Here "fBT" and "n" represents the count source of Base Timers and value of register GiP00 respectively. But "n" must be 1 or greater.

$$\text{Transfer Speed} = \text{fBT} / 2 \times (n + 2)$$

For example, when fBT = 30MHz, the max transfer speed is 5Mbps.

(2) How to generate the transfer clock by using Channel 3

This example uses Channel 3 in the inverted waveform output mode of the wave generation function. The set value of register GiP03 must be smaller than the set value of register GiP00.

3.1 Register setting

To enable the operation defined in “Section 3.0 Description”, the following register settings must be taken place step by step.

- (1) Disabling the interrupt (Set I flag = 0)

Set I flag = 0. Or set bits ILV2 - 0 = 0b000 in register IIOkIC (k = 0 - 11) where the interrupt request of the Intelligent I/O is assigned.

- (2) Set Register IPS = 0b000000xx (here x depends on user configuration)

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:2]	---	Not used (Set 0b000000 to the bits)
Bit 1	IPS1	Group 1 Input Pin Select Bit 0: assigns ISRxD1 to Port P75 1: assigns ISRxD1 to Port P112
Bit 0	IPS0	Group 0 Input Pin Select Bit 0: assigns ISRxD0 to Port P80 1: assigns ISRxD0 to Port P152

This setting enables use of the receive pin.

- (3) Set Register G2BCR0 = 0b01111111

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	---	Not used (Set 0 to the bit)
Bits [6:2]	DIV4-0	Count Source Division Ratio Select Bits 0b11111: selects no division
Bits [1:0]	BCK1-0	Count Source Select Bits 0b11: selects clock f1

This setting enables use of register B TSR that will be configured in the next step.

- (4) Set Register B TSR = 0b00000000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:4]	---	Not used (Set the bits to 0b0000)
Bits [3:0]	BT3S-BT0S	Base Timer Count Start Bits 0b0000 resets Base Timers in Groups 3 – 0

This setting resets Base Timers in Groups 0 – 4. The Base Timer in Group i starts counting at 0x0000 when selecting the count source of the Base Timer with register GiBCR0 and then setting bit BTS = 1 in register GiBCR1. Here symbol i represents IIO Group number.

(5) Set Register G2BCR0 = 0b00000000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:2]	---	Not used (Set the bits to 0b000000)
Bits [1:0]	BCK1-0	Count Source Select Bits 0b00: supplies no clock

If Group 2 and register BTSR are not used, disable supplying a clock to Group 2.

(6) Set Register GiBCR0 = 0b01111111

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	---	Not used (Set the bits to 0b0)
Bits [6:2]	DIV4-0	Count Source Division ratio Bits 0b00000 selects no division
Bits [1:0]	BCK1-0	Count Source Select Bits 0b00 selects clock f0

This setting enables use of registers that are defined in step (7) thru (15). Set 0b01111111 to this register before going to the following steps. In this way, following registers will hold valid values at the transfer operation.

(7) Set Register GiBCR1 = 0b00000010

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	---	Not used (Set the bit to 0b0) Set the bit to 0.
Bits [6:5]	UD1-0	Up-Down Control Bits 0b00 selects the up-count mode
Bit 4	BTS	Base Timer Start Bit 0b0 resets Base Timer.
Bits [3:2]	---	Not used (set the bit to 0b00)
Bit 1	RST1	Base Timer Reset Cause Select Bit 1 0b0 selects that the reload action occurs when the Base Timer content matches to the content of register GiPO0
Bit 0	---	Not used (set the bit to 0b0)

This register is used for generating the transfer clock. Set bit RTS1 = 1. (The Base Timer is reset when the Base Timer content matches to the content of register GiPO0)

(8) Set Register GiPOCR0 = 0b00000111

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:6]	---	Not used (Set the bits to 0b00)
Bit 5	RLD	Reload Timing Select Bit 0b0 selects the reload action occurs when the register is written.
Bits [4:3]	---	Not used (Set the bits to 0b00)
Bits [2:0]	MOD2-0	Operation Mode Select Bits 0x111 selects the output of the communication function.

The setting (bits MOD2 – 0 = 0b111) selects pin ISTxDi to transmit data. The setting (bit RLD = 0) configures the reload action to occur at the same time data is written to register GiPO0.

(9) Set Register GiPOCR1 = 0b00000111

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:3]	---	Not used (Set the bits to 0b00000)
Bits [2:0]	MOD2-0	Operation Mode Select Bits 0x111 selects the output of the communication function.

The setting (bits MOD2 –0 = 0b111) selects pin ISCLKi to generate the transfer clock.

(10) Set Register GiPOCR3 = 0b00000010

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:6]	---	Not used (Set the bits to 0b00)
Bit 5	RLD	Reload Timing Select Bit 0b0 selects the reload action occurs when the register is written.
Bits [4:3]	---	Not used (Set the bits to 0b00)
Bits [2:0]	MOD2-0	Operation Mode Select Bits 0x010 selects the inverted wave output.

The setting (bits MOD2 –0 = 0b010) selects pin ISCLKi to generate the transfer clock in the inverted wave generation mode. The setting (bit RLD = 0) configures the reload action occurs at the same time data is written to register GiPO0.

(11) Set Register GiPO0 = 0x0001 – 0xFFFFD

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [15:0]	---	This register defines the transfer speed. The transfer speed (bps) is formulated by: $bps = fBT / 2^{*(n+2)}$ n (set-value) = 0x0001 – 0xFFFFD

(12) Set Register GiPO3 = 0x0001

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [15:0]	---	must be set to 0x0001.

0x0001 enables that the transfer clock specified in section (27) is generated immediately after Base Timer starts.

(13) Set Register GiFS = 0b00000000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:4]	---	Not used (Set the bits to 0b0000)
Bit 3	FSC3	Channel 3 Time Measurement/Wave Generation Select Bit 0b00 selects the wave generation function.
Bit 2	---	Not used (Set the bit to 0b0)
Bits [1:0]	FSC1-0	Channel 1 & 0 Time Measurement/Wave Generation Select Bits 0b00 selects the wave generation functions

(14) Set GiFE Register

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:4]	---	Not used (Set the bits to 0b0000)
Bit 3	IFE3	Channel 3 Function Enable Bit 0b1 enables the Channel 3 function.
Bit 2	---	Not used (Set the bit to 0b0)
Bits [1:0]	IFE1-0	Channel 1 and 0 Function Enable Bits 0b11 enables the Channel 1 & 0 functions.

Set 0 to bits respective to un-used Channels.

(15) Set Register GiBCR1 = 0b00010011

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 4	BTS	Base Timer Start Bit 0b1 enables Base Timer to start counting.

By setting bit BTS = 1, the transfer clock starts generating.

(16) Set Register GiCR = 0b00000000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	OPOL	TxD Output Polarity Reverse Select Bit 0b0 selects no reversing.
Bit 6	IPOL	ISrxD Input Polarity Reverse Select Bit 0b0 selects no reversing.
Bit 5	RE	Receive Enable Bit 0b0 disable the receive.
Bit 4	TE	Transmit Enable Bit 0b0 disable the transmission.
Bit 3	---	Not used (Set the bit to 0b0)
Bit 2	RI	Receive Complete Flag (Read-Only)
Bit 1	TXEPT	Transmit Register Empty Flag (Read-Only)
Bit 0	TI	Transmit Buffer Empty Flag (Read-Only)

Bits TI, TXEPT, and RI are read-only bits. Write-action to these bits effect nothing.

Bits TE and RE (Transmission and Receive Enable Bits) must be set after setting the other communication related reregisters.

(17) Set Register GiMR = 0b10000001

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	IRS	Transfer Interrupt Cause Select Bit 0b1 selects "Transmission Complete (TXEPT = 1)".
Bit 6	UFORM	Transfer Direction Select Bit 0b0 selects the LSB-first.
Bits [5:3]	---	Not used (Set the bits to 0b000)
Bit 2	CKDIR	Internal/External Clock Select Bit 0b0 selects the internal clock
Bits [1:0]	GMD1-0	Communication Mode Select Bits 0b01 selects the clocked serial I/O mode.

Selects the clocked serial I/O mode with bits GMD1-0 (= 0b00).

(18) Set Register GiERC = 0b00100000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:6]	---	Not used (Set the bits to 0b00).
Bit 5	RSTHE	Receive Shift Operation Enable Bit 0b1 enables the receive shift action.
Bits [4:0]	---	Not used (Set the bits to 0b00000).

Bit RSHTE = 1 enables supplying the clock generated in Channel 3 to the receive shift register. This bit must be set to 1 when using the clock serial I/O mode.

(19) Set Register GiBCR = 0b00000010

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 4	BTS	Base Timer Start Bit Clear the bit to 0b0

Clear bit BTS before setting fBT.

(20) Set Register GiBCR0 = 0b0*****11 (* indicates user's choice)

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	---	Not used (set 0b0 to the bit)
Bits [6:2]	DIV4-0	Count Source Division Ratio Select Bits Set your own value.
Bits [1:0]	BCK1-0	Count Source Select Bit 0b11 selects clock f1 (fBT).

Define your baud-rate with bits DIV4-0.

(21) Set Register GiBCR1 = 0b00010010

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 4	BTS	Base Timer Start Bit Set the bit to 0b1 for Base Timer to start counting.

(22) Set IIOkIE (k = 0 thru 3) = 0b00000001

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit [7:1]	---	Interrupt Enable Bits 7 thru 1 Set the bits to 0b0000000
Bit 0	IRLT	Interrupt Request Latch Bit 0b1 enables that the request is used for the interrupt.

Bits [7:1] and bit IRLT must not be set to 1 at the same time.

(23) Set Register IIOkIR (k = 0 thru 3) = 0b00000000

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:1]	---	Clear the bits to 0b00000000
Bit 0	---	Not used (Set the bit to 0b0)

The register must be set 0x00 here. If the register holds a value other than 0x00, bit IR in register IIOkIC will not be set to "1" even when an interrupt request is generated. -- means no interrupt operation possible.

(24) Set Register IIOkIE (k = 0 thru 3) = 0b00*00001 (* depends on user configuration)

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:6]	---	Not used (Set the bits to 0b00)
Bit 5	SIOiTE	IIO Group i (i = 0 or 1) Transmit Interrupt Enable Bit Here, k must be 1 or 3 0b1 enables the request.
	SIOiRE	IIO Group i (i = 2 or 3) Receive Interrupt Enable Bit Here, k must be 0 or 3 0b1 enables the request.
Bits [4:1]	---	Not used (Set the bits to 0b0000)
Bit 0	IRLT	Interrupt Request Latch Bit 0b0 selects the request for the interrupt.

(25) Set Register IIOkIC (k = 0 thru 3) = 0b00000**** (* depends on k, user configuration)

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:5]	---	Not used (Set the bits to 0b0000)
Bit 4	IR	Interrupt Request Bit 0b0 sets no interrupt request.
Bits [2:0]	ILV2-0	Interrupt Priority Level Select Bits Set the values (k = 0 thru 3) based on your configuration.

(26) Set Registers PSC, PSLa (a = 0 thru 3), PSb (b = 0 thru 9)

This operation configures ports to be used for ISTxD and ISCLK functions.

(27) Set I flag = 1 (Set the prime interrupt for "Enable")

(28) Set Register CiCR = 0b00110000

Set the register for enabling receive and transmit operations.

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bit 7	OPOL	ISTxD Output Polarity Select Bit 0b0 selects no reversing.
Bit 6	IPOL	ISRxD Input Polarity Reverse Select Bit 0b0 selects no reversing.
Bit 5	RE	Receive Enable Bit 0b1 enables the receive.
Bit 4	TE	Transmit Enable Bit 0b1 enable the transmission.
Bit 3	---	Not used (Set the bit to 0b0)
Bit 2	RI	Receive Complete Flag (Read-Only)
Bit 1	TXEPT	Transmit Register Empty Flag (Read-Only)
Bit 0	TI	Transmit Buffer Empty Flag (Read-Only)

(29) Set Register GiTB

<u>Bit Position</u>	<u>Symbol</u>	<u>Bit Name & Function</u>
Bits [7:0]	---	Set value to be transmitted

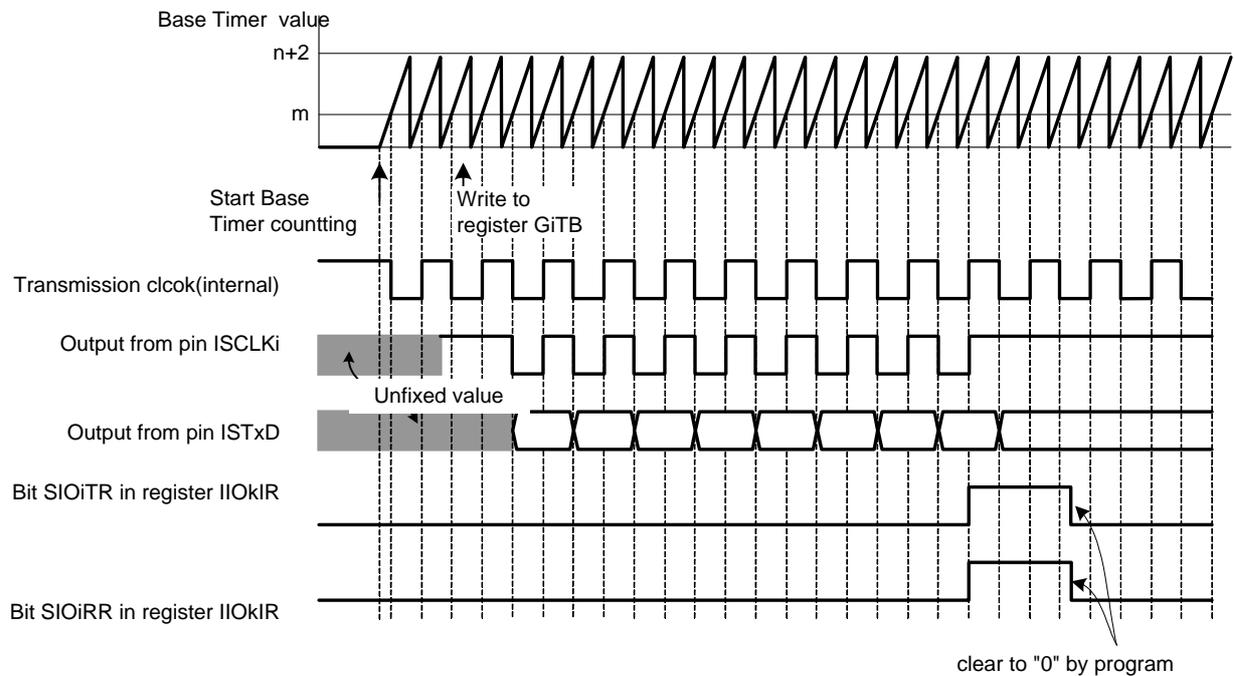
The write-action to the register starts the transmission.

3.2 Precaution on Interrupts

You must clear register IIOkIR to 0x00 during the respective interrupt routine. If you skip this procedure, bit IR in register IIOkIC will not be set to "1" when the respective IIO generates the interrupt request, resulting in no interrupt being invoked.

3.3. Timing Diagram

The following time chart shows the serial I/O operation in this example.



4.0 Sample Programming Code

```

/*****/
/* FILE NAME : apmc81.c */
/* Version : 1.00 */
/* CPU : M32C/83 */
/* FUNCTION : Clocked Serial communication by using Intelligent I/O */
/*-----*/
/* Copyright (C) 2001 Mitsubishi Electric Corporation and */
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/*****/
/*****/
/* include file */
/*****/
#include <stdio.h>
#include "sfr83v101.h"

/*****/
/* Function Definition */
/*****/
void receive_int(void);
#pragma INTERRUPT receive_int
void trans_int(void);
#pragma INTERRUPT trans_int

/*****/
/* Global Variable Definition */
/*****/
static char rec_buff;
static char cnt = 0;

/*****/
/* main Function */
/*****/
void main(void){
    _asm(" fclr i"); /* Disable the interrupt */

    /* main clock set */
    prc0 = 1; /* protect off */
    mcd = 0x12; /* main clock : no division */
    prc0 = 0; /* protect on */

    ips = 0x00; /* set P80 as ISRxD0 */

```

```
/* base clock initial set */
g2bcr0 = 0x7f; /* Enable use of register BTSTR */
btsr = 0x00; /* Reset the Base Timer */
g2bcr0 = 0x00; /* Stop the clock supply to Group 2 */

/* iio Group0 initial set */
g0bcr0 = 0x7f; /* b0,b1: count source f1
                b2-b6: division rate of count source : no division */
g0bcr1 = 0x02; /* Reset the Base Timer */

                g0pocr0 = 0x07; /* select ISTxD */
                g0pocr1 = 0x07; /* select ISCLK */
                g0pocr3 = 0x02; /* transmit clock (reversal waveform output mode) */

                g0po0 = 10; /* BRG = fTB / [(10+2)*2] */
                g0po3 = 1;

g0fs = 0x00; /* ch0 ch1 ch3 select the waveform generation function */
g0fe = 0x0b; /* ch0 ch1 ch3 enable */

g0bcr1 = 0x12; /* start the Base Timer counting */

g0cr = 0x00; /* Disable the communications */
g0mr = 0x81; /* Clocked Serial, internal clock, LSB first */

g0erc = 0x20; /* transmit clock -> receive shift register */

/* iio Group0 interrupt initial set */

iio0ie = 0x01; /* Use the request use for interrupt */
iio1ie = 0x01; /* Use the request use for interrupt */
iio0ir = 0x00;
iio1ir = 0x00;
iio0ie = 0x21; /* Enable interrupt to gr1 sio recive */
iio1ie = 0x21; /* Enable interrupt to gr1 sio trans */

iio0ic = 0x03; /* Set the interrupt priority level */
iio1ic = 0x03; /* Set the interrupt priority level */

/* port set */
psc = 0x00;
psl1 = 0x00;
ps1 = 0xc0;
ps2 = 0x00;

/* interrupt enable */
_asm("fset i");
```

```
g0cr = 0x30;          /* transmit / receive */

g0tb = 0xD5;         /* Write the transmit data */

while(1);
}

/* iio ch0 interrupt */
void receive_int(void){
    iio0ir = 0x00;    /* Clear the interrupt request */
    rec_buff = g0rb; /* Read the received data */
}

void trans_int(void){
    int wait;
    iio1ir = 0x00;    /* Clear the interrupt request */
    g0tb = 0x7A;     /* Write the transmit data */
}

/*----- end program */
```

5.0 Example of Pulse width measuring

The following example shows the clocked serial data transmission with pin ISTxD0(P76) and pin ISCLK0(P77) by using the Intelligent I/O Group 0.

Conditions: Supply voltage = 5V

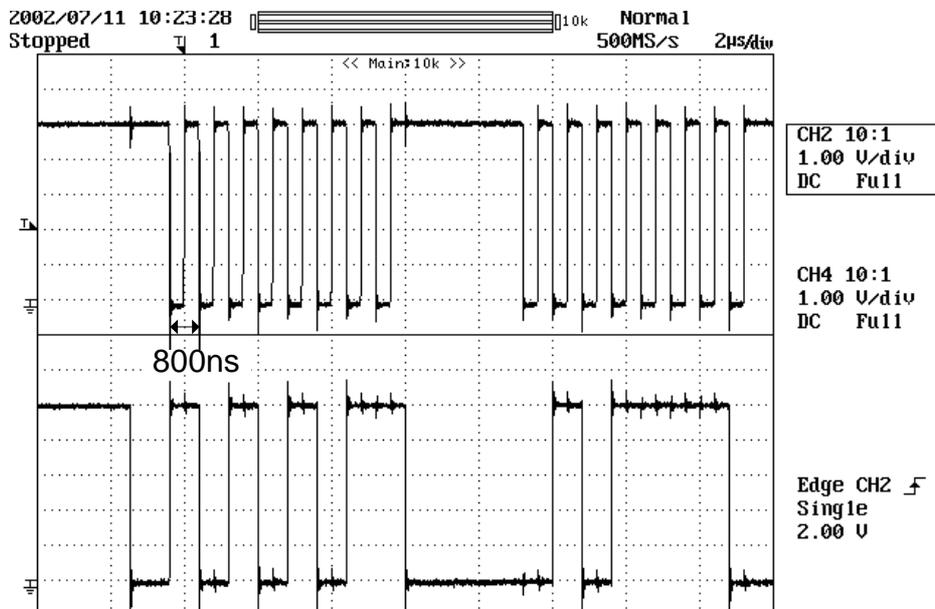
Main clock (XIN) = 30MHz

Base Timer count source (fBT) = 30MHz

Transmission speed: 1.25 Mbps(30MHz /24 : register G0PO0 value is 10)

Data transmission spend 800 nsec every bit.

Transmission data: 1st byte "D516". 2nd byte "7A16"



The result of data transmit with Clocked Serial communication.

6.0 Reference

Data Sheet

M32C/83 Group Rev. B3

(Use the latest version on the web: <http://www.infocom.maec.co.jp/M16C/dsum/32c83dse.htm>)

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