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# SH7263/SH7203 Groups

## Example of BSC Interface Connection to NOR-Type Flash Memory (16-Bit Data Bus)

### Introduction

This application note describes the interface functionality of the bus state controller (BSC) and provides a practical example of connection with asynchronous NOR-type flash memory.

### Target Devices

SH7263/SH7203

### Contents

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2. Description of Sample Application ..... 3

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# 1. Specifications

- 32-, 64-, or 128-Mbit NOR flash memory (from Spansion™) is connected to the SH7263 or SH7203 with a 16-bit data-bus width.
- The bus state controller (BSC) of the SH7263 or SH7203 is used to set up conditions for the execution of read and write operations for an external NOR flash memory.

## 1.1 Module Used

- Bus state controller (BSC)

## 1.2 Applicable Conditions

- Microcontroller: SH7263/SH7203 (R5S72630/R5S72030) Groups
- Flash memory: 32-Mbit product S29GL032A** (2 Mwords × 16 bits) from Spansion™
  64-Mbit product S29GL064A** (4 Mwords × 16 bits) from Spansion™
  128-Mbit product S29GL128N** (8 Mwords × 16 bits) from Spansion™
- Operating frequencies: Internal clock 200 MHz
  Bus clock 66.67 MHz

## 1.3 Related Application Notes

The operation of the reference program for this document was confirmed with the setting conditions described in the *SH7263/SH7203 Group Hardware Manual*. Please refer to the hardware manual with this application note.

# 2. Description of Sample Application

## 2.1 Operational Overview of Module Used

The BSC of the SH7263/SH7203 is used to control externally connected NOR flash memory. Table 1 gives specifications of the NOR flash memory used in this sample program.

**Table 1 Specifications of NOR Flash Memory for the SH7263/SH7203**

| Item | Description | | |
|---|---|---|---|
| Type no. | S29GL032A**<br>(from Spansion™) | S29GL064A**<br>(from Spansion™) | S29GL128N**<br>(from Spansion™) |
| Configuration<br>(Max. byte per area: 64 M) | 4 MB<br>(2 Mwords × 16 bits × 1) | 8 MB<br>(4 Mwords × 16 bits × 1) | 16 MB<br>(8 Mwords × 16 bits × 1) |
| Data bus width | 16 bits | | |
| Access time | In random access: 90 ns (max.)<br>In page reading: 25 ns (max.) | | |
| Boot block | Top-boot and bottom-boot devices identified by the model no. | | |

Figure 1 shows a memory map. Type of memory to be connected and data-bus width are specified by individual CS space. In this sample program, NOR flash memory is connected to the CS0 space.

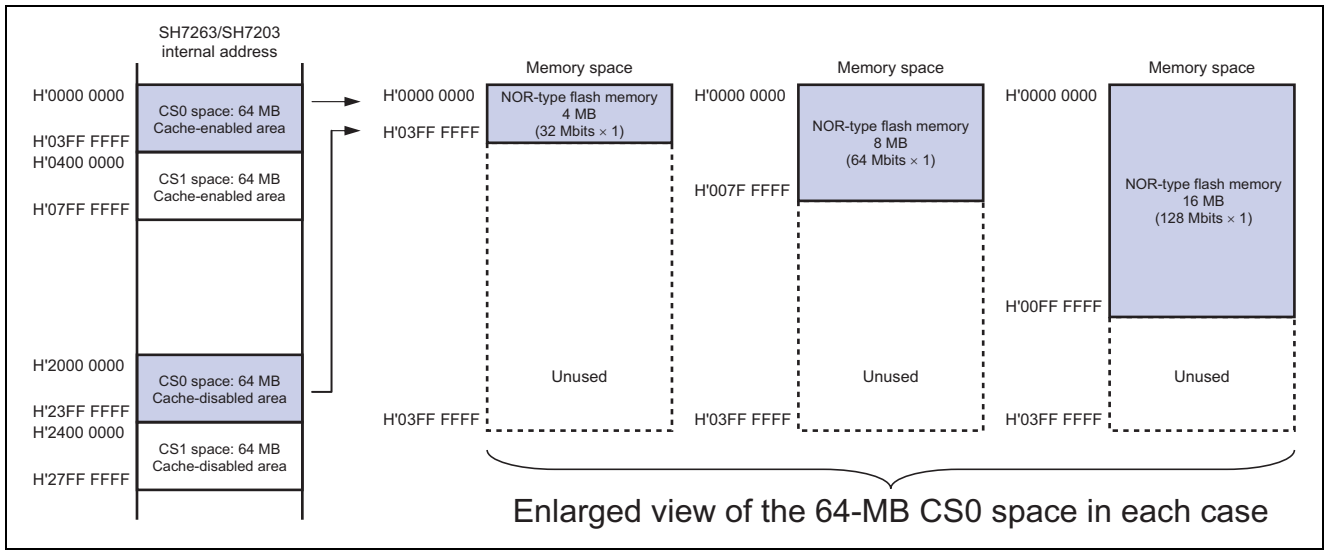


**Figure 1 Memory Map (32-/64-/128-Mbit Product)**

Figures 3, 4, and 5 show examples of circuits used to connect NOR flash memory.

SH7263/SH7203 is connected to NOR flash memory with a 16-bit data bus width. To set up NOR flash memory with a data-bus width of 16 bits, the $\overline{\text{BYTE}}$ pin is fixed to the high level. To set up space CS0 of the SH7263/SH7203 for the same bus width, the MD pin is fixed to the low level.

Note: Endian
The SH 7263/SH7203 supports both big endian, in which the most significant byte (MSB) of data is that in the direction of the 0th address, and little endian, in which the least significant byte (LSB) is that in the direction of the 0th address. In the initial state after a power-on reset, all areas will be in big endian mode. Little endian cannot be selected for area 0. However, the endian of areas 1 to 7 can be changed by the setting in the CSnBCR register setting as long as the target space is not being accessed.

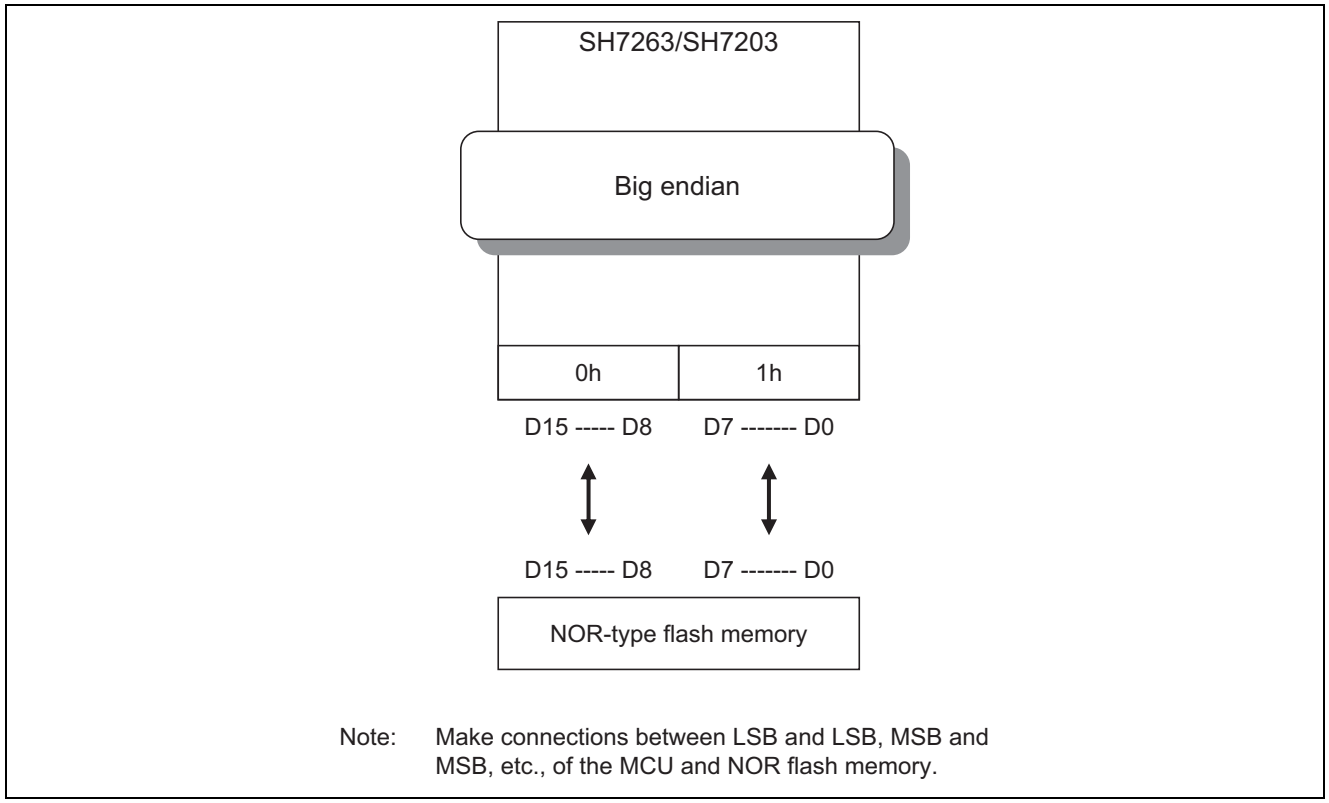


**Figure 2 Example of Connection between the SH7263/SH7203 and NOR Flash Memory over a 16-Bit Data Bus**

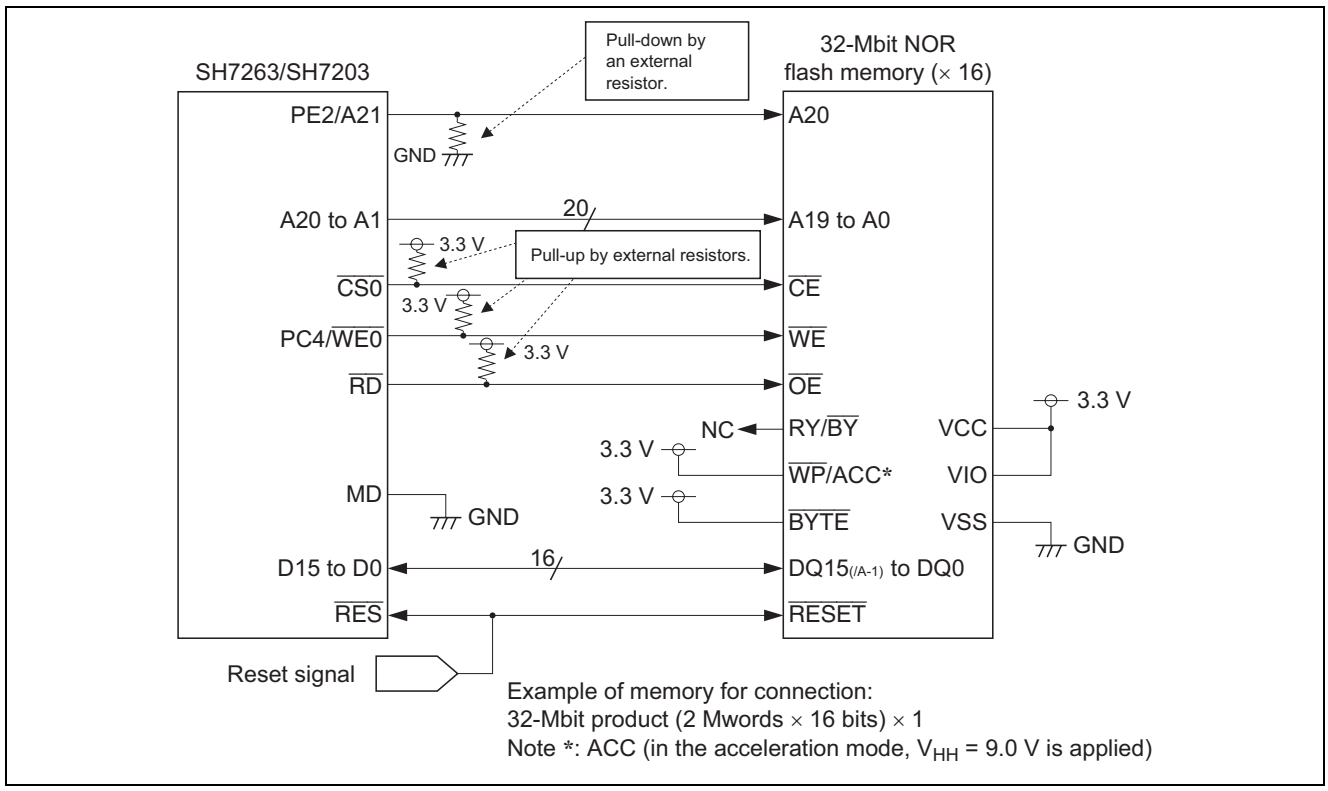


**Figure 3 Circuit Example 1 for Flash Memory Connection (32-Mbit Product/4 MB, 16-Bit Bus)**

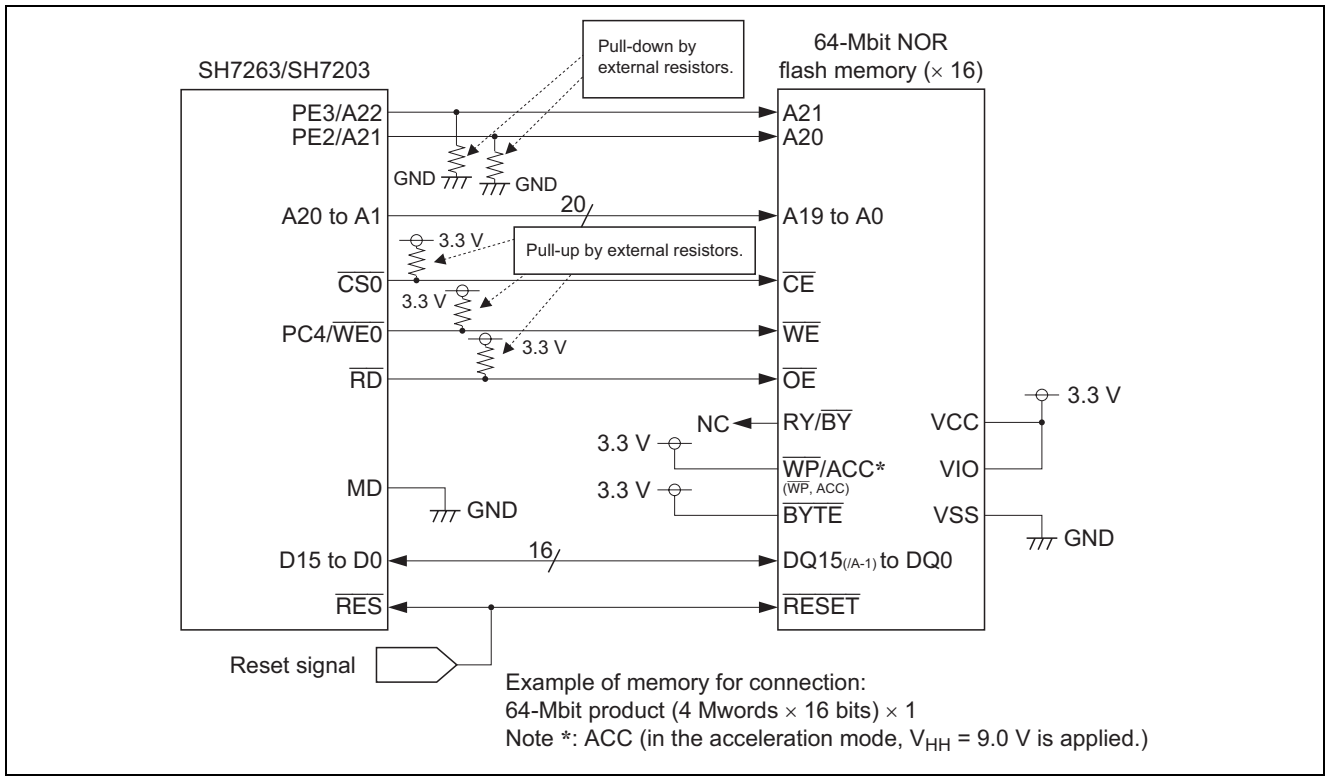


**Figure 4 Circuit Example 2 for Flash Memory Connection (64-Mbit Product/8 MB, 16-Bit Bus)**

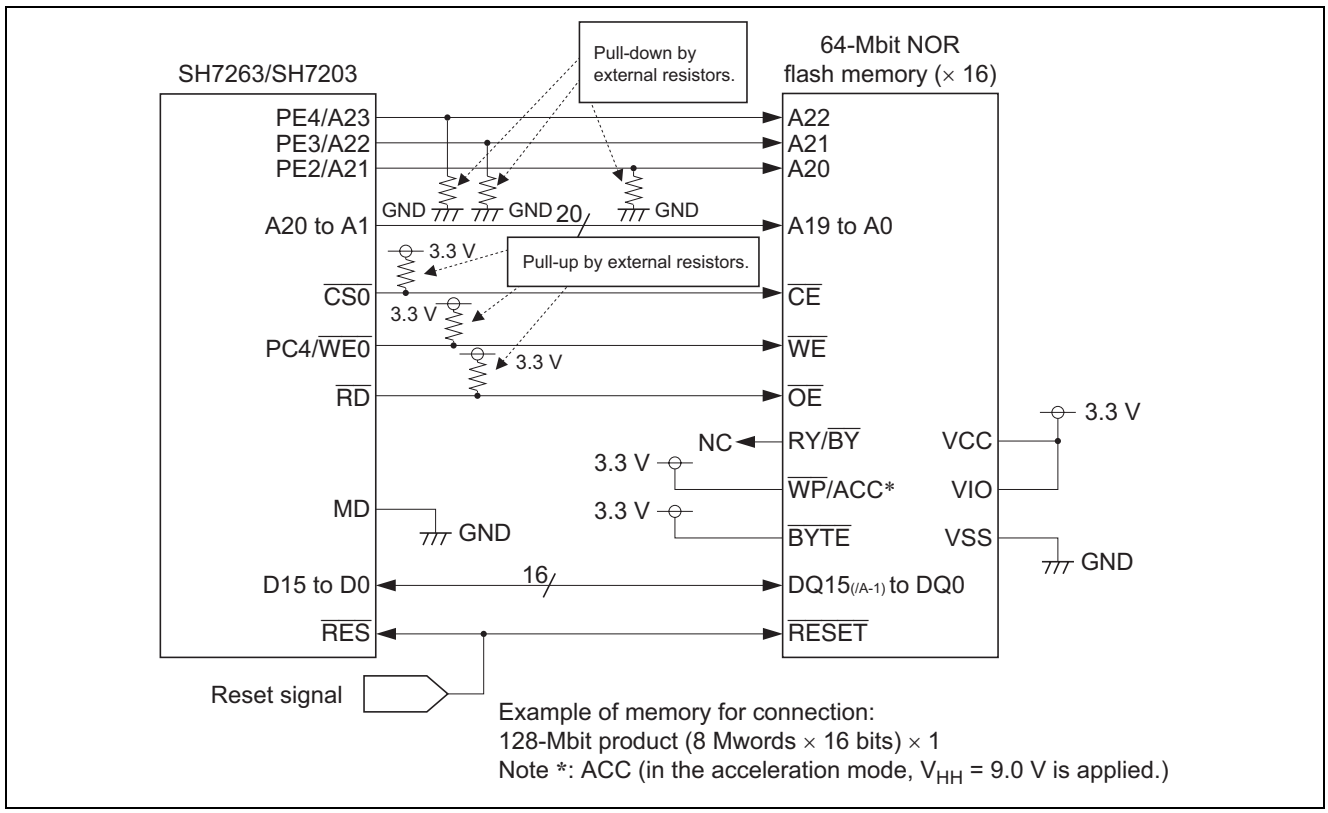


**Figure 5 Circuit Example 3 for Flash Memory Connection (128-Mbit Product/16 MB, 16-Bit Bus)**

Table 2 gives a list of pin functions of the SH7263/SH7203. Since pins A21, A22, A23, and $\overline{WE0}$ are initially set for operation as I/O pins, the pin-function controller (PFC) must be used to switch the pin functions.

When a boot program is executed from the NOR flash memory connected to space CS0, the I/O pins of the MCU are in their initial state (operating as input pins), the states of the pins are not fixed so can become undefined and have an adverse effect on the memory. Thus, to ensure correct reading of the specified addresses in space CS0, pins A21, A22, and A23 must be pulled down to the low level by an external resistor. We also recommend the use of external resistors to apply pull-up processing and thus stabilize the operation of control signals ($\overline{CS0}$, $\overline{WE0}$, and $\overline{RD}$).

**Table 2 List of Pin Functions for the SH7263/SH7203**

| SH7263 Pin | I/O | Initial Pin Function | Function in the Circuit Example |
|---|---|---|---|
| A23 | Output | I/O pin (PE4) | Address bus (for connection of the 128-Mbit product) |
| A22 | Output | I/O pin (PE3) | Address bus (for connection of the 64- or 128-Mbit product) |
| A21 | Output | I/O pin (PE2) | Address bus (for connection of the 32-, 64-, or 128-Mbit product) |
| A20 to A1 | Output | A20 to A1 | Address bus |
| D15 to D0 | Input/output | D15 to D0 | Data bus |
| $\overline{RD}$ | Output | $\overline{RD}$ | Read pulse signal (read data out enable signal) |
| $\overline{WE0}$ | Output | I/O pin (PC4) | Indicates byte write on D15 to D0 |
| $\overline{CS0}$ | Output | $\overline{CS0}$ | Chip selection |
| $\overline{MD}$ | Input | MD | Selects initial values for the CS0 space data-bus width and CS1 to CS7 space data-bus widths. The CS0 space data-bus width cannot be changed after a power-on reset.<br>**MD** / **Data-bus width**<br>1 / 32 bits<br>0 / 16 bits (set value in the sample program) |

## 2.2 Procedure for Setting Modules Used

NOR flash memory is read by either of two methods: ① random-access reading and ② page reading. The bus-state controller settings for the two methods are different. The procedures for settings in both methods are described in this section.

Some devices may not support page reading. Furthermore, page reading is also divided into two types, clock synchronous and asynchronous. This application note describes page reading of the asynchronous type.

### 2.2.1 Procedure for Settings to Use Random-Access Reading

Random-access reading can be used in spaces CS0 to CS7. The TYPE[2:0] bits of the bus control register (CSnBCR, n = 0 to 7) of the space in use are set to "Normal space (B'000)".

Table 3 gives a list of examples for setting the bus state controller with space CS0 in use. For details on the individual registers, see the section on the bus state controller in the *SH7263/ SH7203 Group Hardware Manual*.

Figure 6 shows an example of the procedure for setting the bus state controller.

**Table 3 Example of Bus State Controller Settings (1)**

| Name of Register | Address | Setting | Function |
|---|---|---|---|
| CS0 space bus control register (CS0BCR) | H'FFFC 0004 | H'2000 0400 | • IWW[2:0] = B'010<br>Idle period between writing and reading and between writing and writing: 2 cycles<br>Settings should be made to these bits between writing and writing so as to satisfy the standards for tWPH of NOR flash memory.<br>• TYPE[2:0] = B'000<br>These bits set the type of memory connected to a space.<br>: Normal space<br>[Note]<br>Writing to the BSZ[1:0] bits (data-bus width specification) in this register is ignored. The MD pin should be used to specify the data-bus width of space CS0.<br>Note that settings of bits other than those stated above are not required. Bits other than above should remain in their initial settings. |
| CS0 space wait control register (CS0WCR) | H'FFFC 0028 | H'0000 0B41 | • SW[1:0] = B'01<br>Number of delay cycles from address and $\overline{CS0}$ assertion to $\overline{RD}$ and $\overline{WE}$ assertion: 1.5<br>• WR[3:0] = B'0110<br>Read access wait cycles: 6<br>• WM = B'1<br>External wait input is ignored<br>• HW[1:0] = B'01<br>Delay cycles from $\overline{RD}$ and $\overline{Wn}$ negation to address and $\overline{CS0}$ negation: 1.5 |

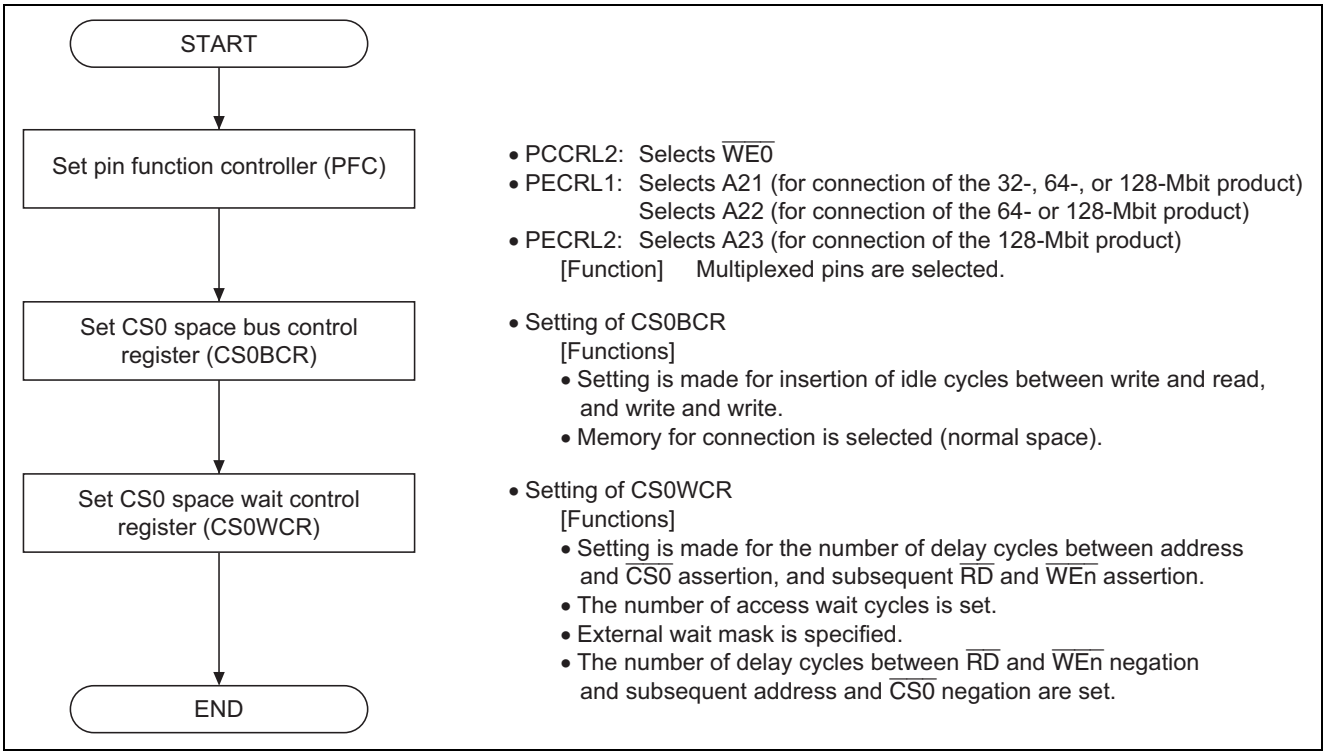


**Figure 6 Example 1 of Procedure for Setting Bus State Controller (CS0 Space)**

### 2.2.2 Procedure for Settings to Use Page Reading

Page reading (in asynchronous) can be used for spaces CS0 and CS4. Set the TYPE[2:0] bits of the bus control register (CSnBCR, n = 0 or 4) for the space in use to "Burst ROM (B'001)". To connect burst ROM to the CS0 space, set the TYPE[2:0] bits to burst ROM after changing the settings of the CS0WCR register to those required for the burst ROM in use.

Table 4 gives a list of examples for setting the bus state controller when the CS0 space is in use. For details on individual registers, see the chapter on the bus state controller described in the *SH7263/SH7203 Group Hardware Manual*.

Figure 7 shows an example of the procedure for setting the bus state controller.

**Table 4 Example 2 for Setting Bus State Controller**

| Name of Register | Address | Setting | Function |
|---|---|---|---|
| CS0 space bus control register (CS0BCR) | H'FFFC 0004 | H'2000 1400 | • IWW[2:0] = B'010<br>Idle period between writing and reading and between writing and writing: 2 cycles<br>Settings should be made to these bits between writing and writing so as to satisfy standard of tWPH of NOR flash memory.<br>• TYPE[2:0] = B'001<br>These bits set the type of memory connected to a space.<br>: Burst ROM (clock asynchronous)<br>[Note]<br>Writing to the BSZ[1:0] bits (data-bus width specification) in this register is ignored. The MD pin should be used to specify the data-bus width of space CS0.<br>Note that settings of bits other than those stated above are not required. Other bits should remain their initial settings. |
| CS0 space wait control register (CS0WCR) | H'FFFC 0028 | H'0013 03C0 | • BST[1:0] = B'01<br>Burst count specification:<br>2 burst × four times<br>• BW[1:0] = B'11<br>Burst wait cycles: 3<br>• W[3:0] = B'0111<br>Access wait cycles: 8<br>• WM = B'1<br>External wait input is ignored |

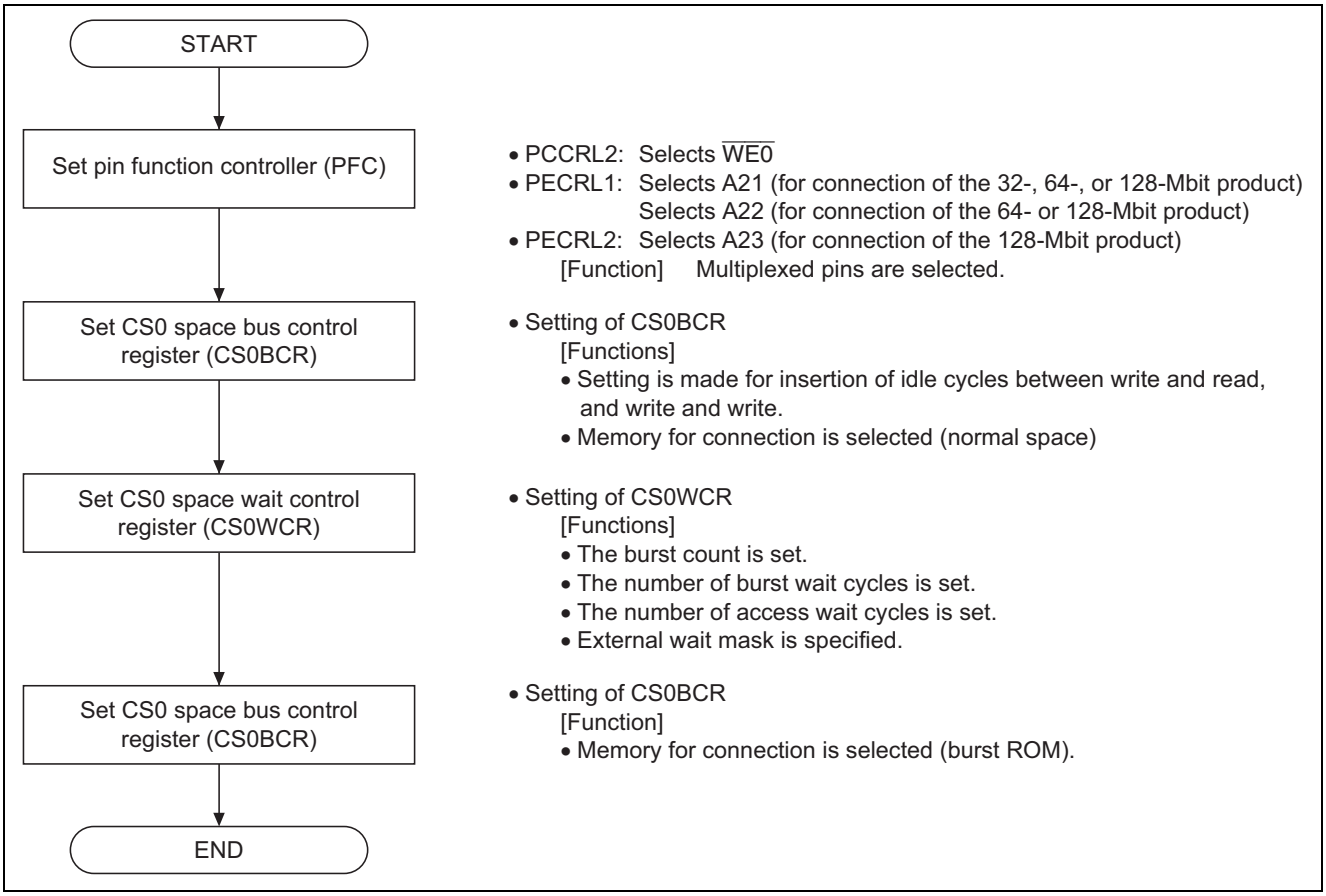


**Figure 7 Example 2 of Procedure for Setting Bus State Controller (CS0 Space)**

## 2.3 Settings of NOR Flash Memory Timing in Sample Program

To connect NOR flash memory, the number of wait cycles that corresponds to the access speed of the flash memory in use must be set. This section describes the main points regarding the settings in the sample program for the cases of random-access reading and page reading.

In this sample program, the bus clock for the SH7263/SH7203 is set to 66.67 MHz (tcyc = 15 ns).

For AC characteristics of NOR flash memory and the SH7263/SH7203, refer to the datasheets of the individual devices.

### 2.3.1 Reference Examples for Setting Flash Memory with Random-Access Reading in Use (Space CS0)

1. Extension of CSn assertion period
   A. Cycles of delay from address and $\overline{CS0}$ assertion to $\overline{RD}$ and $\overline{WE0}$ assertion (Th)
   Confirm that tCS (chip enable setup time) for the NOR flash memory in use is satisfied. In this sample program, the number of cycles of delay (Th) is the setting of the SW bits in the CS0 space wait control register (CS0WCR) minus 0.5 cycles (Th = SW – 0.5 cycles). In the following reference example, the setting is for Th = 1.0.

$$tCS(min) \leq \underbrace{tCS\_min}_{P20} \quad \text{.....(figure 10)}$$

   B. Cycles of delay from $\overline{RD}$ and $\overline{WE0}$ negation to address and $\overline{CS0}$ negation (Tf)
   Confirm that tAH (address hold time) for the NOR flash memory in use is satisfied. In this sample program, the number of cycles of delay (Tf) is the setting of the HW bits in the CS0 space wait control register (CS0WCR) minus 0.5 cycles (Tf = HW – 0.5 cycles). In the following reference example, the setting is for Tf = 1.0.

$$tAH(min) \leq \underbrace{(T1 - tWED1\_max)}_{P14} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2)}_{P16} + \underbrace{(tcyc \times Tf)}_{P17} + \underbrace{(tAD1\_min)}_{P18} \quad \text{.....(figure 10)}$$

2. Access wait cycles
   Cycles to wait (Tw) between T1 and T2 cycles.
   With this setting, confirm that bus timing requirements of the SH7263/SH7203 and NOR flash memory that is in use are satisfied. In this reference example, the setting is for one wait cycle (Tw = 1).
   Additionally, T1 and T2 used in the following formula are tcyc.

   tRC (read cycle time) of NOR flash memory.....(figure 8)

$$tRC(min) \leq \underbrace{(tcyc \times Th - tCSD1\_max)}_{P5} + \underbrace{(T1)}_{P2} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2 - tRDS1\_min)}_{P4}$$

Note: The applicable condition was originally tRC (min) ≤ tcyc × Th + T1 + tcyc × Tw + T2 + tcyc × Tf. In this sample program, however, we apply tRC = tCE to take as the strictest condition.

- tACC of NOR flash memory (address access time) ..... (figure 8)

  $tACC(max) \leq \underbrace{(tcyc \times Th - tAD1\_max)}_{P1} + \underbrace{(T1)}_{P2} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2 - tRDS1\_min)}_{P4}$

- tCE of NOR flash memory ($\overline{CE}$ access time) ..... (figure 8)

  $tCE(max) \leq \underbrace{(tcyc \times Th - tCSD1\_max)}_{P5} + \underbrace{(T1)}_{P2} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2 - tRDS1\_min)}_{P4}$

- tOE of NOR flash memory ($\overline{OE}$ access time) ..... (figure 8)

  $tOE(max) \leq \underbrace{(T1 - tRSD\_max)}_{P6} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2 - tRDS1\_min)}_{P4}$

- tOH of NOR flash memory (retention time from data output in the previous-cycle) ..... (figure 8)

  $tOH(min) \leq tRDH1(min)$

- tWC of NOR flash memory (write cycle time) ..... (figure 9)

  $tWC(min) \leq \underbrace{(tcyc \times Th - tAD1\_max)}_{P1} + \underbrace{(T1)}_{P2} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(T2)}_{P16} + \underbrace{(tcyc \times Tf)}_{P17} + \underbrace{(tAD1\_min)}_{P18}$

- tAS of NOR flash memory (address setup time) ..... (figure 9)

  $tAS(min) \leq \underbrace{tAS\_min}_{P19}$

- tWP of NOR flash memory (write pulse width) ..... (figure 10)

  $tWP(min) \leq \underbrace{(T1 - tWED1\_max)}_{P14} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(tWED1\_min)}_{P8}$

- tDS of NOR flash memory (data setup time) ..... (figure 9)

  $tDS(min) \leq \underbrace{(tcyc \times Th - tWDD1\_max)}_{P9} + \underbrace{(T1)}_{P2} + \underbrace{(tcyc \times Tw)}_{P3} + \underbrace{(tWED1\_min)}_{P8}$

- tDH of NOR flash memory (data hold time) ..... (figure 9)

  $tDH(min) \leq \underbrace{tWDH4\_min}_{P12}$

3. Wait between cycles of access

   This setting is for the insertion of a wait between consecutive cycles of access.

   Ensure that this setting satisfies tWPH ("H" write pulse width) for the target NOR flash memory. In this reference example, the number of cycles between writing and reading, and writing and writing, is one.

   $tWPH(min) \leq \underbrace{(T2 - tWED1\_max)}_{P10} + \underbrace{(tcyc \times Tf)}_{P11} + \underbrace{(tcyc \times Taw)}_{P14} + \underbrace{(tcyc \times Th)}_{P15} + \underbrace{(tWED1\_min)}_{P13}$ (figure 11)

Figure 8 shows read timing 1 for NOR flash memory (1).

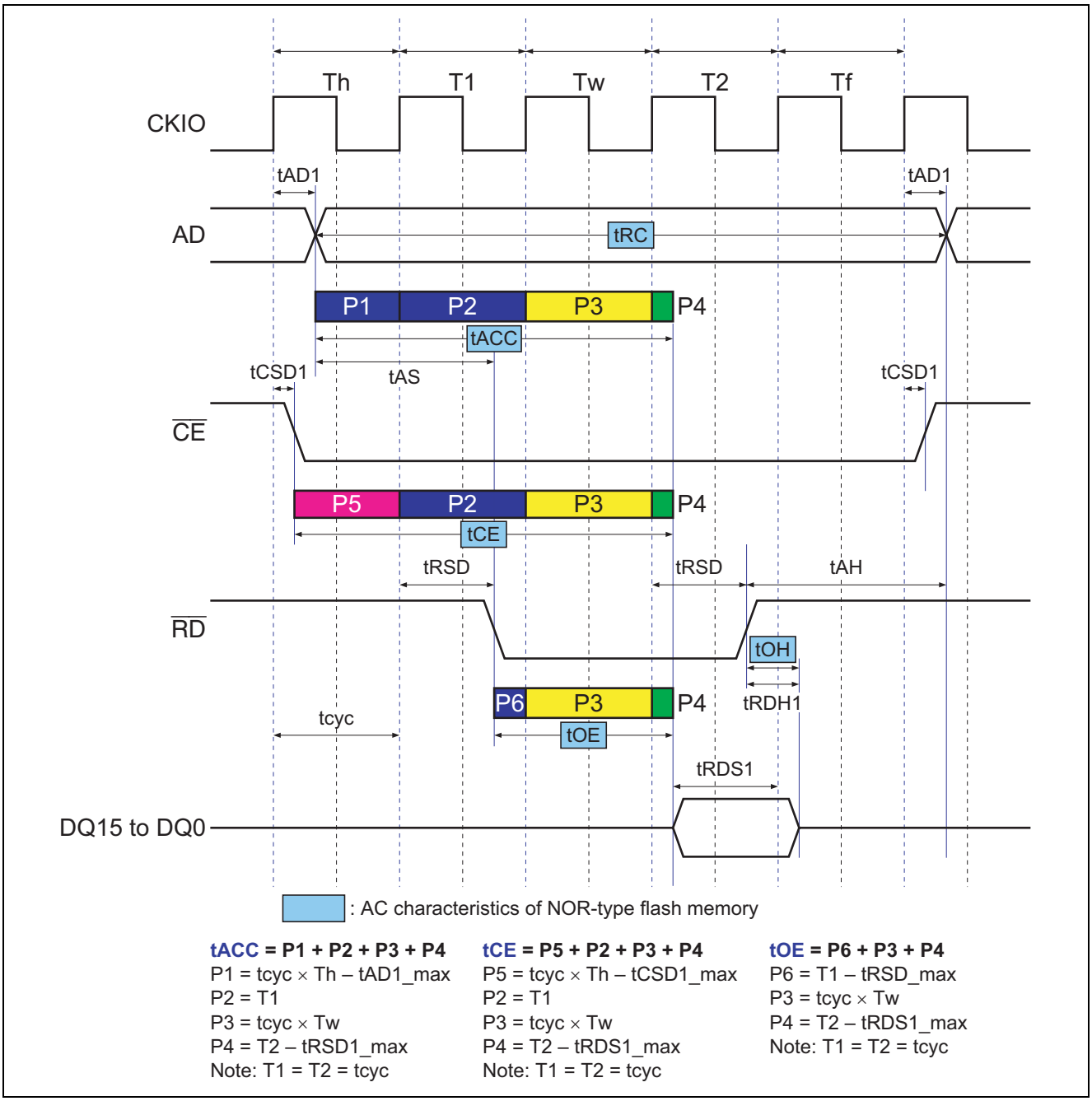


**Figure 8 Read Timing for NOR Flash Memory When SW = 1, WR = 1, and HW = 1 (1)**

Figure 9 shows write timing 1 for NOR flash memory (1).

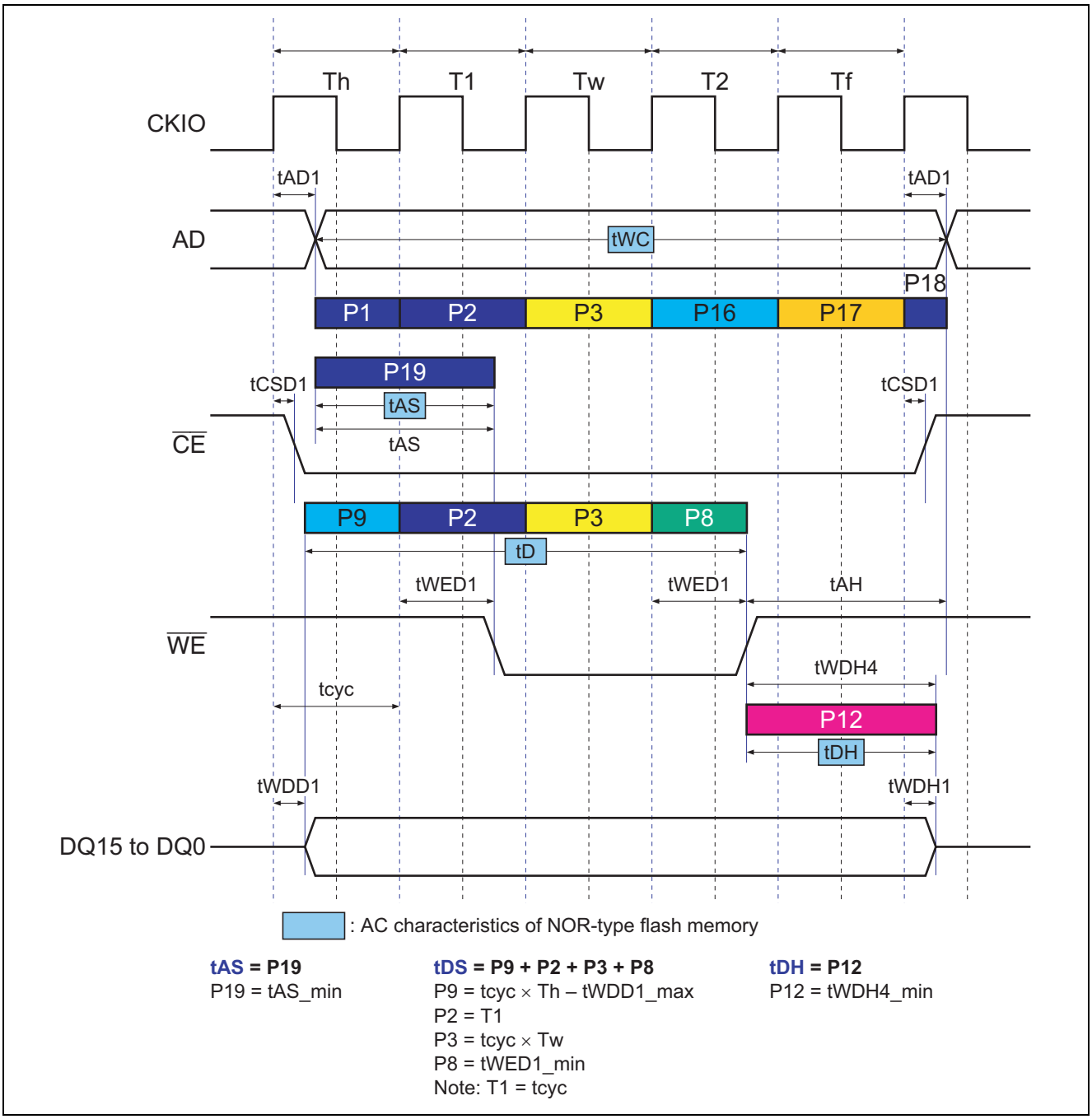


**Figure 9 Write Timing for NOR Flash Memory When SW = 1, WR = 1, and HW = 1 (1)**

Figure 10 shows write timing for NOR flash memory (2).

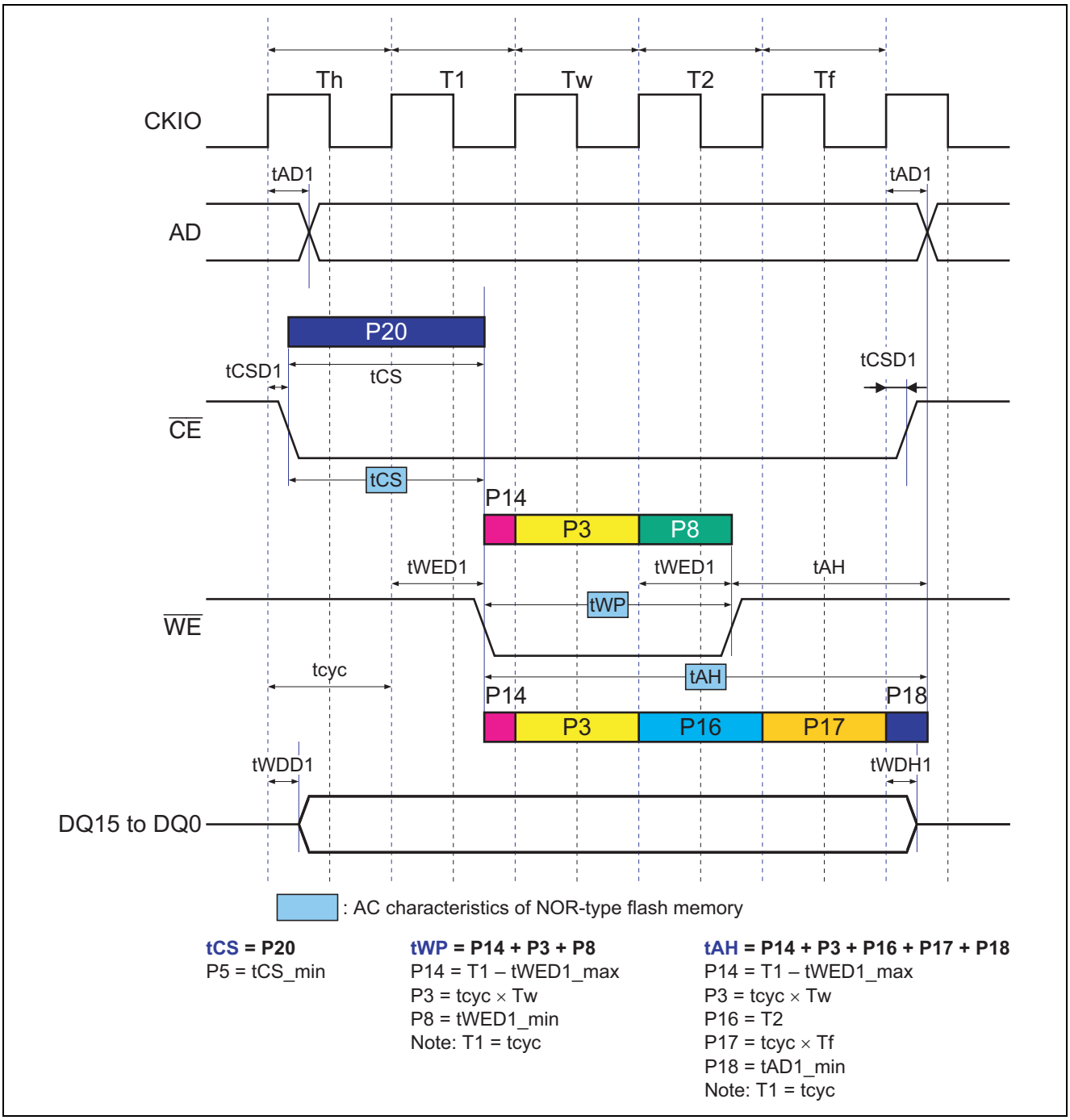


**Figure 10 Write Timing for NOR Flash Memory When SW = 1, WR = 1, and HW = 1 (2)**

Figure 11 shows write timing for NOR flash memory (3).

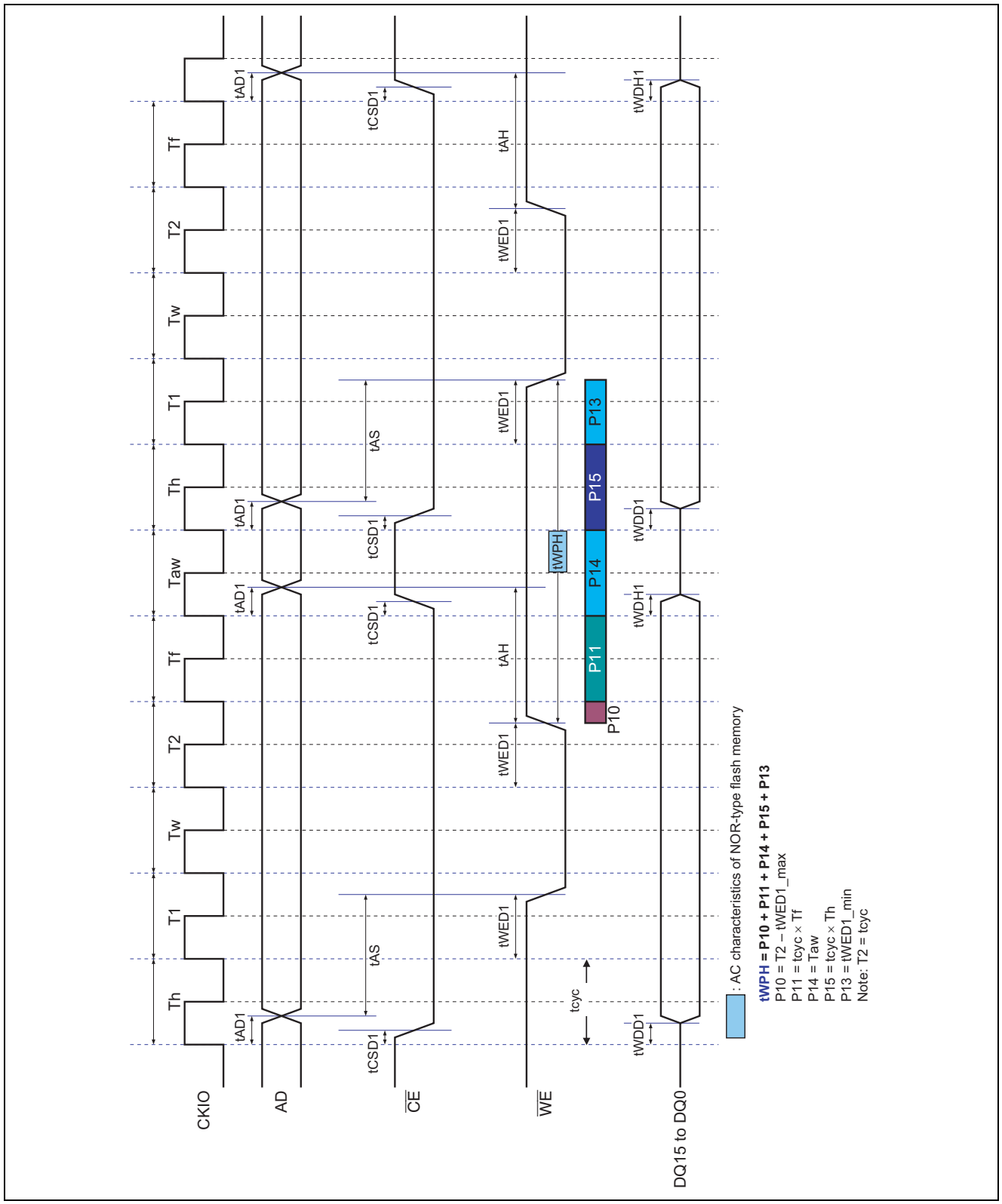


**Figure 11 Write Timing for NOR Flash Memory When SW = 1, WR = 1, HW = 1, and Taw = 1 (3)**

### 2.3.2 Reference Examples for Setting Flash Memory with Page Reading in Use (Space CS0)

1. Extension of CSn assert period

   For page reading in the CS0 space, extension of CSn assert period cannot be set. Therefore, both of the following numbers of cycles of delay are set to 0.5 (fixed): ① cycles of delay from address and $\overline{CS0}$ assertion to $\overline{RD}$ and $\overline{WE0}$ assertion (Th), and ② cycles of delay from $\overline{RD}$ and $\overline{WE0}$ negation to address and $\overline{CS0}$ negation (Tf).

   In this sample program, settings for numbers of cycles of delay (Th) and (Tf) are the number of cycles minus (fixed) (Th = Tf = 0.5 – 0.5 = 0 cycle). In the following reference example, the setting is Th = Tf = 0.0.

   Ensure that the settings satisfy tCS (chip enable setup time) and tAH (address hold time) requirements for the NOR flash memory that is in use.

   $$tCS(min) \leq \underbrace{tCS\_min}_{PB13}$$ ..... (figure 14)

   $$tAH(min) \leq \underbrace{(T1 - tWED1\_max)}_{PB14} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2)}_{PB18} + \underbrace{(tAD1\_min)}_{PB19}$$ ..... (figure 14)

2. Access wait cycles

   Set wait cycles (Tw) which are inserted into the first access cycles.

   Ensure that this setting satisfies the bus-timing requirements of the SH7263/SH7203 and the NOR flash memory that is in use. In the following reference example, one wait cycle (Tw = 1) is set.

   Furthermore, T1 and T2B used in the following formulae are tcyc.

- tRC of NOR flash memory (read cycle time) ..... (figure 12)

  $$tRC(min) \leq \underbrace{(T1 - tCSD1\_max)}_{PB4} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2B - tRDS3\_min)}_{PB3}$$

Note: Because the page read does not have standard of tRC originally, tRC = tCE has been applied for the first time access cycles.

- tACC of NOR flash memory (access-access time) ..... (figure 12)

  $$tACC(max) \leq \underbrace{(T1 - tAD1\_max)}_{PB1} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2B - tRDS3\_min)}_{PB3}$$

- tCE of NOR flash memory ($\overline{CE}$ access time) ..... (figure 12)

  $$tCE(max) \leq \underbrace{(T1 - tCSD1\_max)}_{PB4} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2B - tRDS3\_min)}_{PB3}$$

- tOE of NOR flash memory ($\overline{OE}$ access time) ..... (figure 12)

  $$tOE(max) \leq \underbrace{(T1 - tRSD\_max)}_{PB5} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2B - tRDS3\_min)}_{PB3}$$

- tPACC of NOR flash memory (page access time/the second and subsequent access cycles) ..... (figure 12)

  $$tPACC(max) \leq \underbrace{(T2B - tAD2\_max)}_{PB6} + \underbrace{(tcyc \times Twb)}_{PB7} + \underbrace{(T2B - tRDS3\_min)}_{PB8}$$

- tOH of NOR flash memory (retention time for previous cycle data output) ..... (figure 12)

  $$tOH(min) \leq tRDH3(min)$$

- tWC of NOR flash memory (write cycle time) ..... (figure 13)

  $$tWC(min) \leq \underbrace{(T1 - tAD1\_max)}_{PB1} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(T2)}_{PB18} + \underbrace{(tAD1\_min)}_{PB19}$$

- tAS of NOR flash memory (address setup time) ..... (figure 13)

$$tAS(min) \leq \underbrace{tAS\_min}_{PB17}$$

- tWP of NOR flash memory (write pulse width) ..... (figure 14)

$$tWP(min) \leq \underbrace{(T1 - tWED1\_max)}_{PB14} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(tWED1\_min)}_{PB9}$$

- tDS of NOR flash memory (data setup time) ..... (figure 13)

$$tDS(min) \leq \underbrace{(T1 - tWDD1\_max)}_{PB10} + \underbrace{(tcyc \times Tw)}_{PB2} + \underbrace{(tWED1\_min)}_{PB9}$$

- tDH of NOR flash memory (data hold time) ..... (figure 13)

$$tDH(min) \leq \underbrace{tWDH4\_min}_{PB12}$$

3. Wait between access cycles
   This setting is for the insertion of waiting time between consecutive cycles of access.
   With this setting, confirm that tWPH ("H" write pulse width) of the target NOR flash memory is satisfied. In this reference example, one cycle (Taw = 1) is set as wait cycles between writing and reading, and writing and writing.

$$tWPH(min) \leq \underbrace{(T2 - tWED1\_max)}_{PB11} + \underbrace{(tcyc \times Taw)}_{PB15} + \underbrace{(tWED1\_min)}_{PB16}$$

..... (figure 15)

Figure 12 shows page read timing for NOR flash memory (1).

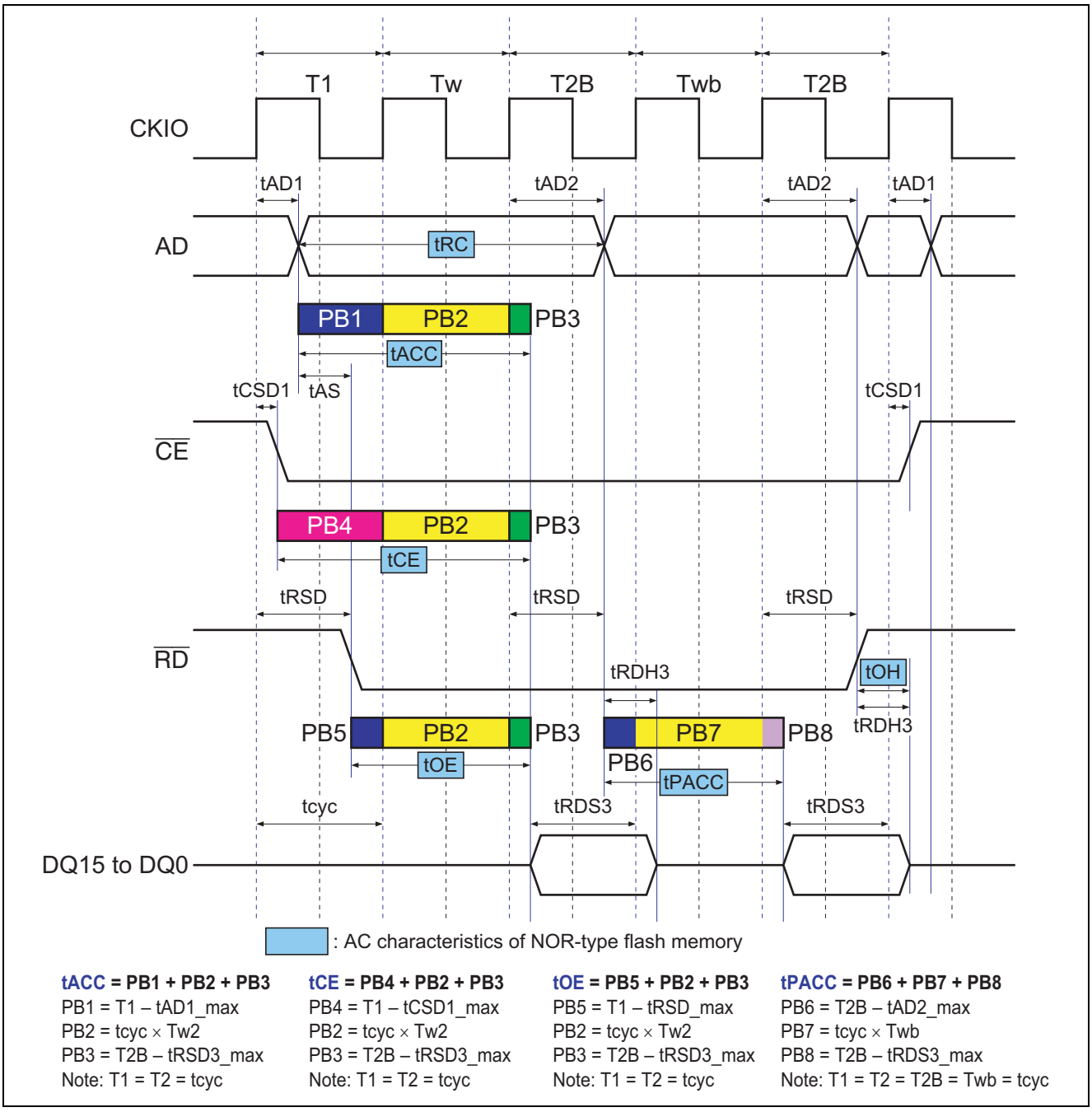


**Figure 12 Page Read Timing for NOR Flash Memory When W = 1, BW = 1, and BST = 2 (1)**

Figure 13 shows write timing for NOR flash memory (4).

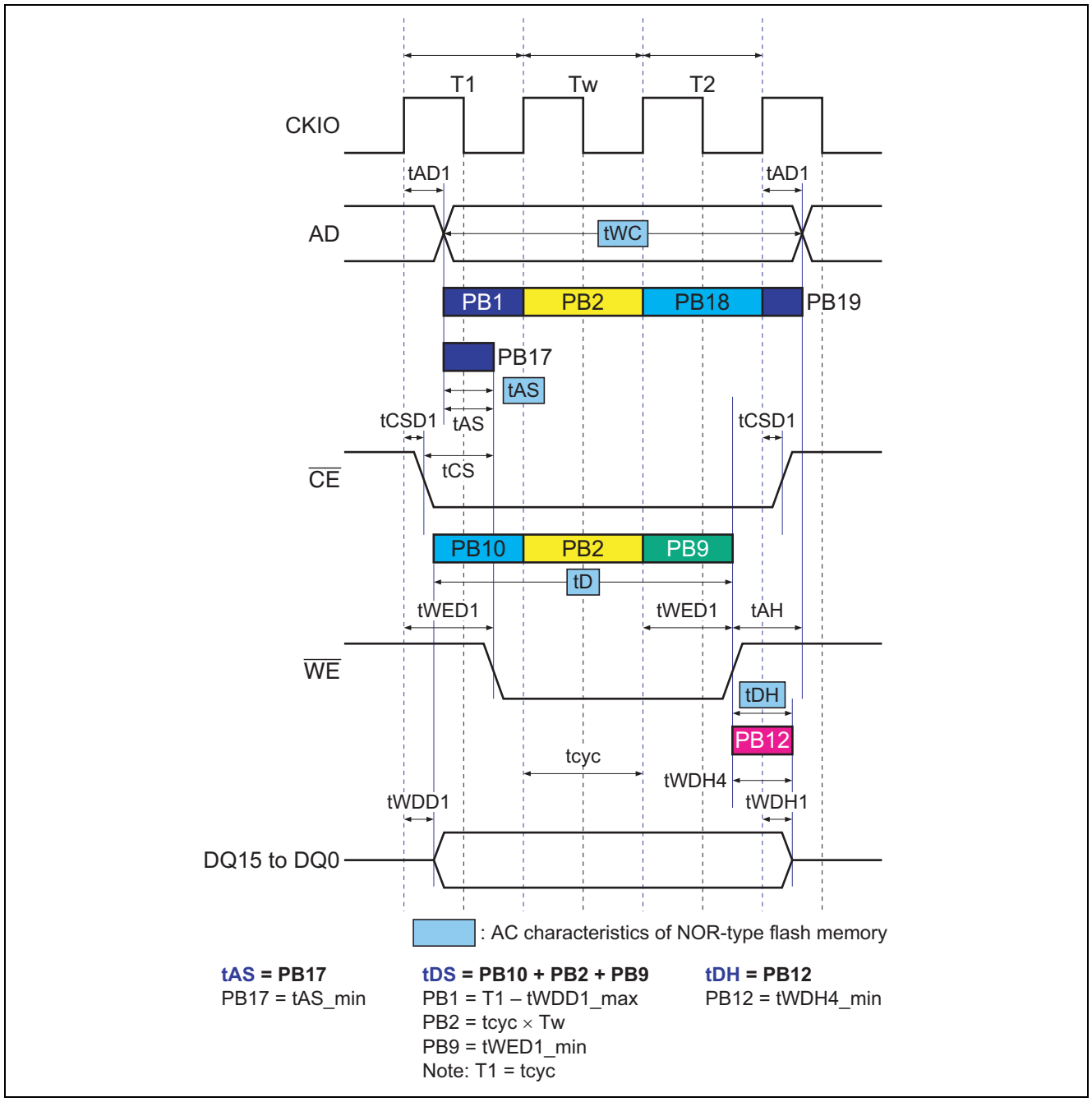


**Figure 13 Write Timing of NOR Flash Memory When W = 1 (4)**

Figure 14 shows write timing for NOR flash memory (5).

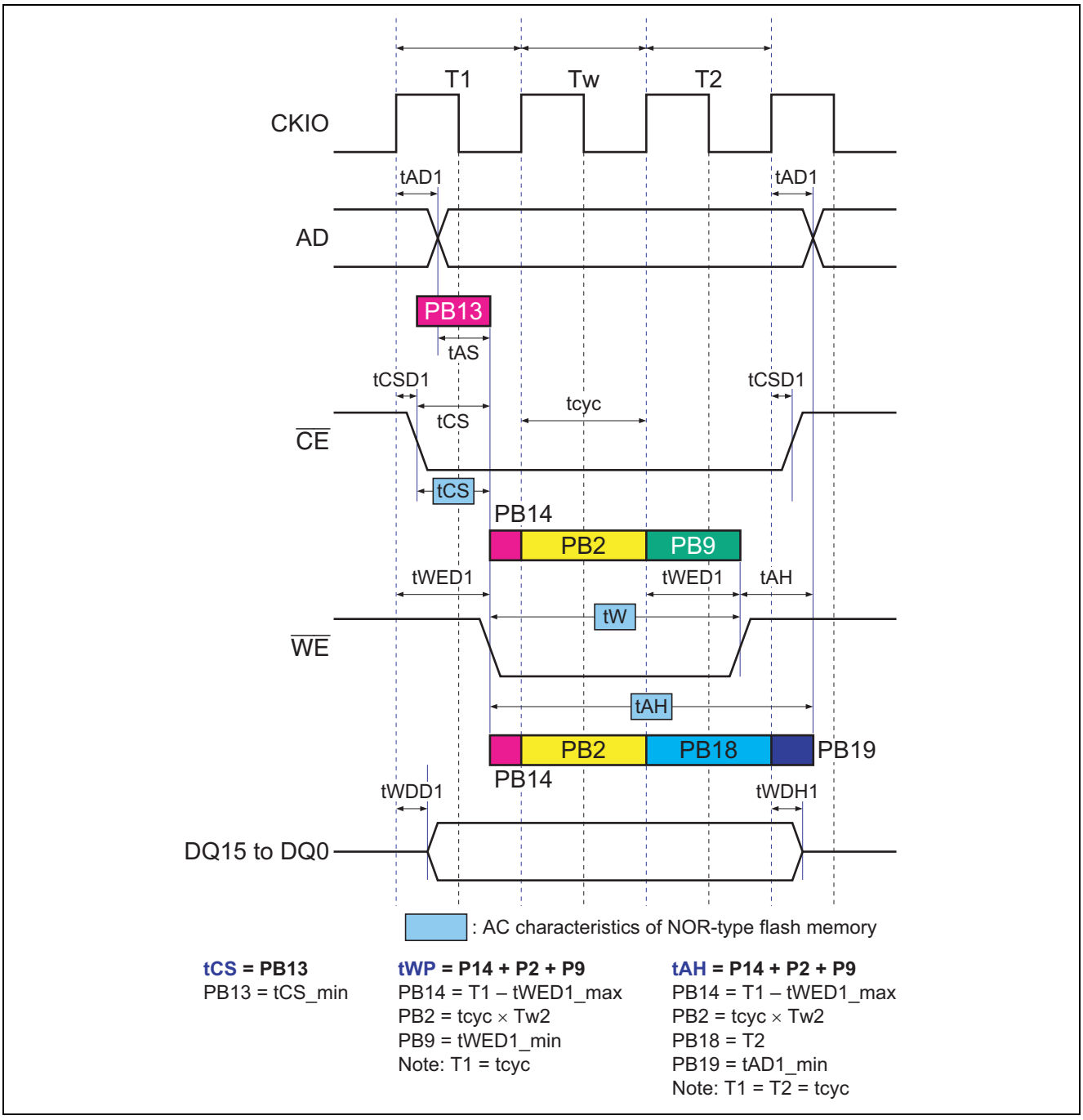


**Figure 14 Write Timing of NOR Flash Memory When W = 1 (5)**

Figure 15 shows write timing for NOR flash memory (6).

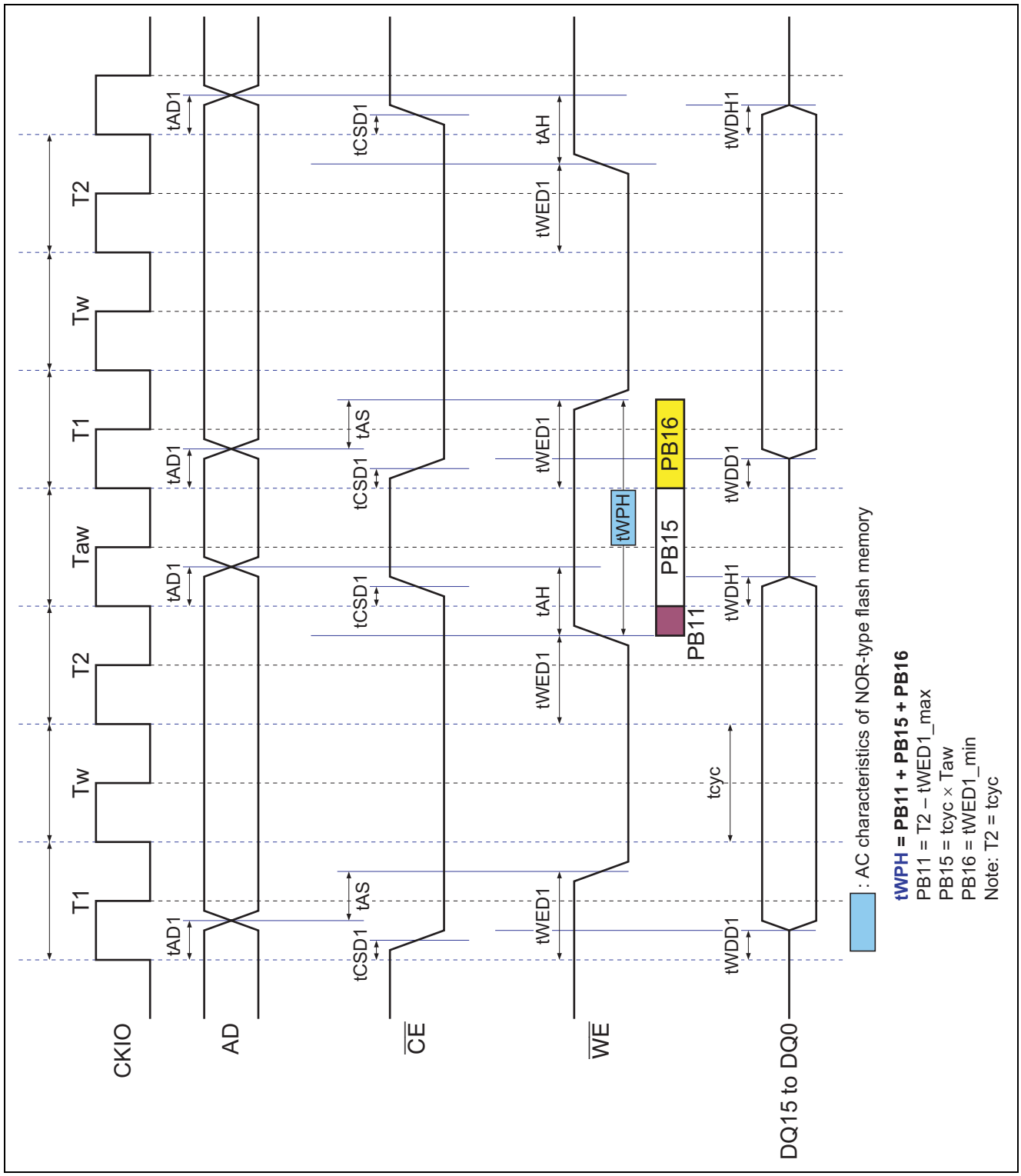


**Figure 15 Write Timing of NOR Flash Memory When W = 1 and Taw = 1 (6)**

[Reference]
Figure 16 shows page read timing for NOR flash memory (2).

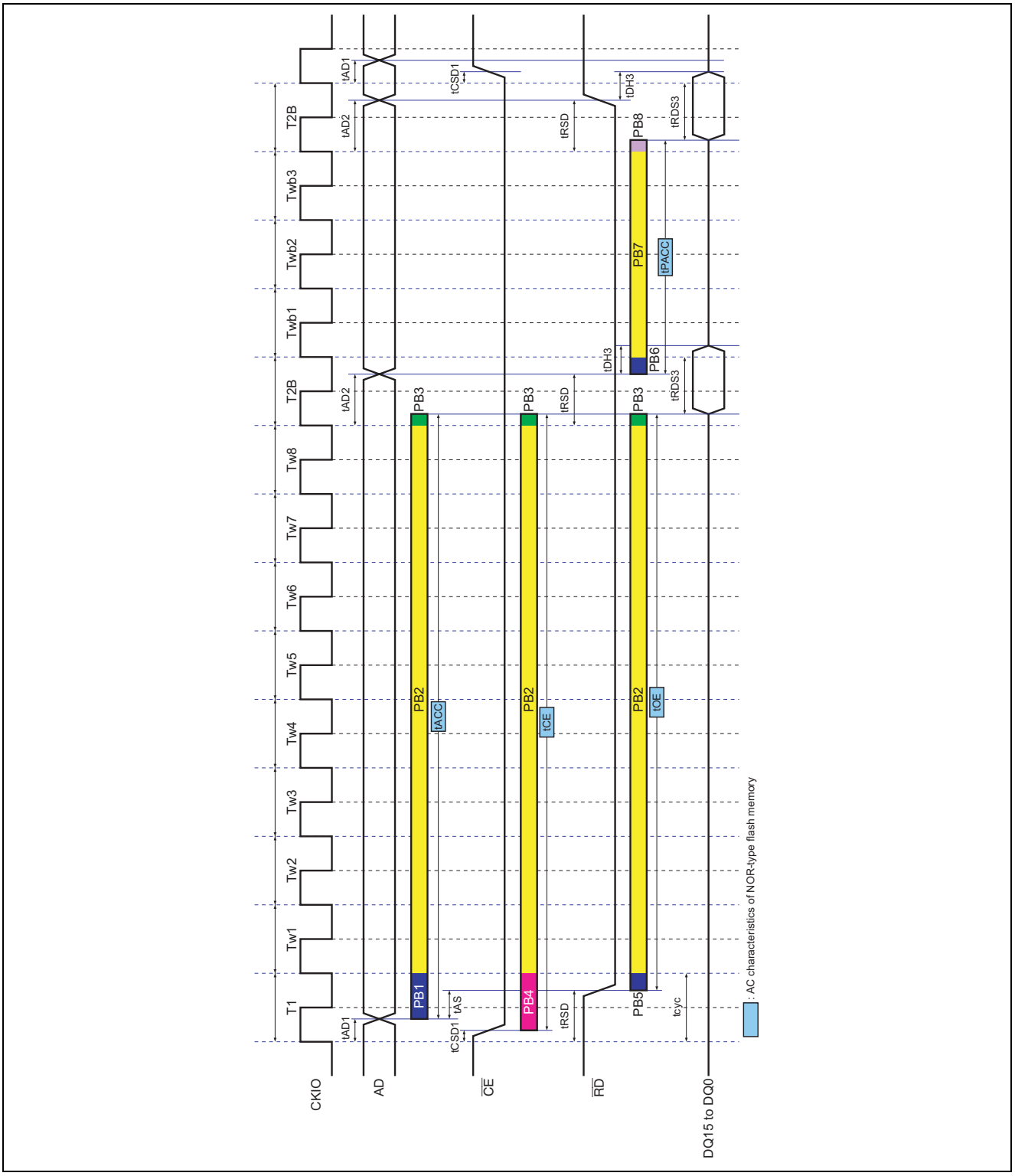


**Figure 16 Page Read Timing of NOR Flash Memory When W = 8, BW = 3, and BST = 2 (2)**

## 3. Documents for Reference

- Software Manual
  SH-2A, SH-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manuals
  SH7263 Group Hardware Manual
  SH7203 Group Hardware Manual
  The most up-to-date versions of the documents are available on the Renesas Technology Website.

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## Revision Record

| | | Description | |
|---|---|---|---|
| **Rev.** | **Date** | **Page** | **Summary** |
| 1.00 | Jun.18.08 | — | First edition issued |
| | | | |
| | | | |
| | | | |
| | | | |
| | | | |

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