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April 1st, 2010
Renesas Electronics Corporation

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APPLICATION NOTE**Flickering of LEDs Connected to I/O Ports****Introduction**

The two LEDs connected to the I/O ports are alternately turned on and off.

Target Device

H8/300H Tiny Series H8/3664

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1. Specifications

1. The two LEDs connected to the I/O ports are alternately turned on and off, as shown in figure 1.1.
2. The timing for turning on and off the LEDs is set to 0.5 s using the clock time-base function of timer A.
3. LED1 is connected to the P7₄ output pin of port 7 and LED2 is connected to the P8₇ output pin of port 8.

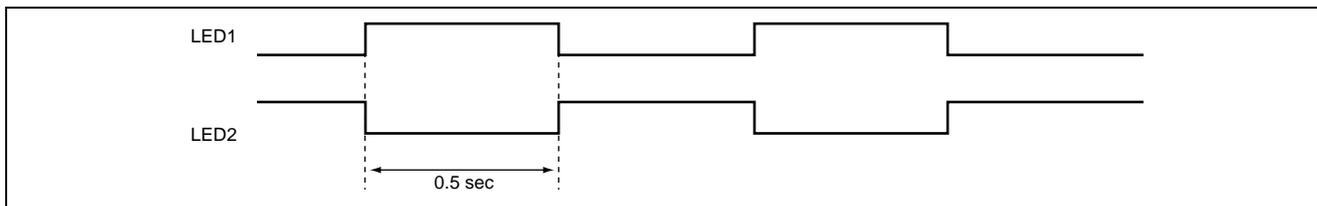


Figure 1.1 LED Flickering Operation

2. Description of Functions Used

In this sample task, the LEDs that are connected to the I/O ports are turned on and off.

Figure 2.1 is a block diagram of the I/O ports. The elements of the block diagram are described below.

- Port control register 7 (PCR7) selects inputs/outputs in bit units for pins P7₆ to P7₄ of port 7. Setting PCR7₄ to 1 makes the P7₄ pin an output port, while clearing the bit to 0 makes it an input port.
- Port data register 7 (PDR7) is an 8-bit register that stores data for port 7 pins P7₆ to P7₄. If port 7 is read while PCR7 bits are set to 1, the values stored in PDR7 are read, regardless of the actual pin states. If port 7 is read while PCR7 bits are cleared to 0, the pin states are read.
- Port control register 8 (PCR8) selects inputs/outputs in bit units for pins P8₇ to P8₀ of port 8. Setting PCR8₇ to 1 makes the P8₇ pin an output port, while clearing the bit to 0 makes it an input port.
- Port data register 8 (PDR8) is an 8-bit register that stores data for port 8 pins P8₇ to P8₀. If port 8 is read while PCR8 bits are set to 1, the values stored in PDR8 are read, regardless of the actual pin states. If port 8 is read while PCR7 bits are cleared to 0, the pin states are read.

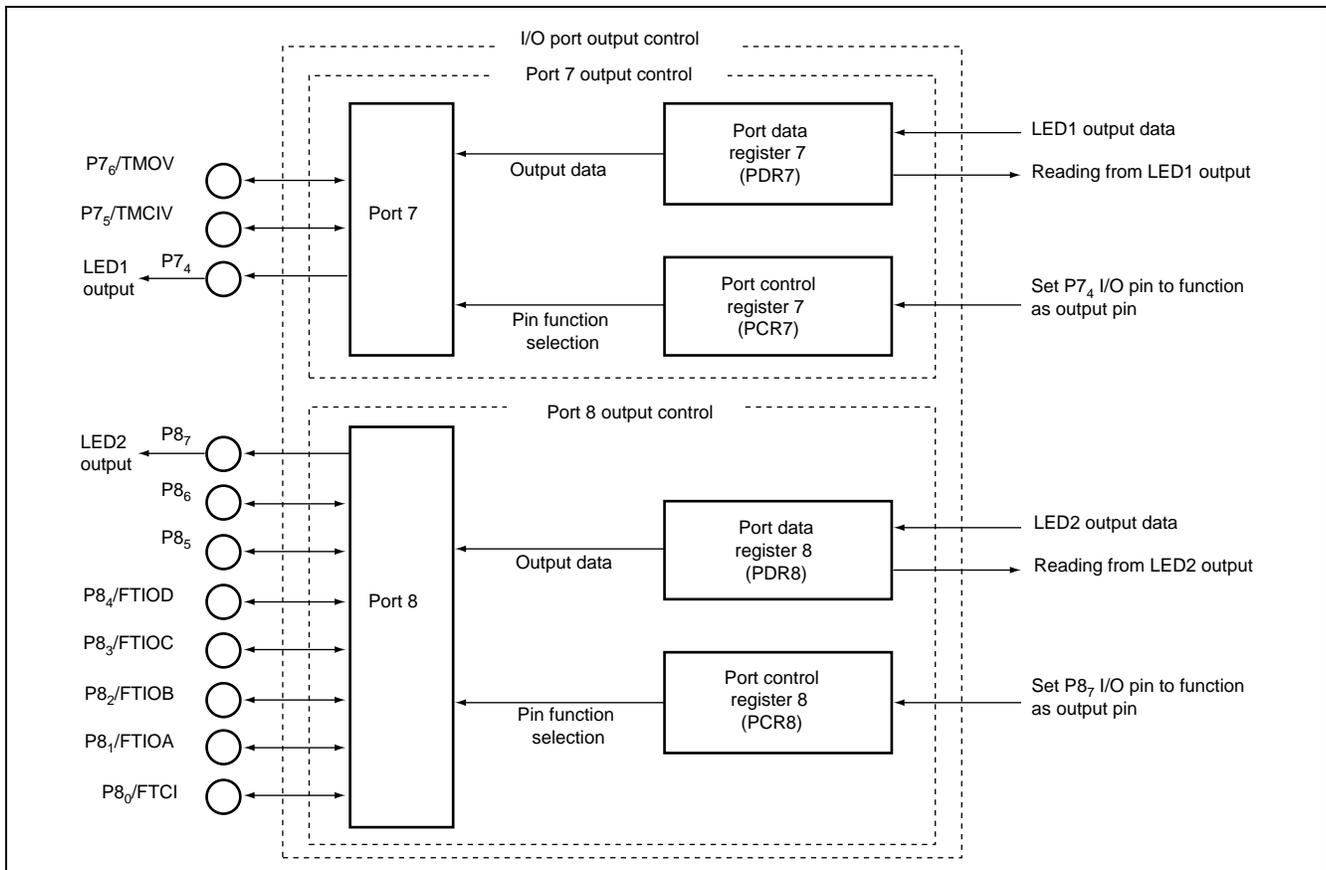


Figure 2.1 I/O Ports

Table 2.1 lists the function allocation for this sample task. The functions listed in table 2.1 are allocated so that the LEDs connected to the I/O ports can be made to flicker.

Table 2.1 Function Allocation

Function	Description
PDR7	Stores data output from pins P7 ₆ to P7 ₄ of port 7
PDR8	Stores data output from pins P8 ₇ to P8 ₀ of port 8
PCR7	Sets functions of I/O pins P7 ₆ to P7 ₄ of port 7
PCR8	Sets functions of I/O pins P8 ₇ to P8 ₀ of port 8
P7 ₄	LED1 output pin
P8 ₇	LED2 output pin
PSW	5-bit counter with clock input of 32.768 kHz/4
TCA	8-bit counter with clock input of the PSW output clock
TMA	Selects the clock time-base function of timer A and sets the TCA overflow cycle to 0.5 s

3. Description of Operations

Figure 3.1 shows this sample task's principle of operation. The hardware and software processing shown in figure 3.1 makes the LEDs connected to the I/O ports flicker.

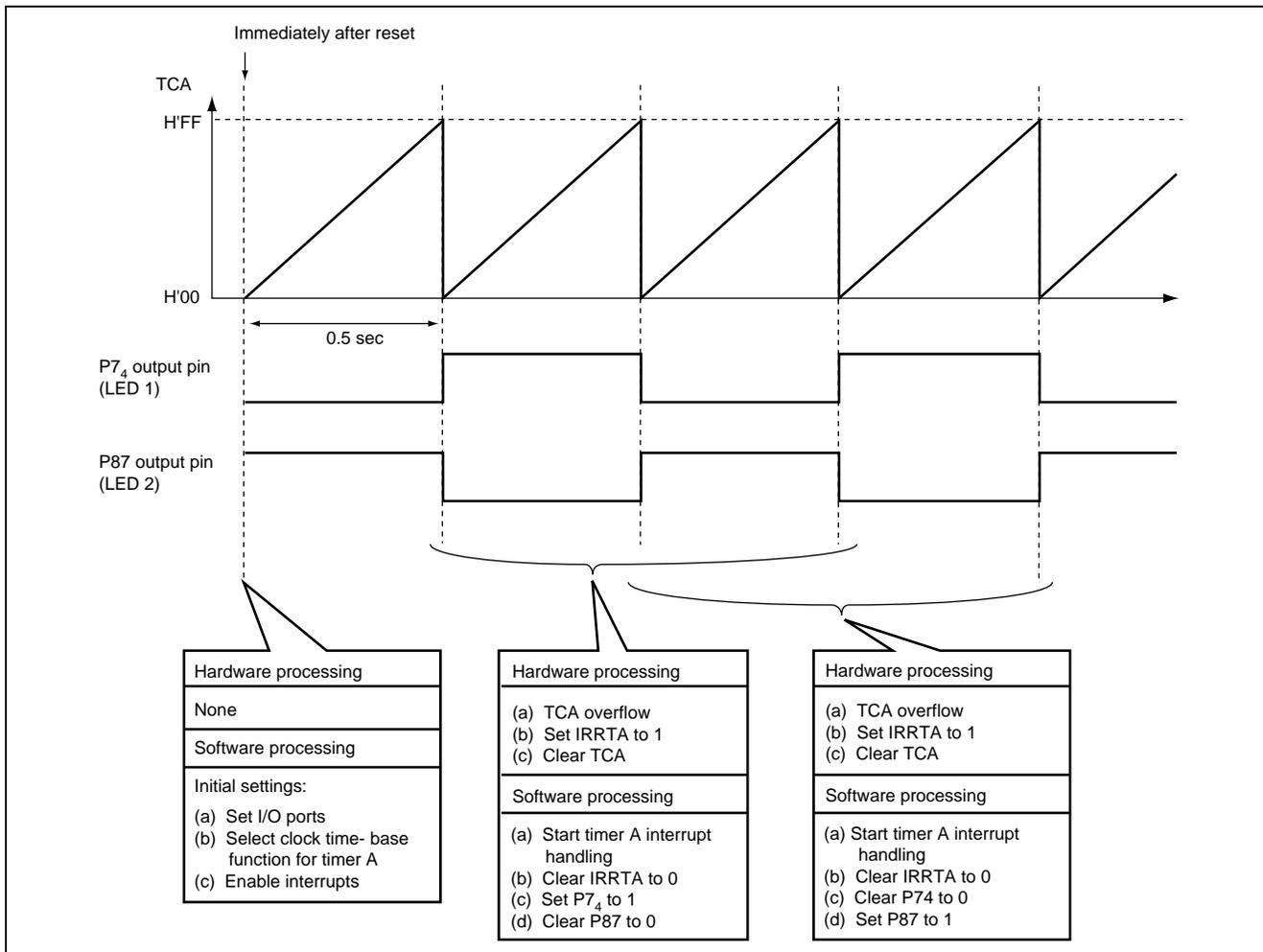


Figure 3.1 Operation Principle: Making LEDs Connected to I/O Ports Flicker

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the software used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Selects the clock time-base function for timer A, sets I/O ports, and enables interrupts.
Port output	taint	During the timer A interrupt handling routine, judges the LED1 and LED2 outputs and controls output.

4.2 Description of Arguments

No arguments are used in this sample task.

4.3 Description of Internal Registers

Table 4.2 describes the internal registers used in this sample task.

Table 4.2 Description of Internal Registers

Register Name	Function	Address	Setting
TMA	Timer mode register A (internal clock select):	H'FFA6	
TMA3	When TMA3 and TMA0 are both set to 1 and TMA2 and TMA1 are both cleared to 0, timer A is set to the clock time-base function, the prescaler is set to PSW, and the TCA overflow cycle is set to 0.5 s.	Bit 3	TMA3 = 1
TMA2		Bit 2	TMA2 = 0
TMA1		Bit 1	TMA1 = 0
TMA0		Bit 0	TMA0 = 1
TCA	Timer counter A: 8-bit up-counter incremented by clock input of PSW output clock and overflows every 0.5 s.	H'FFA7	H'00
PDR7	P74	Port data register 7 (port data register 7 ₄): When P74 is cleared to 0, the P7 ₄ pin output level is low. When P74 is set to 1, the P7 ₄ pin output level is high.	H'FFDA Bit 4 0
PDR8	P87	Port data register 8 (port data register 8 ₇): When P87 is cleared to 0, the P8 ₇ pin output level is low. When P87 is set to 1, the P8 ₇ pin output level is high.	H'FFDB Bit 7 1
PCR7	PCR74	Port control register 7 (port control register 7 ₄): When PCR7 ₄ is set to 1, the P7 ₄ pin functions as an output pin.	H'FFEA Bit 4 1

Table 4.2 Description of Internal Registers (cont)

Register Name	Function	Address	Setting
PCR8	PC87	Port control register 8 (port control register 8 ₇): When PC87 is set to 1, the P8 ₇ pin functions as an output pin.	H'FFEB Bit 7 1
IENR1	IENTA	Interrupt enable register 1 (timer A interrupt enable): When IENTA is set to 1, timer A interrupt requests are enabled.	H'FFF4 Bit 6 1
IRR1	IRRTA	Interrupt request register 1 (timer A interrupt request flag): When IRRTA is cleared to 0, no timer A interrupt is requested. When IRRTA is set to 1, a timer A interrupt is requested.	H'FFF6 Bit 6 0

4.4 Description of RAM

RAM is not used in this sample task.

5. Flowcharts

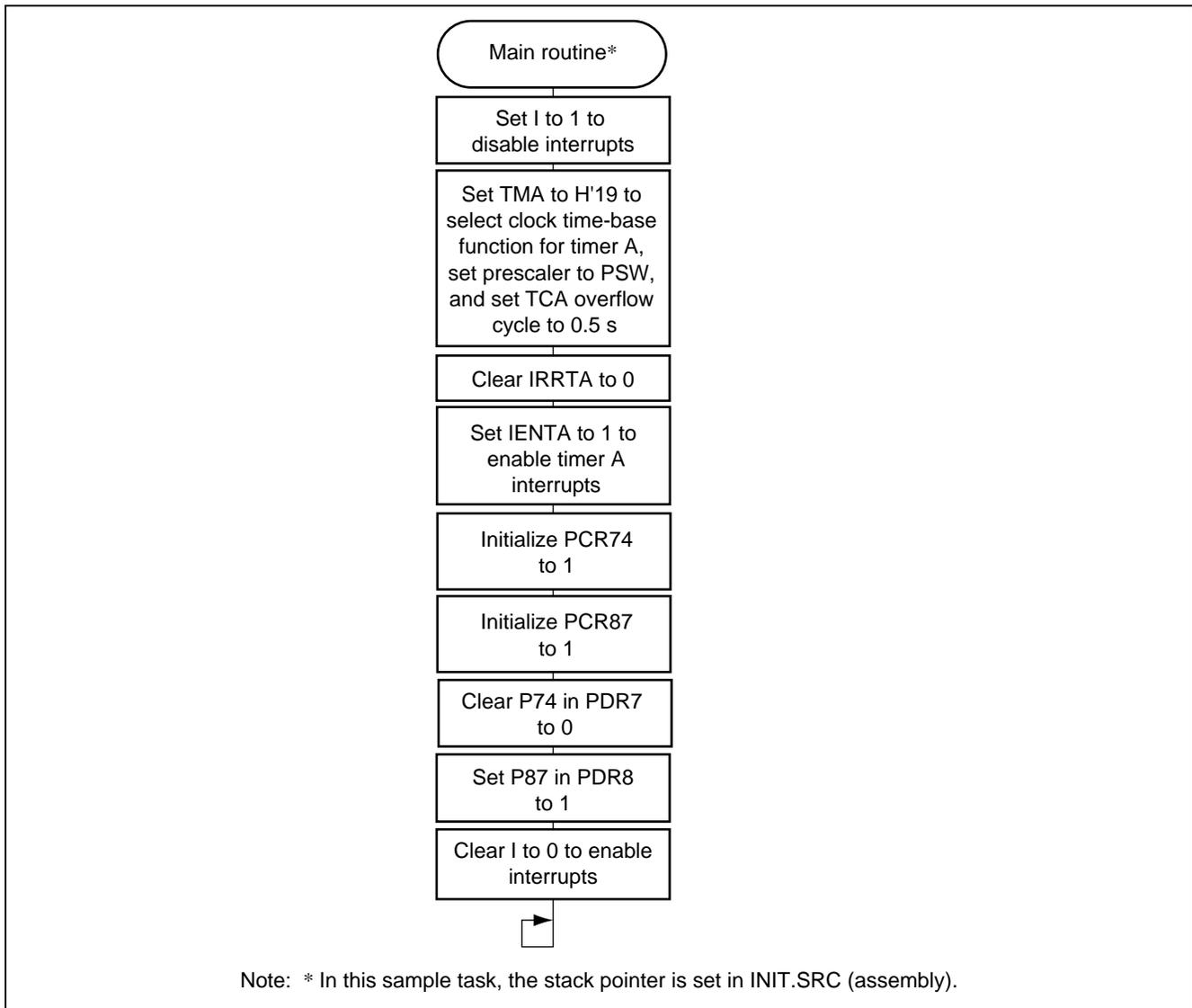


Figure 5.1 Flowchart for Main Routine

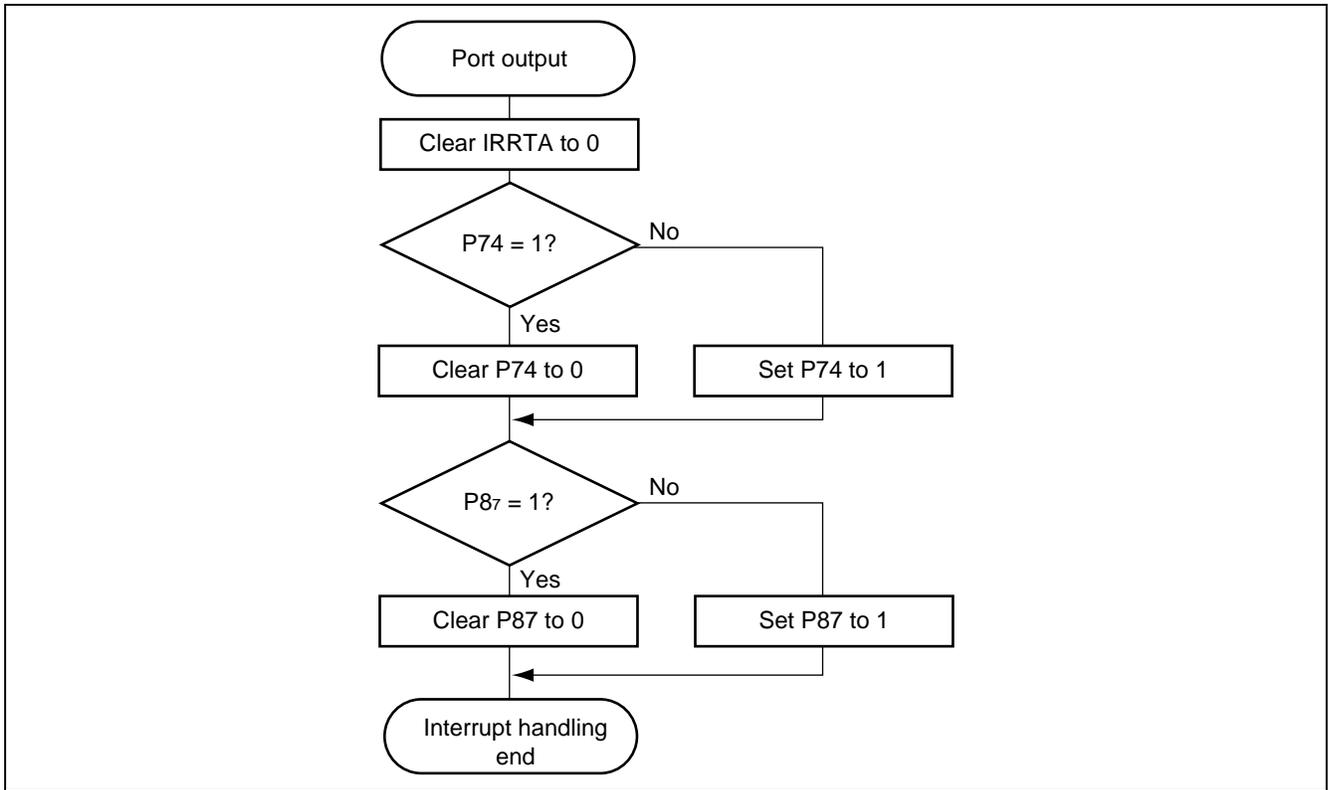


Figure 5.2 Flowchart for Timer A Interrupt Handling Routine

6. Program Listing

INIT.SRC (Program listing)

```
.EXPORT _INIT
.IMPORT _main
;
.SECTION P, CODE
_INIT:
MOV.W #H'FF80,R7
LDC.B #B'10000000,CCR
JMP @_main
;
.END
```

```
/*
*****
/*
H8/300H Tiny Series -H8/3664-
/*
Application Note
/*
'Flickering of LEDs Connected to I/O Port'
/*
Function
/*
: I/O Port
/*
External Clock : 16MHz
/*
Internal Clock : 16MHz
/*
Sub Clock : 32.768kHz
/*
*****
```

```
#include <machine.h>
```

```

/*****/
/*   Symbol Definition                               */
/*****/

struct BIT {
    unsigned char  b7:1;    /* bit7 */
    unsigned char  b6:1;    /* bit6 */
    unsigned char  b5:1;    /* bit5 */
    unsigned char  b4:1;    /* bit4 */
    unsigned char  b3:1;    /* bit3 */
    unsigned char  b2:1;    /* bit2 */
    unsigned char  b1:1;    /* bit1 */
    unsigned char  b0:1;    /* bit0 */
};

#define TMA      *(volatile unsigned char *)0xFFA6 /* Timer Mode Register A */
#define TCA      *(volatile unsigned char *)0xFFA7 /* Timer Counter A */
#define PDR7_BIT (*(struct BIT *)0xFFDA)          /* Port Data Register 7 */
#define P74      PDR7_BIT.b4                      /* Port Data Register 74 */
#define PDR8_BIT (*(struct BIT *)0xFFDB)          /* Port Data Register 8 */
#define P87      PDR8_BIT.b7                      /* Port Data Register 87 */
#define PCR7_BIT (*(struct BIT *)0xFFEA)          /* Port Control Register 7 */
#define PCR74    PCR7_BIT.b4                      /* Port Control Register 74 */
#define PCR8_BIT (*(struct BIT *)0xFFEB)          /* Port Control Register 8 */
#define PCR87    PCR8_BIT.b7                      /* Port Control Register 87 */
#define IENR1_BIT (*(struct BIT *)0xFFF4)         /* Interrupt Enable Register 1 */
#define IENTA    IENR1_BIT.b6                    /* Timer A Interrupt Enable */
#define IRR1_BIT (*(struct BIT *)0xFFF6)         /* Interrupt Request Register 1 */
#define IRRTA    IRR1_BIT.b6                    /* Timer A Interrupt Request Flag */

#pragma interrupt (taint)

/*****/
/*   Function Definition                               */
/*****/

extern void INIT ( void ); /* SP Set */
void main ( void );
void taint ( void );

```

```

/*****
/*   Vector Address                               */
/*****

#pragma section V1                               /* VECTOR SECTOIN SET */
void (*const VEC_TBL1[])(void) = {
/* 0x00 - 0x0f */
    INIT                                         /* 00 Reset           */
};
#pragma section V2                               /* VECTOR SECTOIN SET */
void (*const VEC_TBL2[])(void) = {
    taint                                       /* 26 Timer A Interrupt */
};
#pragma section                                 /* P                   */
/*****
/*   Main Program                               */
/*****

void main ( void )
{
    set_imask_ccr(1);                          /* Interrupt Disable   */

    TMA = 0x19;                                /* Initialize TCA Overflow Period */

    IRRTA = 0;                                 /* Clear IRRTA         */
    IENTA = 1;                                 /* Timer A Interrupt Enable */

    PCR74 = 1;                                 /* Initialize P74 Output Terminal Function */
    PCR87 = 1;                                 /* Initialize P87 Output Terminal Function */

    P74 = 1;                                   /* Initialize P74 Terminal Output */
    P87 = 0;                                   /* Initialize P87 Terminal Output */

    set_imask_ccr(0);                          /* Interrupt Enable     */

    while(1) {
        ;
    }
}

```

```
/* ***** */
/* Timer A Interrupt */
/* ***** */
void taint ( void )
{
    IRRTA = 0; /* Clear IRRTA */
    if ( P74 == 1 ) { /* Turn on LED1 ? */
        P74 = 0; /* Turn off LED1 */
    }
    else{
        P74 = 1; /* Turn on LED1 */
    }

    if ( P87 == 1 ){ /* Turn on LED2 ? */
        P87 = 0; /* Turn off LED2 */
    }
    else{
        P87 = 1; /* Turn on LED2 */
    }
}

```

Link Address Setting:

Section Name	Address
CV1	H'0000
CV2	H'0026
P	H'0100

