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April 1st, 2010
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SH7263/SH7203

Guidelines for Hi-Speed USB 2.0 Board Design

Summary

This document describes the guidelines for Hi-Speed USB 2.0 board design.

Target Device

The application explained in this document applies to the following LSIs.

- SH7263/SH7203 (In this document, SH7263/SH7203 are described as "SH7263".)

Note: The contents in this document are provided as a reference example based on the USB specification, and the signal system quality is not guaranteed. When implementing this example into an existing system, the overall system should be thoroughly evaluated, and the user should integrate at their own discretion.

Contents

1. Introduction

This document is described by using the pin names of the SH7263 USB 2.0 host/function module. Table 1 lists the outline of the USB 2.0 host/function module pin.

Table 1 Outline of the USB 2.0 Host/Function Module Pin

Pin Number	Pin Name	I/O	Name	Function
101	DP	I/O	USB D+ data	USB bus D+ data
100	DM	I/O	USB D- data	USB bus D- data
102	VBUS	I	VBUS input	Connect to USB bus VBUS
105	REFRIN	I	Reference input	Connect to USBAPVss via 5.6 KΩ ± 1% resistor
93	USB_X1	I	USB crystal resonator/ External clock	Connect to USB crystal resonator. Also, the external clock can be input to the USB_X1 pin.
94	USB_X2	O		
107	USBAPVcc	I	Transceiver analog pin power supply	3.3 V analog power supply for pins
106	USBAPVss	I	Transceiver analog pin ground	3.3 V analog ground for pins
99	USBDPVcc	I	Transceiver digital pin power supply	3.3 V digital power supply for pins
98	USBDPVss	I	Transceiver digital pin ground	3.3 V digital ground for pins
103	USBAVcc	I	Transceiver analog core power supply	1.2 V analog power supply for core
104	USBAVss	I	Transceiver analog core ground	1.2 V analog ground for core
108	USBDVcc	I	Transceiver digital core power supply	1.2 V digital power supply for core
109	USBDVss	I	Transceiver digital core ground	1.2 V digital ground for core
Notes	PVcc	I	Power supply for I/O circuit	3.3 V power supply for I/O pin
	PVss	I	Ground for I/O circuit	3.3 V ground for I/O pin
	Vcc	I	Power supply	1.2 V power supply for CPU internal
	Vss	I	Ground	1.2 V ground for CPU internal

Note: Refer to the SH7263/SH7203 Microcomputer Hardware Manuals for information on the PVcc, PVss, Vcc, and Vss power supply pins.

2. USB Transmission Line

The USB transmission line indicates the wiring pattern that connects the USB connector and the SH7263 embedded USB transceiver.

USB 2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The Hi-Speed mode has a 480 Mbps communication speed. Therefore, the USB transmission lines must be designed as a high-frequency circuit. Impedance control is required for the USB transmission lines.

Notes on designing the wiring pattern of the USB transmission lines are described below.

- The characteristic impedance required for the USB transmission lines is the differential impedance 90 Ω ± 15%.
- The pattern width and pattern pitch for impedance control vary depending on board thickness, material, and layer configuration. Contact the board manufacturer for more details.
- The wiring pattern length of the USB transmission lines from the SH7263 to the USB connector must be designed not to exceed the maximum delay time which is regulated by the USB specification. Table 2 lists the recommended values for the wiring pattern length of the USB transmission lines on typical PCB.

Table 2 Recommended Values For the Wiring Pattern Length of USB Transmission Line

	Maximum Delay Time (USB Specification)	Wiring Pattern Length	D+ and D- Wiring Differential
Host controller	3 ns	150 mm or less	2.5 mm or less
Function controller	1 ns	50 mm or less	2.5 mm or less

- The lower layer of the USB transmission lines must be a ground plane. The ground plane must be at least 2 mm wider than the USB transmission lines. The power supply for the ground plane is USBDPVss.
- Do not allocate other signal lines near the USB transmission lines. Particularly lines of heavily fluctuating signals, such as clock and data bus lines, must be allocated far from the USB transmission lines. Moreover, the USB transmission lines and other lines must not cross.
- The same layer (surface layer) as the USB transmission lines should be allocated 2 mm far from the USB transmission lines, and grounded with a guard ring.
- The USB transmission lines should be allocated on the same layer without passing through a hole. In addition, wiring should not be divaricated.
- The USB transmission lines should be wired with uniform spaces.
- The USB transmission lines should be allocated far from the oscillator, power supply circuit, and other I/O connectors.
- The USB transmission lines should be wired with straight lines. If they are bent, they should be bent gently in an arc or up to 135 degrees, and should not be bent at acute angles (right angles).
- It is recommended that the clock, reset, read, write and chip select signals should be grounded with a guard ring.

Figure 1 shows a design example of a Host controller USB transmission line pattern, and Figure 2 shows a design example of a function controller USB transmission line pattern.

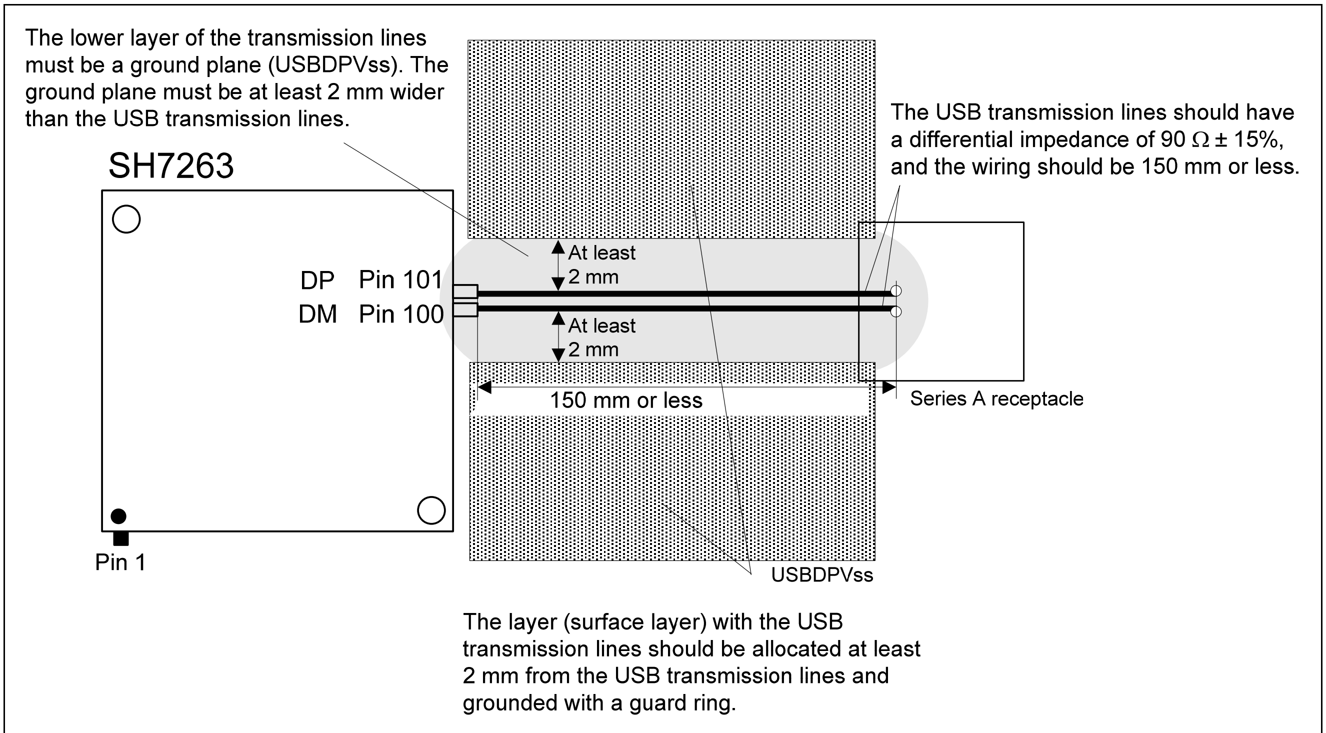


Figure 1 Design Example of the Host Controller USB Transmission Line Pattern

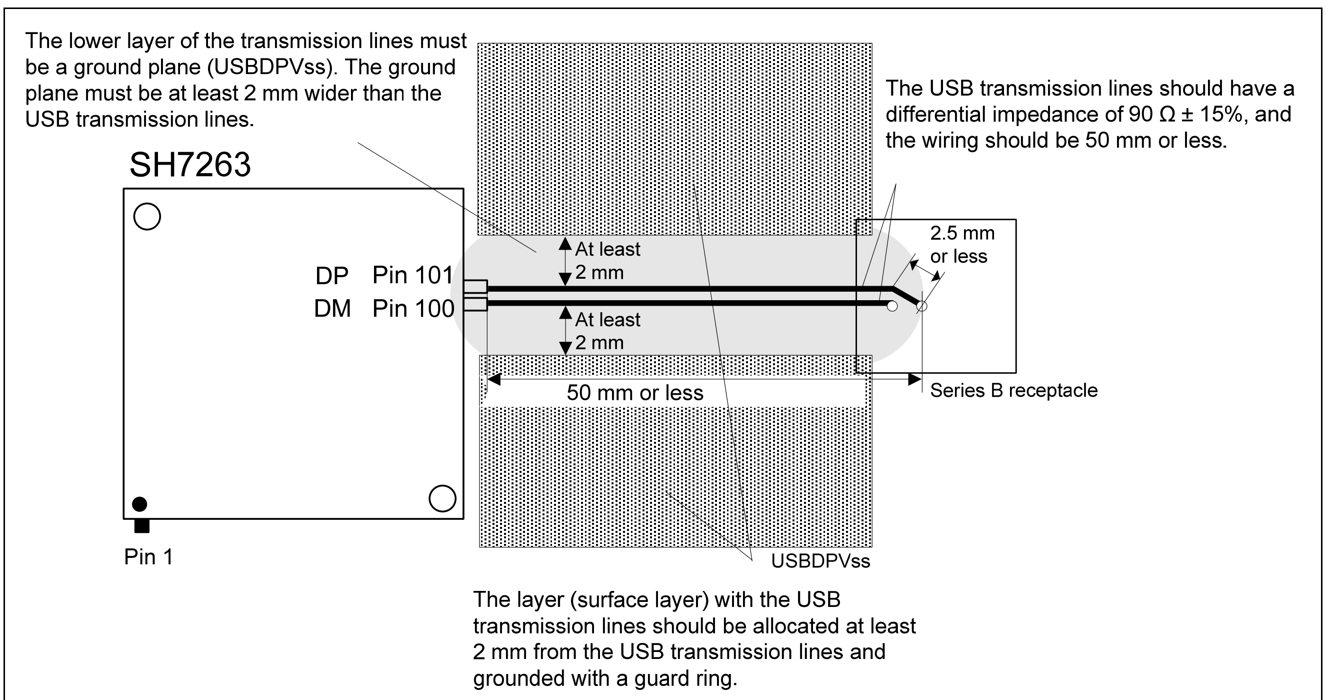


Figure 2 Design Example of the Function Controller USB Transmission Line Pattern

3. Power Supply and Ground Pattern

Notes on designing a power supply/ground pattern are described below.

- Power supplies and ground patterns should be separated into digital and analog. Table 3 and Table 4 list the power supply and ground classifications.

Table 3 USB Power Supply Classifications

SH7263 Pin Name	Power Supply Classifications			
	Analog Power Supply (1.2 V)	Digital Power Supply (1.2 V)	Analog Power Supply (3.3 V)	Digital Power Supply (3.3 V)
USBAVcc	○			
USBDVcc		○		
USBAPVcc			○	
USBDPVcc				○
Vcc		○		
PVcc				○

Note: ○ indicates the power used.

Table 4 USB Ground Classifications

SH7263 Pin Name/ USB Connector	Ground Classifications	
	Analog Ground (AGND)	Digital Ground (DGND)
USBAVss	○	
USBDVss		○
USBAPVss	○	
USBDPVss		○
Vss		○
PVss		○
USB Connector Ground (Including Frame Ground)		○

Note: ○ indicates the power used.

- The patterns of power supplies and grounds should be designed with as wide a surface layer as possible.
- Tantalum capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as power supply capacitors.
- Aluminum electrolytic capacitors affect the jitter value when measuring the EYE pattern. The capacitors should be thoroughly designed and tested before use.
- As the capacitance value of decoupling capacitor, it is recommended that the capacities for 0.001 µF, 0.01 µF, 0.1 µF, and 10 µF are allocated closest to the USB power supply pin. Figure 3 shows an example of decoupling capacitor allocation.

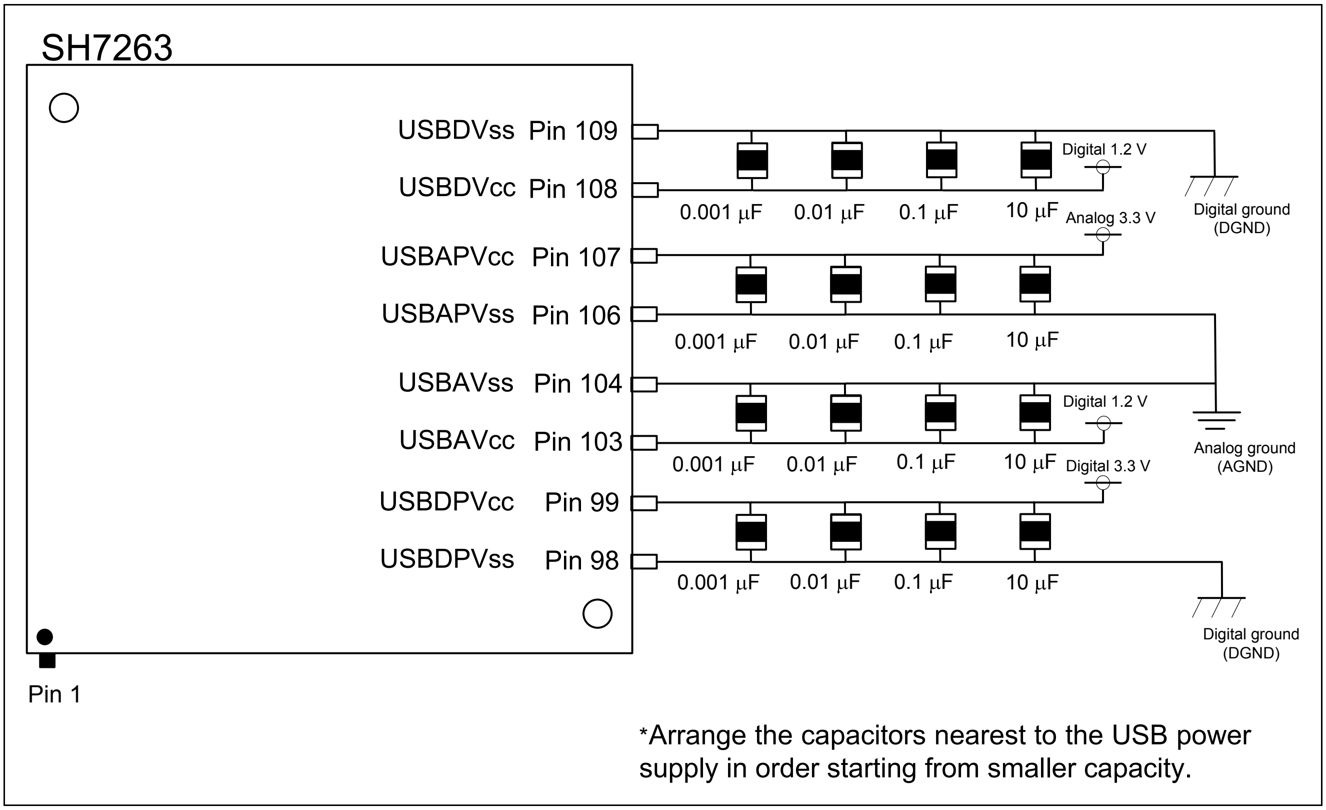


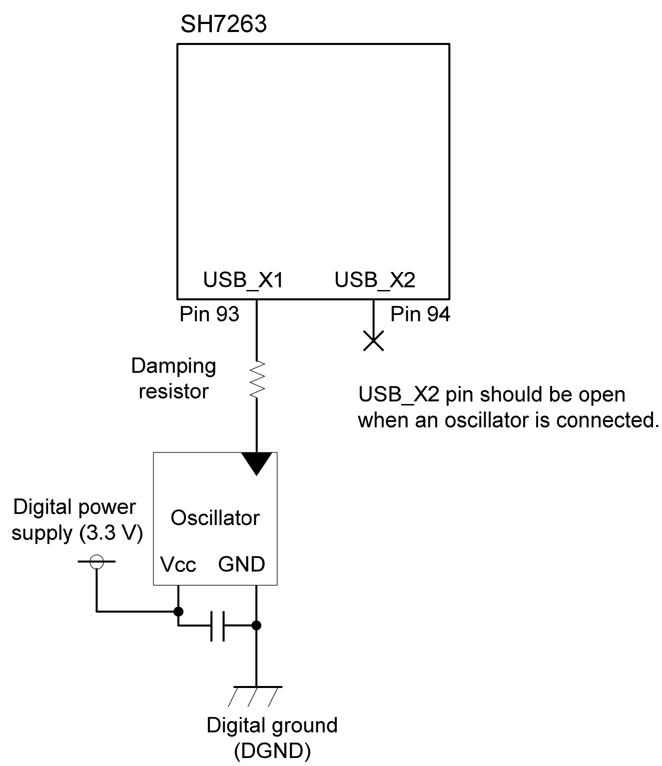
Figure 3 Example of the Decoupling Capacitor Allocation

4. Oscillation Circuit

Notes on designing an oscillation circuit are described below.

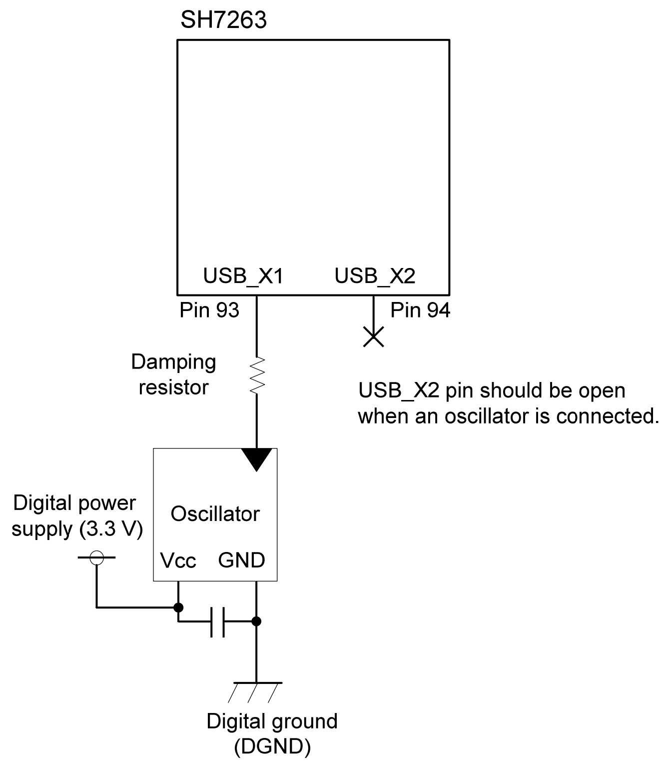
- The oscillation circuit should be allocated near the USB USB_X1 clock input pin. Grounding the USB_X1 with a guard ring is recommended.
- Oscillation components that fulfill a 48 MHz ± 100 ppm frequency specification should be used.
- When using a crystal resonator, the manufacturer should be consulted before deciding the circuit constant.

Figure 4 shows a connection example when the crystal resonator is used, and Figure 5 shows a connection example when an oscillator is used.



*A pattern with built-in damping resistors should be designed as the oscillator components may cause an overshoot or undershoot.

Figure 4 Example of a Crystal Resonator Connection



*A pattern with built-in damping resistors should be designed as the oscillator components may cause an overshoot or undershoot.

Figure 5 Example of an Oscillator Connection

5. VBUS Power Supply Circuit

Notes on designing the VBUS power supply circuit are described below.

- When the SH7263 is used as a host controller, the additional capacity of the VBUS line should be designed to be 120 μF or more.
- When the SH7263 is used as a function controller, the additional capacity of the VBUS line should be designed to be within 1.0 μF to 10 μF.
- The VBUS line should include a filter circuit as an overshoot may be caused by inconsistent impedance when the USB cable is connected. The 1.0 μF to 10 μF capacitor and 100 Ω to 1 KΩ resistor should be added as a filter circuit. The constant should be defined after confirming that an overshoot has not occurred on the board. Also, a resistor of more than 1 KΩ should not be added.
- When the SH7263 is used as a host controller, the VBUS power should be supplied to the function devices. A power switch IC with over-current protection for the USB power bus (hereinafter called "USB power switch IC") is recommended for the VBUS power supply control. Make sure to consider the limitation value of the current of VBUS power supply line based on the current value used by the system power supply applied and the USB function devices communicated. In addition, refer to the USB power switch IC datasheet used for the VBUS power supply control circuit.

Figure 6 shows an example of the VBUS power supply circuit when the SH7263 is used as a host controller.

Figure 7 shows an example of the VBUS power supply circuit when the SH7263 is used as a function controller.

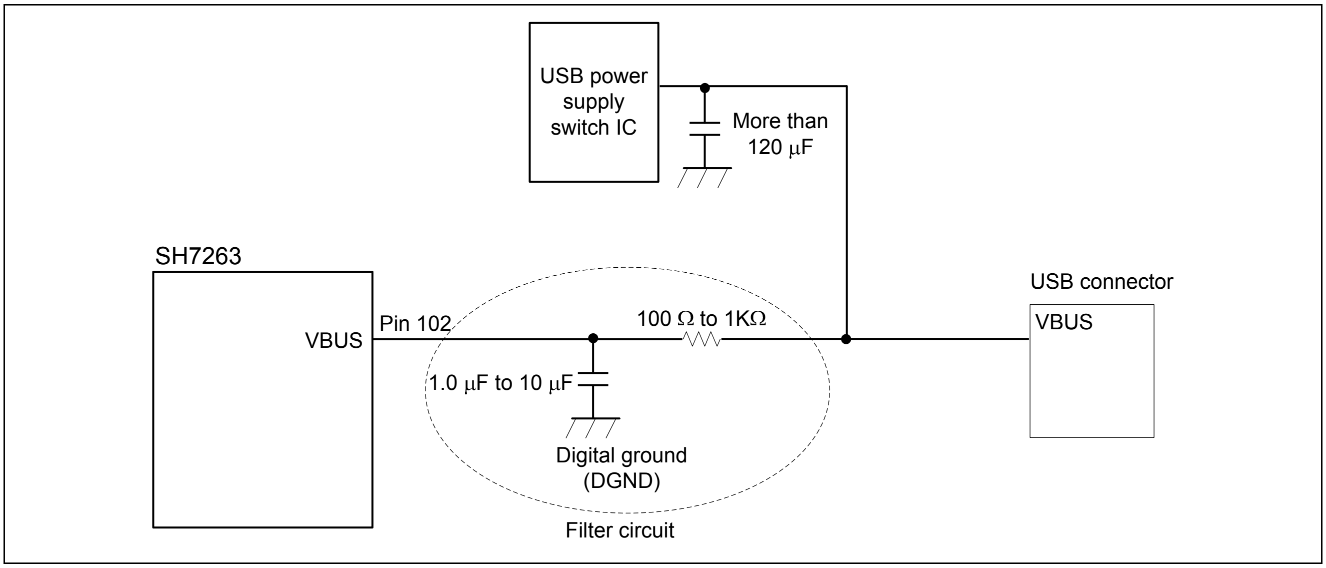


Figure 6 Example of the Host Controller VBUS Power Supply Circuit

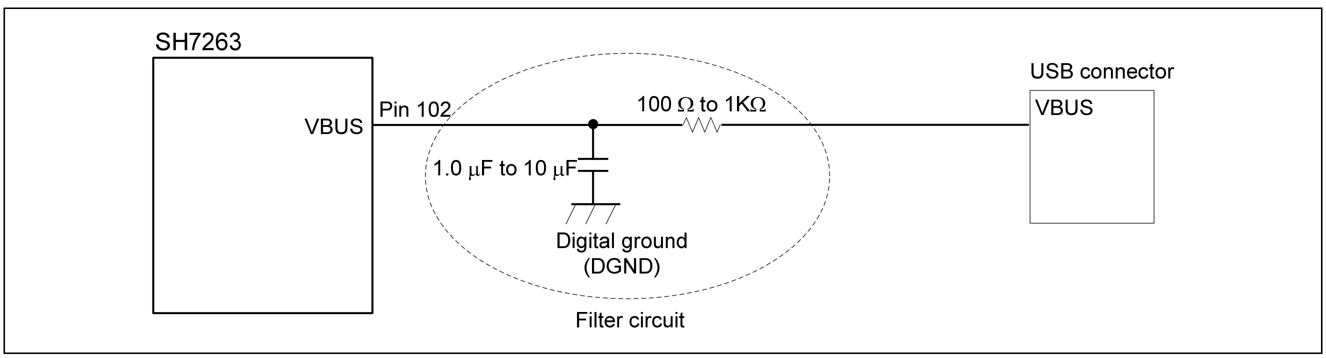


Figure 7 Example of the Function Controller VBUS Power Supply Circuit

6. REFRIN Pin

Notes on designing the circuit around the REFRIN pin are described below.

- A resistor of 5.6 KΩ ± 1% (hereinafter called “reference resistor”) should be allocated between the REFRIN pin and USBAPVss.
- A reference resistor should be allocated as close as possible to the SH7263.
- The REFRIN pin, the reference resistor, and USBAPVss should be connected with a bold, minimal pattern.
- The reference resistor and USBAPVss should be connected in an exclusive pattern, and then connected to the analog ground. The pattern should be designed to avoid common impedance with other signals.
- To prevent cross talk, heavily fluctuating signals such as DP, DM, clocks, address data, and control signals should neither cross nor go side by side with the reference resistor and patterns. It is recommended that the reference resistor and patterns be grounded with a guard ring.

Figure 8 shows the block diagram of the pin connection and the design example of the pattern around the REFRIN pin.

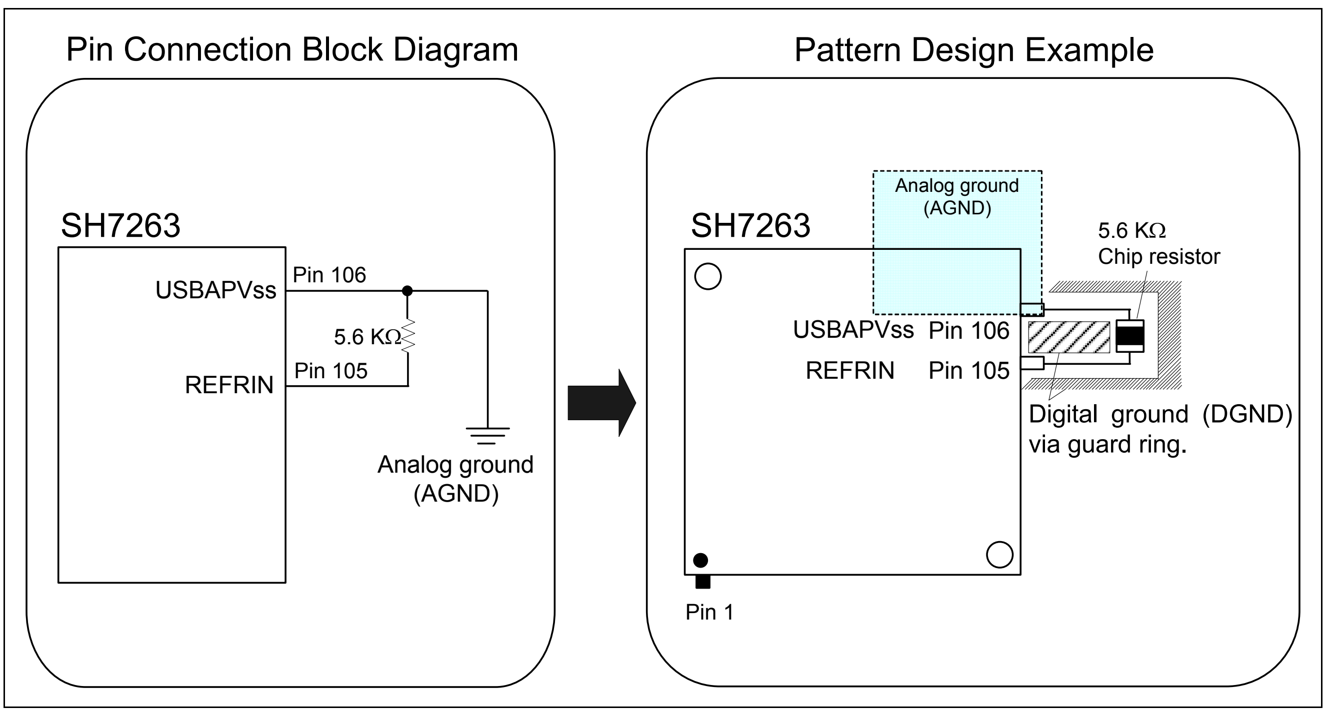


Figure 8 Pin Connection and Design Example of the Pattern Around the REFRIN Pin

7. EMI/ESD Workarounds

Notes on EMI/ESD workarounds are described below.

- When components for EMI/ESD workarounds such as coils and diodes are mounted on the USB transmission lines, they should be allocated near the USB transmission lines and the wiring should be as short as possible.
- The components for the EMI/ESD workarounds must be USB 2.0 compliant. Also, by mounting EMI/ESD workaround components, an inconsistent impedance may occur on the USB transmission lines, and the waveform may become distorted. Components for use should be selected after thorough evaluation.

Figure 9 shows the block diagram of a connection example when the components for EMI/ESD workarounds are used.

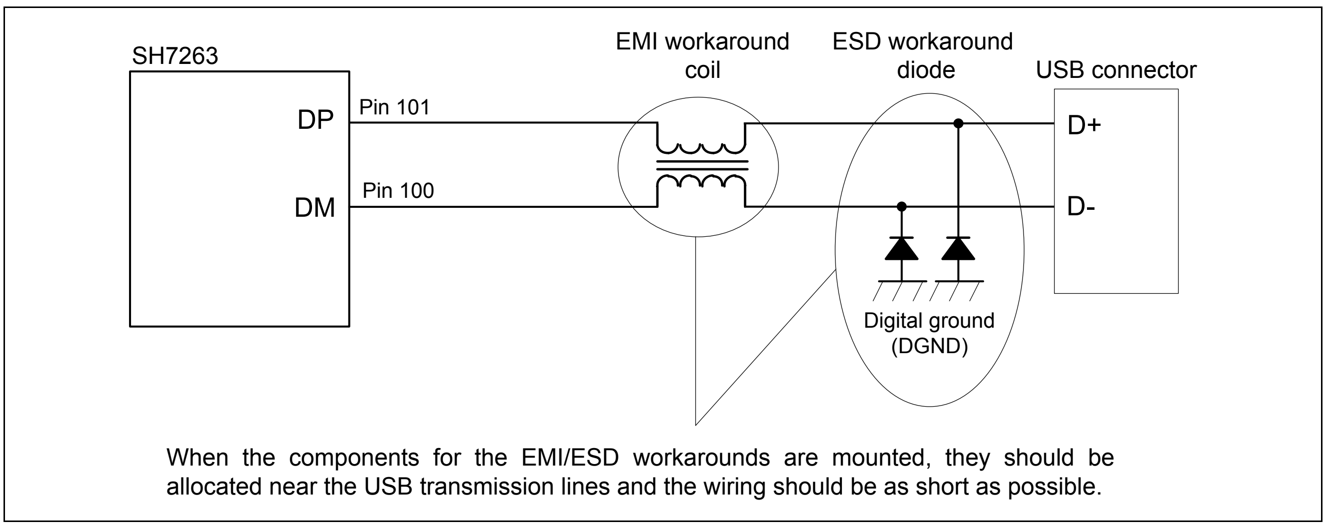


Figure 9 Connection Example When Components for EMI/ESD Workarounds are Used

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Revision History

Rev.	Date	Description	
		Page	Summary
1.0	Jan. 14, 2009	—	First edition issued