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Renesas Electronics Corporation

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# H8/38076R

## Transition to the Subsleep Mode

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### Introduction

In this example a transition is made from the subactive mode, one of the power-down modes of the H8/38076R, to the subsleep mode, another power-down mode.

### Target Device

H8/38076R

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## 1. Specifications

After a reset is cleared the H8/38076R can transition to any of seven power-down modes, in which power consumption is reduced substantially, in addition to the normal active (high-speed) mode. In this sample task a transition is made from the active (high-speed) mode to the subsleep mode, one of the power-down modes.

## 2. Description of Functions

### 2.1 Functions Used

In this sample task a transition is made from the active (high-speed) mode to the subsleep mode, one of the power-down modes.

The state of the H8/38076R in the subsleep mode is shown in table 1, and the functions used as described below.

1. Subclock ( $\phi_w$ )

This 32.768-kHz oscillation clock is a reference clock for operation of the CPU and peripheral functions.

2. Power-Down Mode (Subsleep Mode) Function

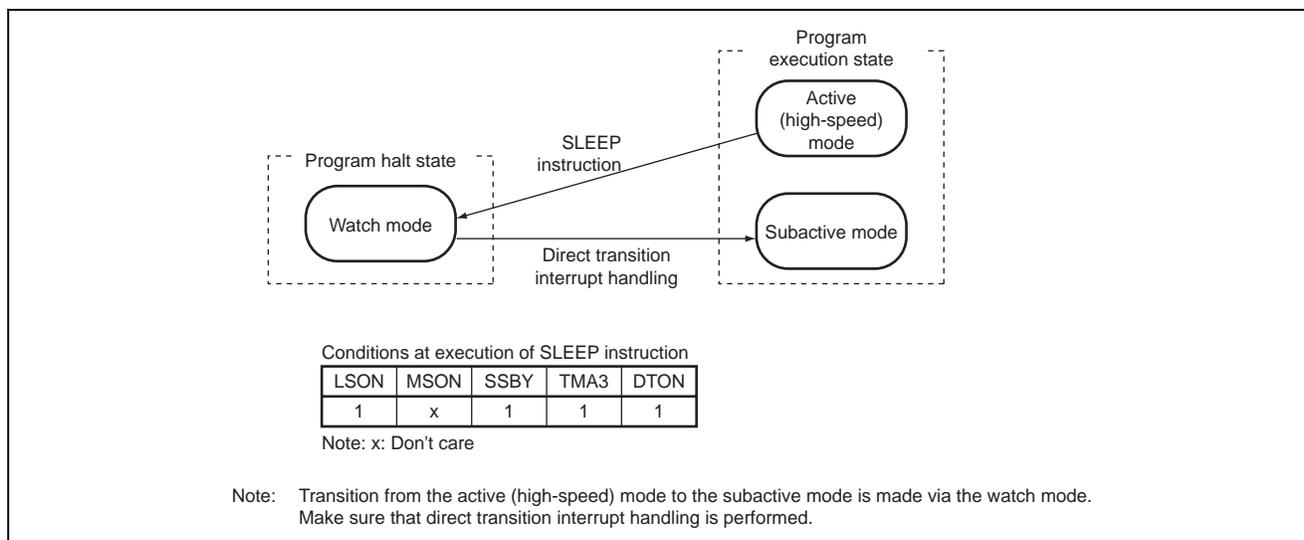
In the subsleep mode CPU operation stops but internal peripheral modules other than the A/D converter and PWM module continue to function. The contents of CPU registers, some registers of internal peripheral modules, and internal RAM are retained as long as the required voltage is applied. I/O ports keep the same states as before the transition.

The subsleep mode is cleared by an interrupt. When an interrupt is requested, the subsleep mode is cleared and interrupt exception handling starts. A transition is made to the subactive mode after the subsleep mode is cleared. The subsleep mode is not cleared if the I bit in CCR is set to 1 or the requested interrupt is disabled by an interrupt enable register.

When the  $\overline{\text{RES}}$  signal goes low in the subsleep mode, the system clock oscillator starts. The  $\overline{\text{RES}}$  signal must be kept low until output from the pulse generator stabilizes since system clock signals are supplied to the entire H8/38076R as soon as the system clock oscillator starts functioning. After the oscillation stabilization time has elapsed the CPU starts reset exception handling if the  $\overline{\text{RES}}$  signal is driven high.

Transition to the subsleep mode is only possible from the subactive mode. To transition to the subsleep mode from the normal active (high-speed) mode it is therefore necessary to first transition to the subactive mode. A diagram of the transition from the active (high-speed) mode to the subactive mode is shown in figure 1. For details of transitioning from the active (high-speed) mode to the subactive mode, see the relevant application note.

- System control register 1 (SYSCR1)  
Together with SYSCR2, SYSCR1 controls the power-down modes.
- System control register 2 (SYSCR2)  
Together with SYSCR1, SYSCR2 controls the power-down modes.



**Figure 1 Mode Transition to the Subactive Mode**

**Table 1 State of the H8/38076R in the Subsleep Mode**

Function	Subsleep Mode	
System clock oscillator	Halted	
Subclock oscillator	Functioning	
CPU	Instructions	Halted
	RAM	Retained
	Registers	Retained
	I/O	Retained
External interrupts	IRQ0	Functioning
	IRQ1	Functioning
	IRQ3	Functioning
	IRQ4	Functioning
	IRQAEC	Functioning
	WKP0 to WKP7	Functioning
Peripheral modules	Timer F	Functioning/Retained <sup>*1</sup>
	AEC (Asynchronous event counter)	Functioning
	RTC (realtime clock)	Functioning/Retained <sup>*2</sup>
	TPU (timer pulse unit)	Retained
	WDT (watchdog timer)	Functioning <sup>*3</sup> /Retained
	SCI3/IrDA module	Functioning/Retained <sup>*4</sup>
	I <sup>2</sup> C module	Retained
	PWM module	Retained
	A/D converter	Retained
LCD controller/driver	Functioning/Retained <sup>*5</sup>	

Notes: 1. Functioning if  $\phi_W/4$  is selected as an internal clock. Halted and retained otherwise.

2. Functioning if the clock time-base function is selected and retained if the interval timer is selected.

3. Only if the internal oscillator is selected.

4. Functioning if  $\phi_W/2$  is selected as an internal clock. Halted and retained otherwise.

5. Functioning if  $\phi_W$ ,  $\phi_W/2$ , or  $\phi_W/4$  is selected as the clock to be used. Halted and retained otherwise.

## 2.2 Assignment of Functions

Table 2 shows the assignment of functions in this sample task. A transition is made from the subactive mode, one of the power-down modes of the H8/38076R, to the subsleep mode, another power-down mode, using functions assigned as shown in table 2.

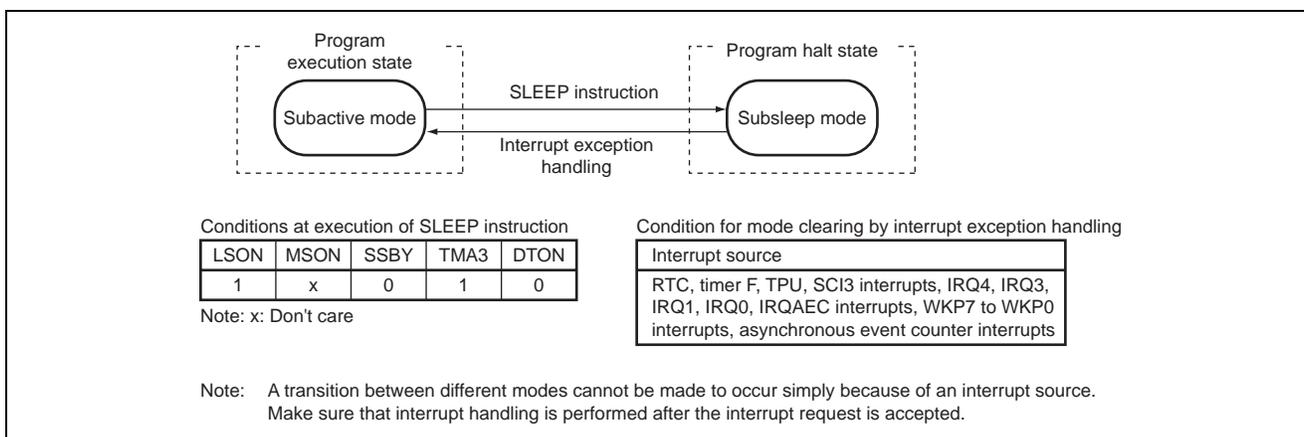
**Table 2 Assignment of Functions**

<b>Elements</b>	<b>Description</b>
SYSCR1	Together with SYSCR2, controls transition to the subsleep mode
SYSCR2	Together with SYSCR1, controls transition to the subsleep mode

### 3. Principles of Operation

The principles of operation of this sample task are described below. Using the procedure shown, a transition is made from the subactive mode to the subsleep mode, one of the power-down modes. The mode transitions in this sample task are illustrated in figure 2.

1. Transition to the subsleep mode
  - a. Clear the SSBY bit to 0 and set the LSON and TMA3 bits to 1 in SYSCR1.
  - b. Clear the DTON bit in SYSCR2 to 0.
  - c. Execute the SLEEP instruction.
2. Clearing the subsleep mode
  - a. Receive an interrupt request in the subsleep mode.
  - b. Perform interrupt handling. (The recovery destination of the interrupt will be the subactive mode.)



**Figure 2 Mode Transition Diagram**

#### 4. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- SYSCR1                      System control register 1                      Address: H'FFF0

Bit	Bit Name	Set Value	R/W	Description
7	SSBY	0	R/W	Software standby Selects the mode to transition to after execution of the SLEEP instruction. 0: A transition is made to the sleep mode or the subsleep mode 1: A transition is made to the standby mode or the watch mode
3	LSON	1	R/W	Selects the system clock ( $\phi$ ) or subclock ( $\phi_{SUB}$ ) as the CPU operating clock when the watch mode is cleared. 0: The CPU operates on the system clock ( $\phi$ ) 1: The CPU operates on the subclock ( $\phi_{SUB}$ )
2	TMA3	1	R/W	In combination with bits SSBY and LSON in SYSCR1 and bits DTON and MSON in SYSCR2, TMA3 selects the mode to which transition is made after the SLEEP instruction is executed.

- SYSCR2                      System control register 2                      Address: H'FFF1

Bit	Bit Name	Set Value	R/W	Description
3	DTON	0	R/W	Direct transfer on flag Selects the mode to transition to after the SLEEP instruction is executed with bits SSBY, TMA3, and LSON in SYSCR1 and bit MSON in SYSCR2.
1	SA1	User defined	R/W	Subactive mode clock selection 1 and 0
0	SA0	User defined	R/W	Selects the operating clock frequency in the subactive and subsleep modes. The operating clock frequency changes to the set frequency after the SLEEP instruction is executed. 00: $\phi_W/8$ 01: $\phi_W/4$ 1x: $\phi_W/2$

Note: x: Don't care

**Revision Record**

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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