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H8/38076R

Voltage Measurement Using 4-Channel Successive Approximation A/D Conversion

Introduction

In this example the internal A/D converter is used to measure voltage by 4-channel A/D conversion.

Target Device

H8/38076R

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1. Specifications

- In this sample task the A/D converter is used to measure voltage by 4-channel A/D conversion.
- The end of conversion is determined by referencing the ADSF bit by software polling.
- The four channel voltages are input to AN0 to AN3, and the A/D conversion results are stored in RAM.
- A sample connection diagram is shown in figure 1.

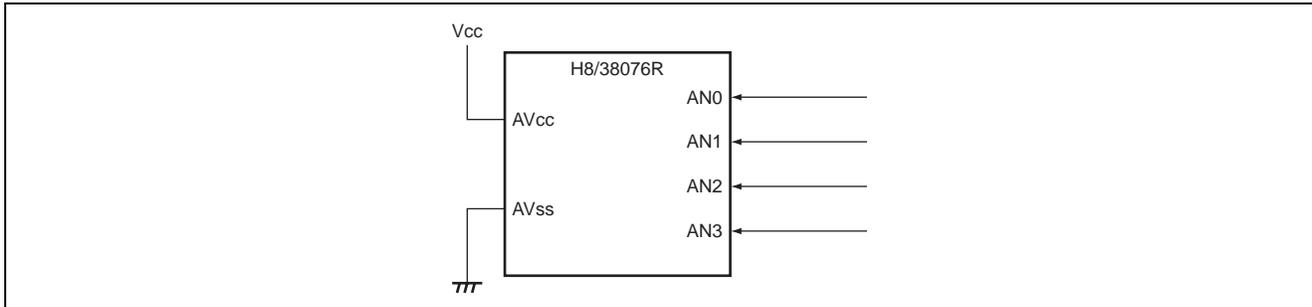


Figure 1 Voltage Measurement by 4-Channel A/D Conversion

2. Functions Used

2.1 Functions

In this sample task the A/D converter is used to measure voltage by 4-channel A/D conversion. A block diagram of the A/D converter is shown in figure 2 and its operation is described below.

1. A/D Converter

The H8/38076R includes a successive approximation type 10-bit A/D converter that allows up to eight analog input channels to be selected.

- A/D result register (ADRR)

ADRR is a 16-bit read-only register that stores the result of A/D conversion. The upper 10 bits of the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR value during A/D conversion is undefined. After A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion operation starts. The initial value of ADRR is undefined.

- A/D mode register (AMR)

AMR sets the conversion time for the A/D converter, selects the external trigger, and specifies the analog input pins. In this sample task AN3 is set as the input pin.

- A/D start register (ADSR)

ADSR starts and stops A/D conversion.

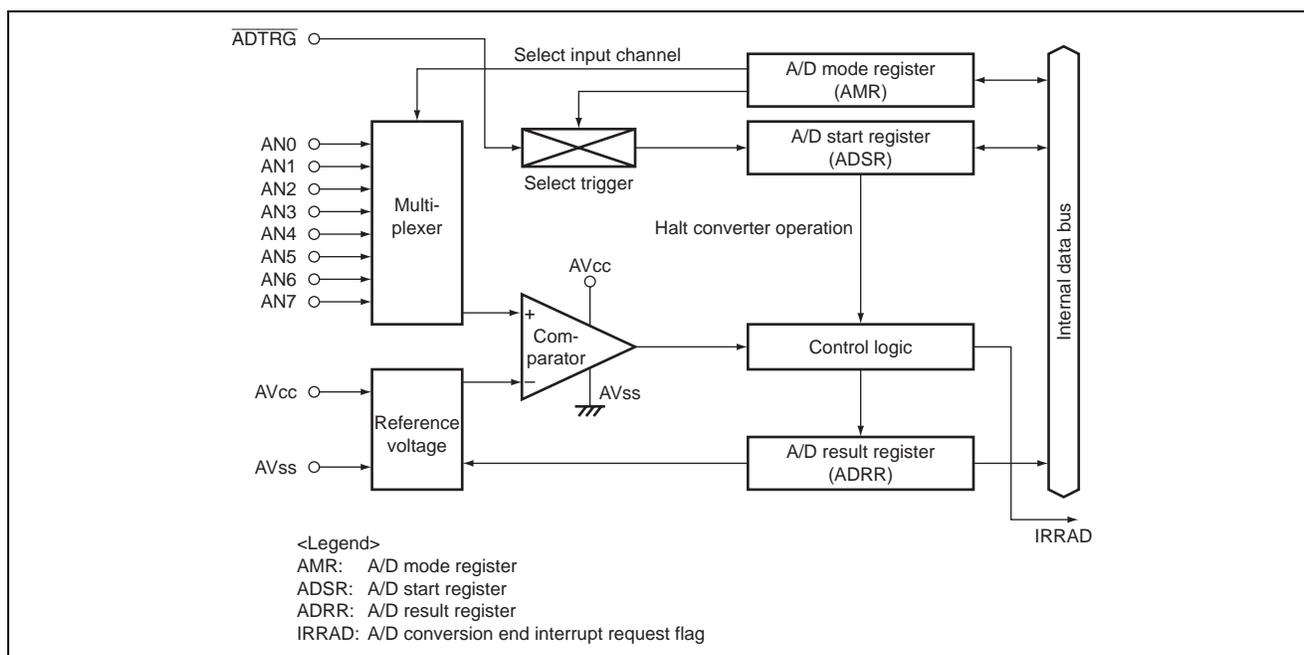


Figure 2 Block Diagram of A/D Converter

2. Port B

Port B is an input-only port with pins that function as both interrupt input pins and analog input pins.

- **Port mode register B (PMRB)**

PMRB controls the selection of functions for port B pins. In this sample task it is used to set AN0, AN1, and AN2 as input pins.

3. Module Standby Function

The module-standby function can be specified for any peripheral module. In the module standby mode the clock supply to the specified module stops and it enters a power-down mode. Clearing a bit in CKSTPR1 or CKSTPR2 corresponding to a module sets it to the module standby mode. Setting the bit to 1 cancels the module standby mode for the corresponding module.

- **Clock stop register 1 (CKSTPR1)**

CKSTPR1 allows the internal peripheral modules to enter the standby state in module units. In this sample task the A/D converter enters the standby state after A/D conversion completes.

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. The watchdog timer is operated using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Classification	Description
ADRR	A/D	Stores A/D conversion result (16-bit register)
AMR	A/D	Sets A/D conversion time, enables/disables A/D conversion by external trigger input, and selects analog input pins. In this sample task the A/D conversion time is set to 31 states, external trigger input is not used, and channels 0 to 3 are used.
ADSR	A/D	Specifies start and forced stop of A/D conversion
PMRB	I/O port	Function selection for analog input pins
CKSTPR1	Power-down	Sets the module standby mode of A/D converter
AN0 to AN7	Pin	Input pins of the A/D converter. Pins AN0 to AN3 are used in this sample task.
ADTRG	Pin	External trigger input pin. Not used in this sample task.
AVcc, AVss	Pin	Power supply pins for analog block (reference voltage, comparator) of the A/D converter

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Voltage is measured using the hardware and software processings shown in figure 3.

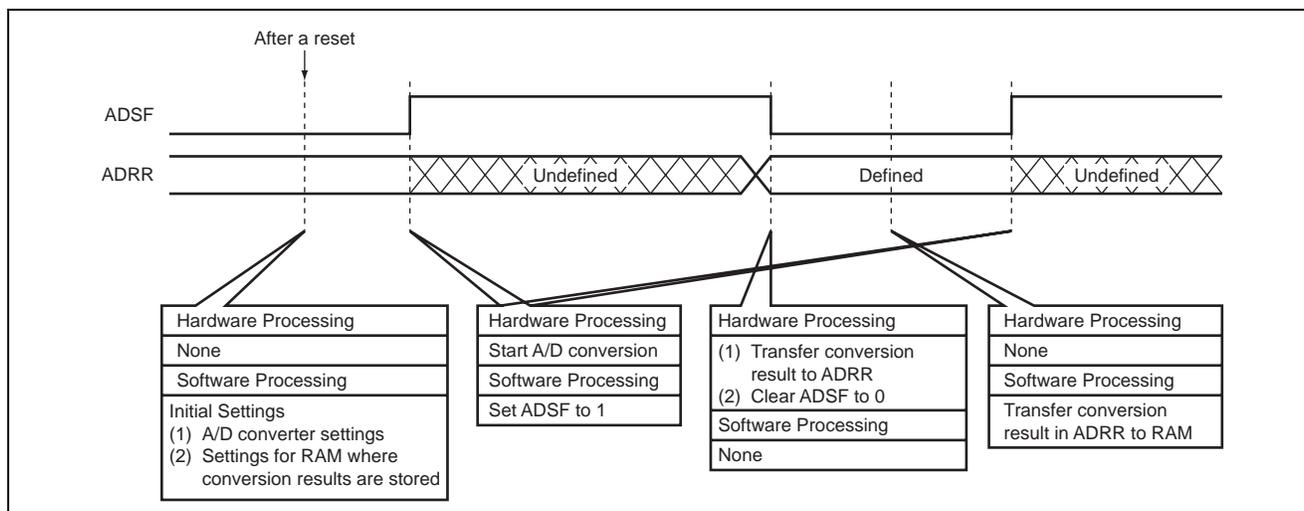


Figure 3 Principles of Operation of Voltage Measurement by A/D Conversion

3.1 Usage Notes

- **Permissible signal source impedance**
The analog input of the H8/38076R is designed to guarantee conversion accuracy for an input signal with a signal source impedance of 10 kΩ or less. This specification enables the A/D converter's sample-and-hold circuit input capacitance to be charged within the sampling time. If the sensor output impedance exceeds 10 kΩ, charging may be insufficient and it may not be possible to guarantee A/D conversion accuracy. However, if a large capacitance is provided externally, the input load will essentially comprise only the internal input resistance of 10 kΩ, and the signal source impedance will be unnecessary. However, as a low-pass filter effect is obtained in this case, it may not be possible to accurately convert analog signals having a large differential coefficient (e.g., 5 mV/μs or greater) in some cases. When converting high-speed analog signals, a low-impedance buffer should be inserted.
- **Influences on absolute accuracy**
Adding capacitance results in coupling with the ground, and therefore noise from the ground may adversely affect absolute accuracy. Be sure to make a connection to an electrically stable ground. Care is also required to ensure that filter circuits do not interfere with digital signals or act as antennas on the mounting board.
- **Usage notes**
The ADRR register should be read only when the ADSF bit in ADSR is cleared to 0.
Changing the digital input signal at an adjacent pin during A/D conversion may adversely affect conversion accuracy.
When A/D conversion is started after clearing the module standby mode, wait for 10 φ clock cycles before starting A/D conversion.
In the active mode and the sleep mode, the analog power supply current flows in the ladder resistor even when the A/D converter is on standby. Therefore, it is recommended that AVcc be connected to the system power supply and the ADCKSTP bit in CKSTPR1 be cleared to 0 if the A/D converter is not used.

4. Description of Software

4.1 Functions

Table 2 shows the functions used in this sample task.

Table 2 List of Functions

Function Name	Description
main	Initializes RAM area to be used, stores A/D conversion result
init_ad	Makes initial settings for A/D converter
meas_ad	Starts A/D conversion from arguments, returns result as return value
stop_ad	Sets A/D converter to the module standby mode

4.2 Constants

No constants are used in this sample task.

4.3 RAM Usage

The RAM usage in this sample task is shown in table 3.

Table 3 RAM Usage

Label Name	Description	Amount of Memory Used	Used in
data[0] to data[3]	Buffer for storing A/D conversion result	4 words	main

4.4 Modules

4.4.1 main() Function

1. Module Specifications

- Initializes RAM area to be used, stores A/D conversion result

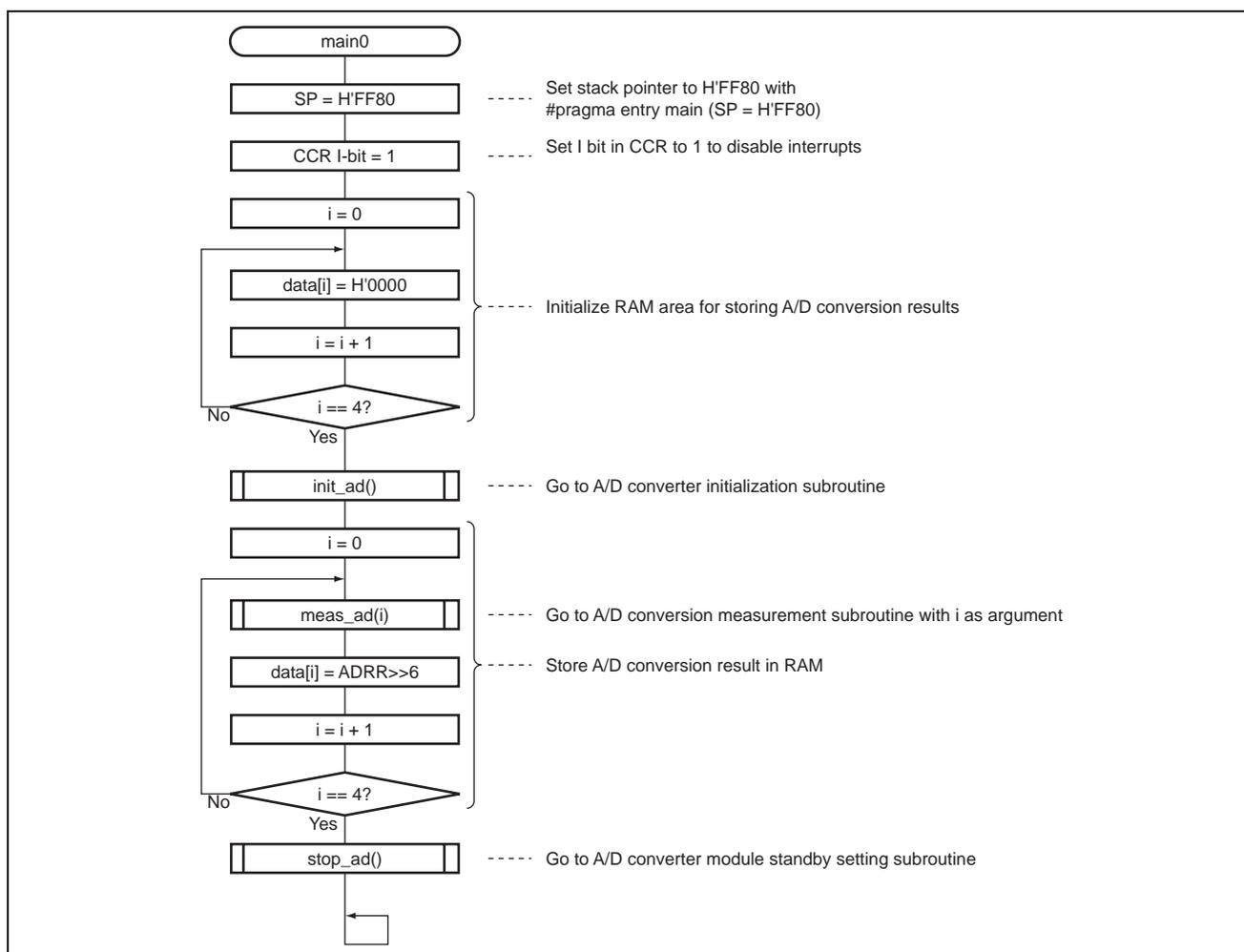
Table 4 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None
Return values	None	None	None

2. Internal Registers Used

No internal registers are used in this function.

3. Flowchart



4.4.2 init_ad() Function

1. Module Specifications

- Makes initial settings for A/D converter

Table 5 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None
Return values	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

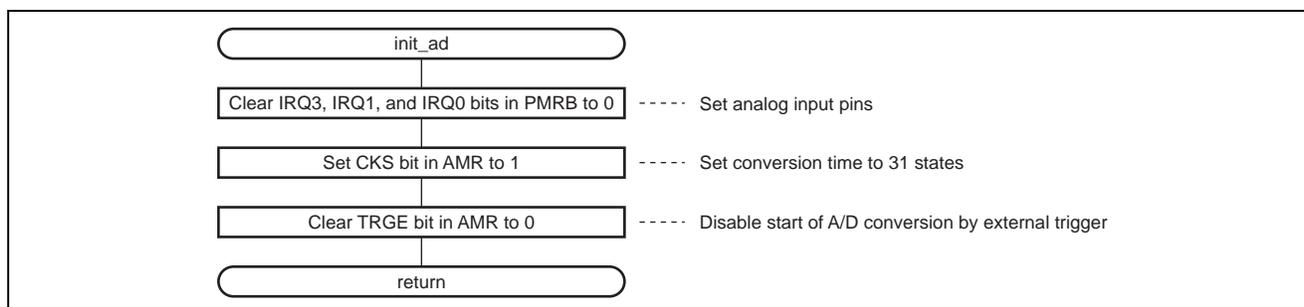
- AMR A/D mode register Address: H'FFBE

Bit	Bit Name	Set Value	R/W	Description
7	CKS	1	R/W	Clock selection Sets the A/D conversion time. 0: Conversion time = 62 states 1: Conversion time = 31 states
6	TRGE	0	R/W	External trigger selection Enables or disables start of A/D conversion by external trigger input. 0: A/D conversion start by external trigger input disabled 1: A/D conversion starts at rising or falling edge of ADTRG pin The edge of the ADTRG signal is selected by the ADTRGNEG bit in IEGR.
3	CH3	0	R/W	Channel selection 3 to 0
2	CH2	0	R/W	Selects the analog input channel.
1	CH1	0	R/W	00xx: No channel selected
0	CH0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 1010: AN6 1011: AN7 11xx: Use prohibited Channel selection should be made while the ADSF bit is cleared to 0. Legend: x: Don't care

- PMRB Port mode register B Address: H'FFCA

Bit	Bit Name	Set Value	R/W	Description
2	IRQ3	0	R/W	<p>PB2/AN2/IRQ3 pin function switch</p> <p>Selects whether pin PB2/AN2/IRQ3 is used as PB2/AN2 or as IRQ3.</p> <p>0: Functions as PB2/AN2 input pin</p> <p>1: Functions as IRQ3 input pin</p>
1	IRQ1	0	R/W	<p>PB1/AN1/IRQ1 pin function switch</p> <p>Selects whether pin PB1/AN1/IRQ1 is used as PB1/AN1 or as IRQ1.</p> <p>0: Functions as PB1/AN1 input pin</p> <p>1: Functions as IRQ1 input pin</p>
0	IRQ0	0	R/W	<p>PB0/AN0/IRQ0 pin function switch</p> <p>Selects whether pin PB0/AN0/IRQ0 is used as PB0/AN0 or as IRQ0.</p> <p>0: Functions as PB0/AN0 input pin</p> <p>1: Functions as IRQ0 input pin</p>

3. Flowchart



4.4.3 meas_ad() Function

1. Module Specifications

- Starts A/D conversion from arguments, returns result as return value

Table 6 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char	ch	Specifies the input channels to be used. The specified values of 0 to 7 correspond to AN0 to AN7.
Return values	unsigned short	—	Returns the A/D conversion result. The values of the upper 6 bits are 0 and values of the lower 10 bits are valid.

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- AMR A/D mode register Address: H'FFBE

Bit	Bit Name	Set Value	R/W	Description
3	CH3	Undefined	R/W	Channel select 3 to 0
2	CH2	Undefined	R/W	Selects the analog input channel.
1	CH1	Undefined	R/W	00xx: No channel selected
0	CH0	Undefined	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 1010: AN6 1011: AN7 11xx: Use prohibited Channel selection should be made while the ADSF bit is cleared to 0. Legend: x: Don't care.

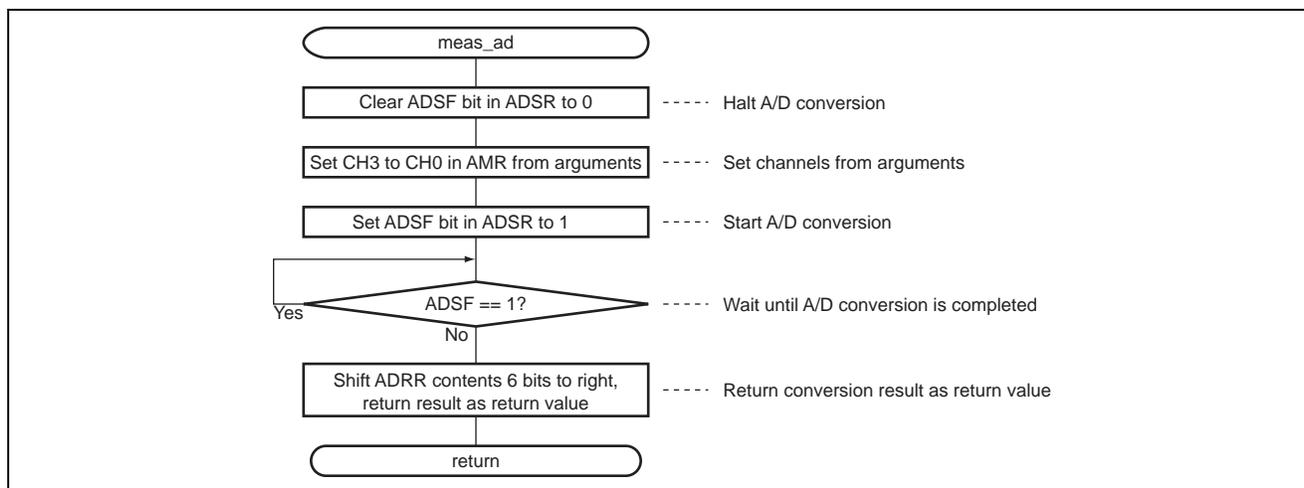
- ADSR A/D start register Address: H'FFBF

Bit	Bit Name	Set Value	R/W	Description
7	ADSF	1	R/W	A/D conversion starts when this bit is set to 1. When conversion is completed, the converted data is set in ADDR and at the same time this bit is cleared to 0. A/D conversion can be forcibly terminated by writing 0 to this bit.

- ADRR A/D result register Address: H'FFBC

Bit	Bit Name	Set Value	R/W	Description
15	ADR9	Undefined	R	ADRR is a 16-bit read-only register that stores the result of A/D conversion. The upper 10 bits of the data are stored in ADRR. ADRR can be read by the CPU at any time, but the ADRR values during A/D conversion is undefined. After A/D conversion is completed, the conversion result is stored as 10-bit data, and this data is retained until the next conversion operation starts. The initial value of ADRR is undefined.
14	ADR8	Undefined	R	
13	ADR7	Undefined	R	
12	ADR6	Undefined	R	
11	ADR5	Undefined	R	
10	ADR4	Undefined	R	
9	ADR3	Undefined	R	
8	ADR2	Undefined	R	
7	ADR1	Undefined	R	
6	ADR0	Undefined	R	

3. Flowchart



4.4.4 stop_ad() Function

1. Module Specifications

- Sets A/D converter to the module standby mode

Table 7 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- AMR A/D mode register Address: H'FFBE

Bit	Bit Name	Set Value	R/W	Description
3	CH3	0	R/W	Channel select 3 to 0
2	CH2	0	R/W	Selects the analog input channel.
1	CH1	0	R/W	00xx: No channel selected
0	CH0	0	R/W	0100: AN0 0101: AN1 0110: AN2 0111: AN3 1000: AN4 1001: AN5 1010: AN6 1011: AN7 11xx: Use prohibited Channel selection should be made while the ADSF bit is cleared to 0. Legend: x: Don't care.

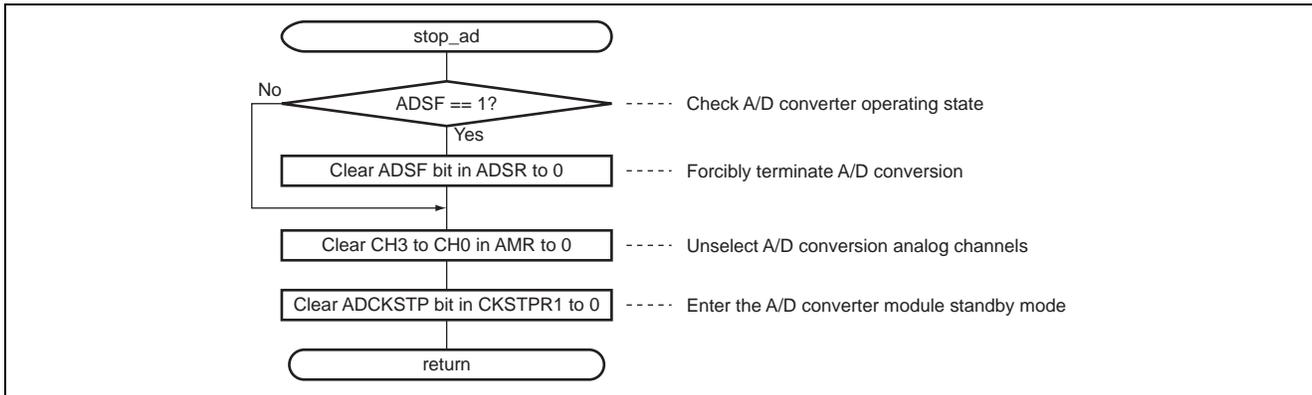
- ADSR A/D start register Address: H'FFBF

Bit	Bit Name	Set Value	R/W	Description
7	ADSF	0	R/W	A/D conversion starts when this bit is set to 1. When conversion is completed, the converted data is set in ADDR and at the same time this bit is cleared to 0. A/D conversion can be forcibly terminated by writing 0 to this bit.

- CKSTPR1 Clock stop register 1 Address: H'FFFA

Bit	Bit Name	Set Value	R/W	Description
4	ADCKSTP	0	R/W	A/D converter module standby The A/D converter enters the standby mode when this bit is cleared to 0.

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100
B	H'F780

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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