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April 1st, 2010
Renesas Electronics Corporation

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H8S Family

One-Shot Pulse Output

Introduction

Outputs a one-shot pulse, synchronizing with a falling edge of an external signal. The delay time from the falling edge and pulse width can be varied.

Target Device

H8S/2339

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1. Specifications

1. As shown in figure 1, this function outputs a one-shot pulse, synchronizing with the falling edge of the external signal.
2. The delay time from the falling edge of the external signal and pulse width can be changed within the following ranges. Set the reference pulse cycle shorter than the cycle set in TCNT0.
 - $1\ \mu\text{s} \leq \text{delay time} < \text{reference pulse cycle} - \text{pulse width}$
 - $50.86\ \text{ns} \leq \text{pulse width} < \text{reference pulse cycle} - \text{delay time}$

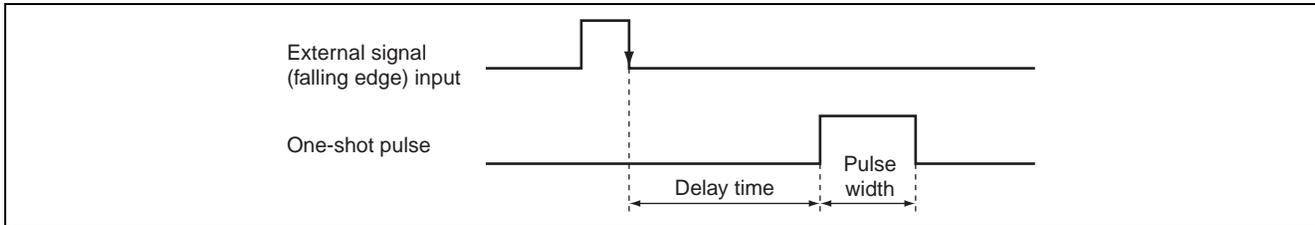


Figure 1 One-Shot Pulse Output

3. Principles of Operation

The principles of operations used are shown in figure 3. As shown in figure 3, a one-shot pulse is output by H8S/2339 hardware and software processing.

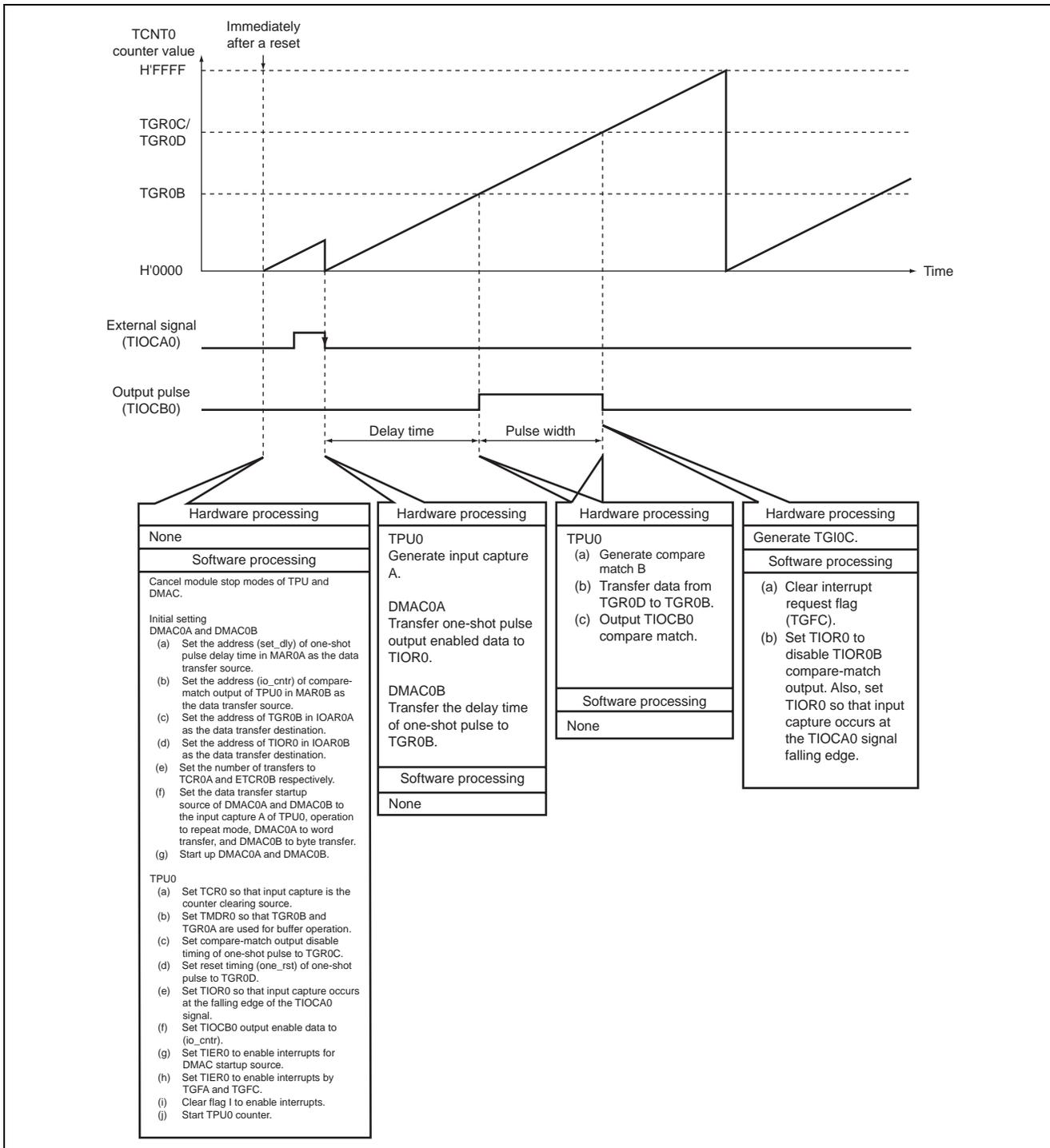


Figure 3 Principles of Operations Used of One-Shot Pulse Output

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	ONEMN	Sets the delay time and pulse width in TGR0B and TGR0D, and a one-shot pulse reset value to TGR0C to output a one-shot pulse.
Pulse output disabled	POUTDLE	Disables pulse output.

2. Description of Arguments

Label Name	Function	Data Length	Used in	I/O
set_dly	Sets a timer value that governs the delay time of one-shot pulse. The delay time is obtained by the following expression: Delay time (ns) = timer value × ϕ cycle (50.86 ns during 19.66-MHz operation)	unsigned short	Main routine	Input
one_rst	Sets a timer value that governs the reset timing of one-shot pulse. The reset timing is obtained by the following expression: Pulse reset timing (ns) = timer value × ϕ cycle (50.86 ns during 19.66-MHz operation)	unsigned short	Main routine	Input
io_cntr	Sets one-shot pulse output enabled data. (A falling edge is set as the input capture A detection edge and compare match B is toggled during output.)	unsigned char	Main routine	Output

3. Description of Internal Registers Used

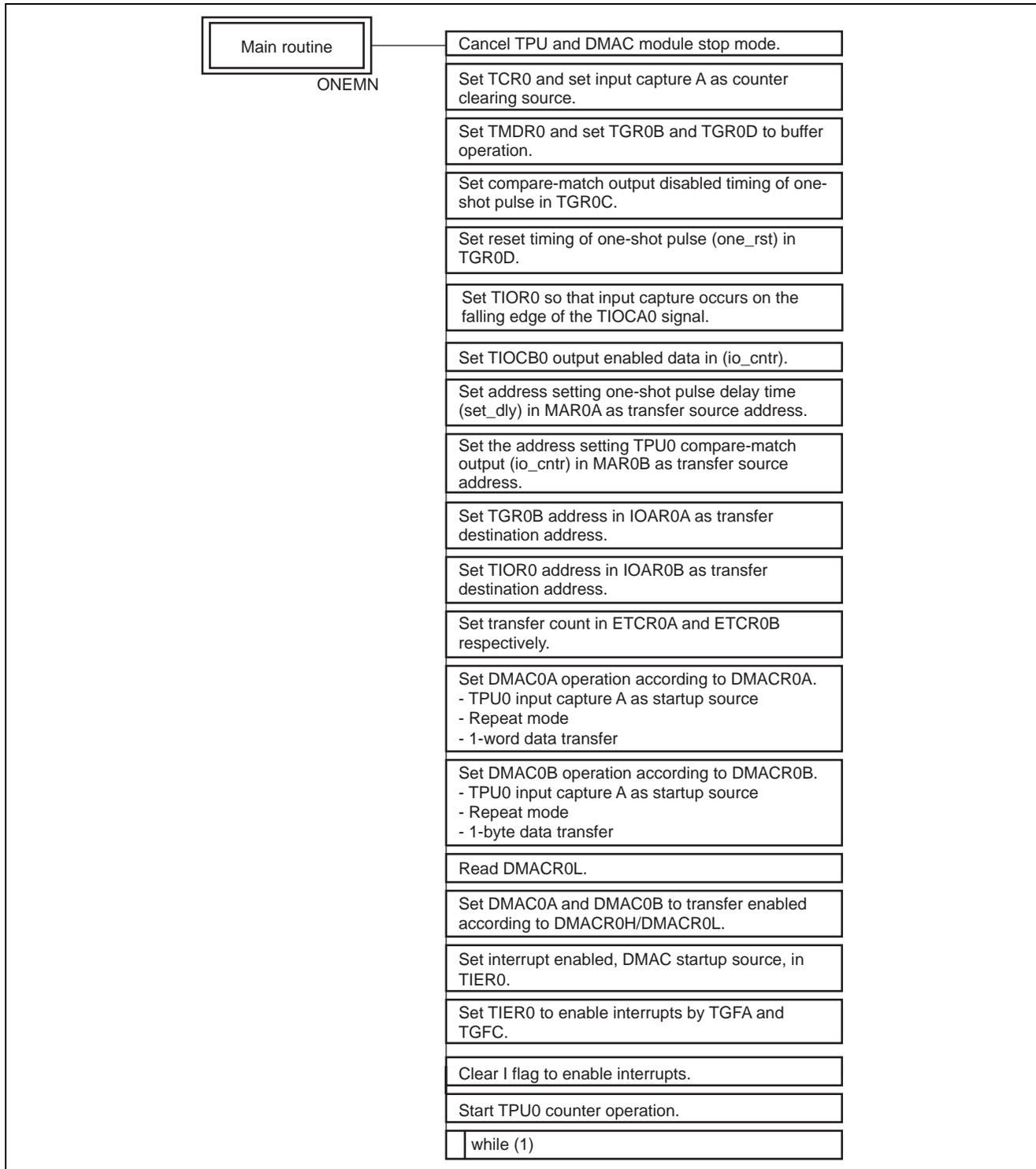
Register Name	Function	Used in	
TPU TSTR	Selects operation/stop of the timer counter.	Main routine	
TPU0	TMDR	Sets TGR0B and TGR0D to buffer operation.	
	TCR0	Sets a clock to be input to TCNT and a counter clearing source.	
	TIOR0	Detects a falling edge of an input pulse.	
		Sets a level to be output from TIOCB0 at occurrence of compare match B.	Pulse output disabled
	TIER0	Enables an interrupt by TGI0C.	Main routine/ pulse output disabled
	TSR0	Indicates occurrence of compare match by TGR0B.	Main routine
	TGR0B	Sets the delay time of one-shot pulse.	
	TGR0C	Sets a pulse output disabled timing value of one-shot pulse.	
	TGR0D	Sets a reset timing value of one-shot pulse.	
DMAC	DMABCR0 DMACR0A DMACR0B	Set the operation of each DMAC channel.	
	MAR0A MAR0B	Set the address of data to be transferred to each register.	
	IOAR0A IOAR0B	Set the transfer destination register address of each channel.	
	ETCR0A ETCR0B	Set the transfer count of each channel.	
	MSTPCR	Cancel the TPU and DMAC module stop mode.	

4. RAM Usage

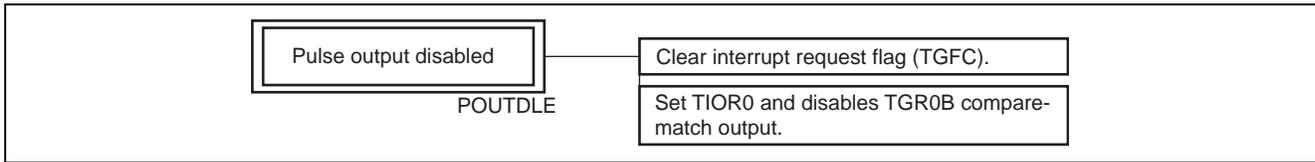
Label	Set Value of the Sample Task
io_cnr	H'39

5. PAD

1. Main Routine



2. Pulse Output Disabled



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Feb.17.05	—	First edition issued

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