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H8S Family

Output of Count-Specified Pulses

Introduction

Outputs as many 50% duty pulses as required (1 to 255).

Target Device

H8S/2339

Contents

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1. Specifications

- 1. As shown in figure 1, this sample task outputs as many 50% duty pulses as required.
- 2. The pulse cycle can be set to $0.81~\mu s$ to $104.17~\mu s$ in increments of $0.41~\mu s$ in approximately 20-MHz (19.6608 MHz) operation.

The number of pulses to be output can set from 1 to 255.

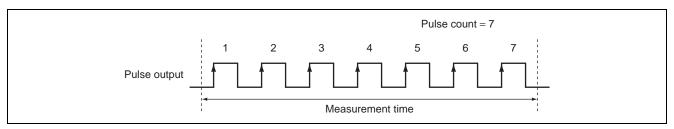


Figure 1 Pulse Output Timing



2. Description of Functions

- 1. The block diagram of the 8-bit timer to be used by this sample task is shown in figure 2. This sample task uses the following functions:
 - A. Function that cascade connects the 2-channel 8-bit timer and counts channel-0 compare match according to the channel-1 timer (compare match count mode).
 - B. Function that generates an interrupt to the set count.

This sample task uses the functions as shown in figure 2 to count pulse rising edges.

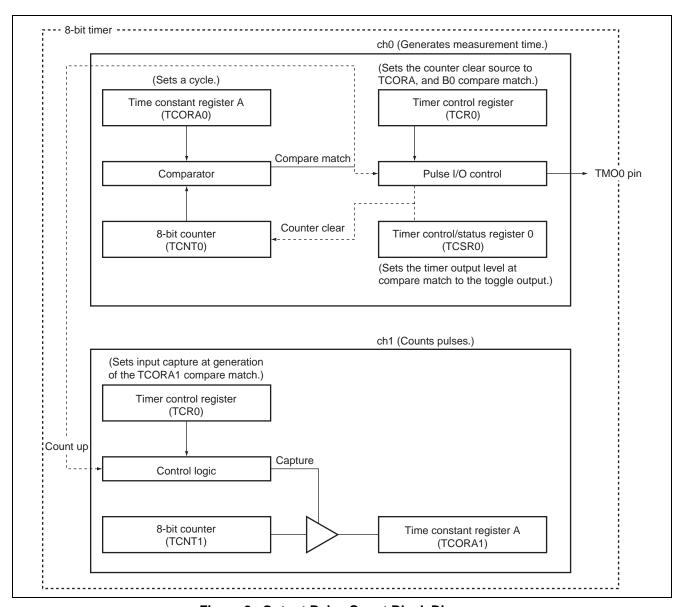


Figure 2 Output Pulse Count Block Diagram



3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs H8S/2339 hardware processing and software processing as shown in figure 3 to measure the number of pulses.

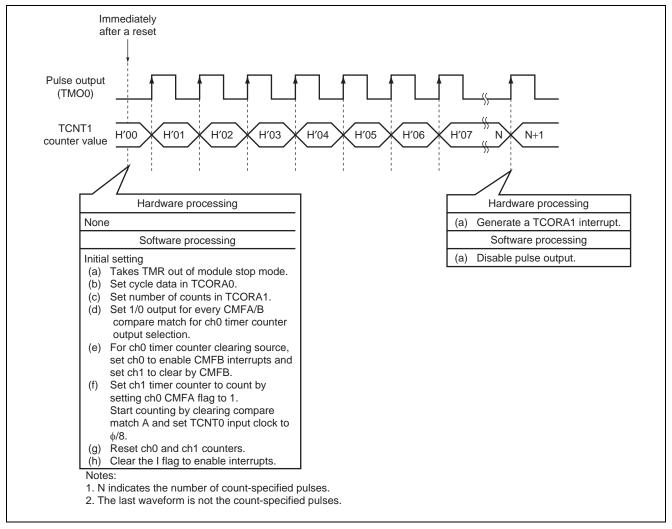


Figure 3 Principles of Operations Used for Measurement of the Number of Pulses



4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	pulsemn	Performs initial setting for the 8-bit timer.
Pulse output stop	pulend	Starts up by a TCORA1 interrupt, clears TCR and TCSR, and disables pulse output.

2. Description of Arguments

Element	Function	Data Length	Used in	I/O
pulse_cycle	Sets a pulse cycle.	1 byte	Main routine	Input
pulse_count	Sets the number of counted pulses.	1 byte	Main routine	Input

3. Description of Internal Registers Used

Element	Function	Used in	
TCORA0	Main routine		
TCORB0	TCORB0 Generates compare match B.		
TCSR0	Outputs 1 for each compare match A and outputs 0 for each compare match B.	Main routine, pulse output stop	
TCR0	Clears the counter at compare match A.	Main routine,	
	Selects the input clock (ϕ /8).	pulse output stop	
TCR1	Counts generation of the compare match A of channel 0.	Main routine,	
	Clears the counter at compare match A.	pulse output stop	
	Enables a compare match (A) interrupt.		
TCORA1	Generates compare match A.	Main routine	
TCNT0	Used to generate compare matches A and B.	Main routine	
TCNT1	Counts the number of times compare match A on channel 0 occurs.	Main routine	
MSTPCR	Cancels the 8-bit timer (TMR) module stop mode.	Main routine	

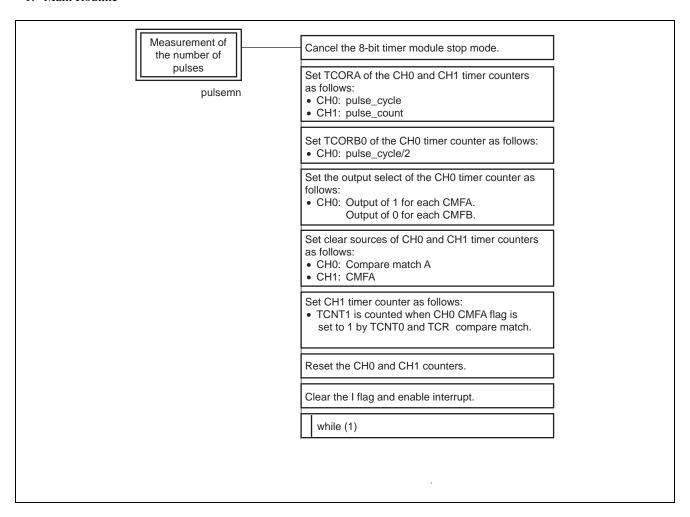
4. RAM Usage

Element	Value Set in this Sample Task
pulse_cycle	H'0A
pulse_count	H'07

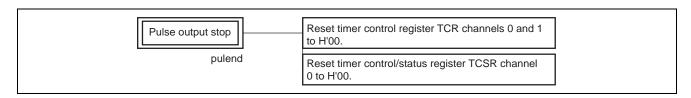


5. PAD

1. Main Routine



2. Pulse Output Stop





Revision Record

	Date	Description		
Rev.		Page	Summary	
1.00	Feb.17.05	_	First edition issued	



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