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H8S / 2200 Series

15-Phase PWM Output

Introduction

A 15-phase PWM waveform with variable duty cycle is output with the desired cycle.

Target Device

H8S / 2239

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1. Specifications

- (1) Outputs 15-phase PWM waveforms with variable duty cycles, as shown in figure 1.
- (2) In operation at 20 MHz, the period of the output PWM signal can be set to any desired value from 100 ns to 3.27 ms.

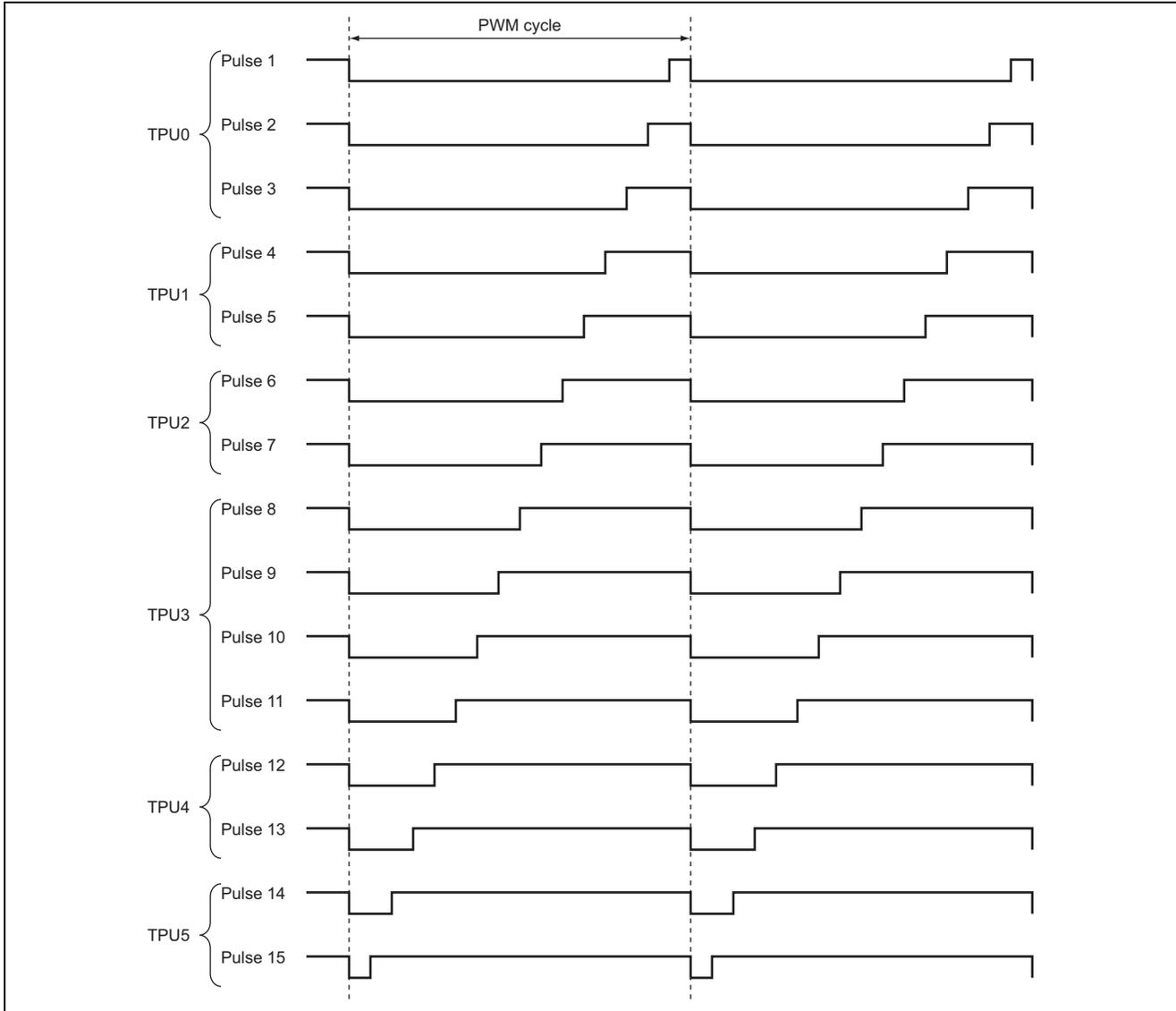


Figure 1 Example of PWM-Waveform Output

2. Description of Module Usage

- (1) TPU0 to TPU5 operate in synchronization to produce 15 PWM waveforms with different phases.
- (a) Figure 2 is a block diagram of how the TPUs are used in this sample task, which demonstrates how up to 15 PWM waveforms with different phases can be output through synchronized operation of the TPU functions (PWM mode 2).

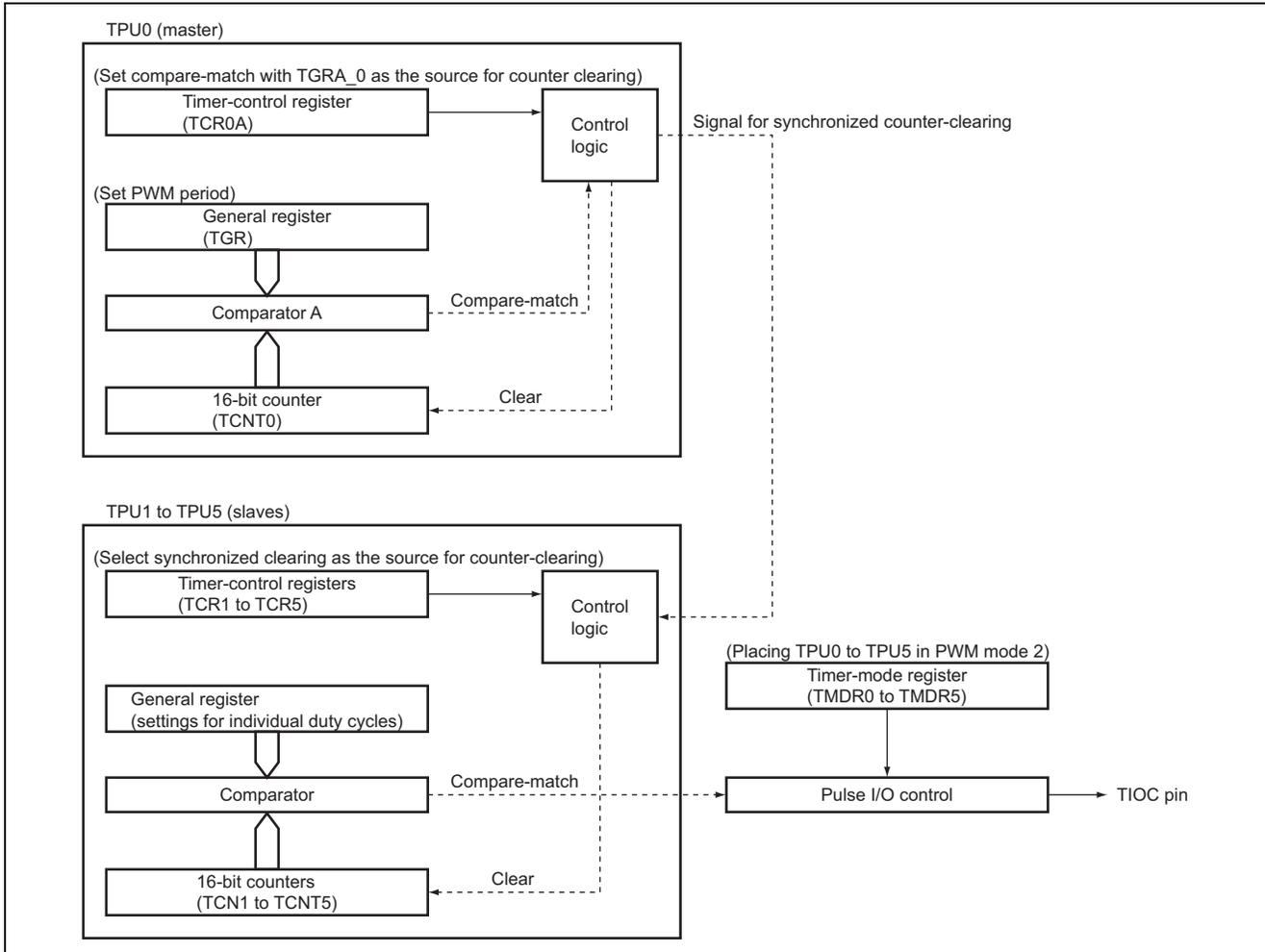


Figure 2 15-Phase PWM Output

(2) Used functions in this sample task are described in table 1. The output of fifteen PWM pulse trains, each with a different phase, is achieved by using the functions in the ways described in the table.

Table 1 Assignment of Functions

Element	Usage
TIOCA1 to TIOCA5	PWM pulse output pins
TIOCB0 to TIOCB5	PWM pulse output pins
TIOCC0, TIOCC3	PWM pulse output pins
TIOCO1, TIOCO3	PWM pulse output pins
TCR0 to TCR5	Selects the source for clearing of timer-counters TPU0 to TPU5
TMOR0 to TMOR3	Places TPU0 to TPU5 in PWM mode 2
TGRA_0	Sets the PWM period
TGRB_0 to TGRB_5	Sets the duty-cycle values

3. Principles of Operation

The principle of operation for 15-phase PWM output is shown in figure 3. As the figure shows, the pulse trains are output on the PWM-output pins, TPU0 to TPU5, through a combination of hardware and software processing.

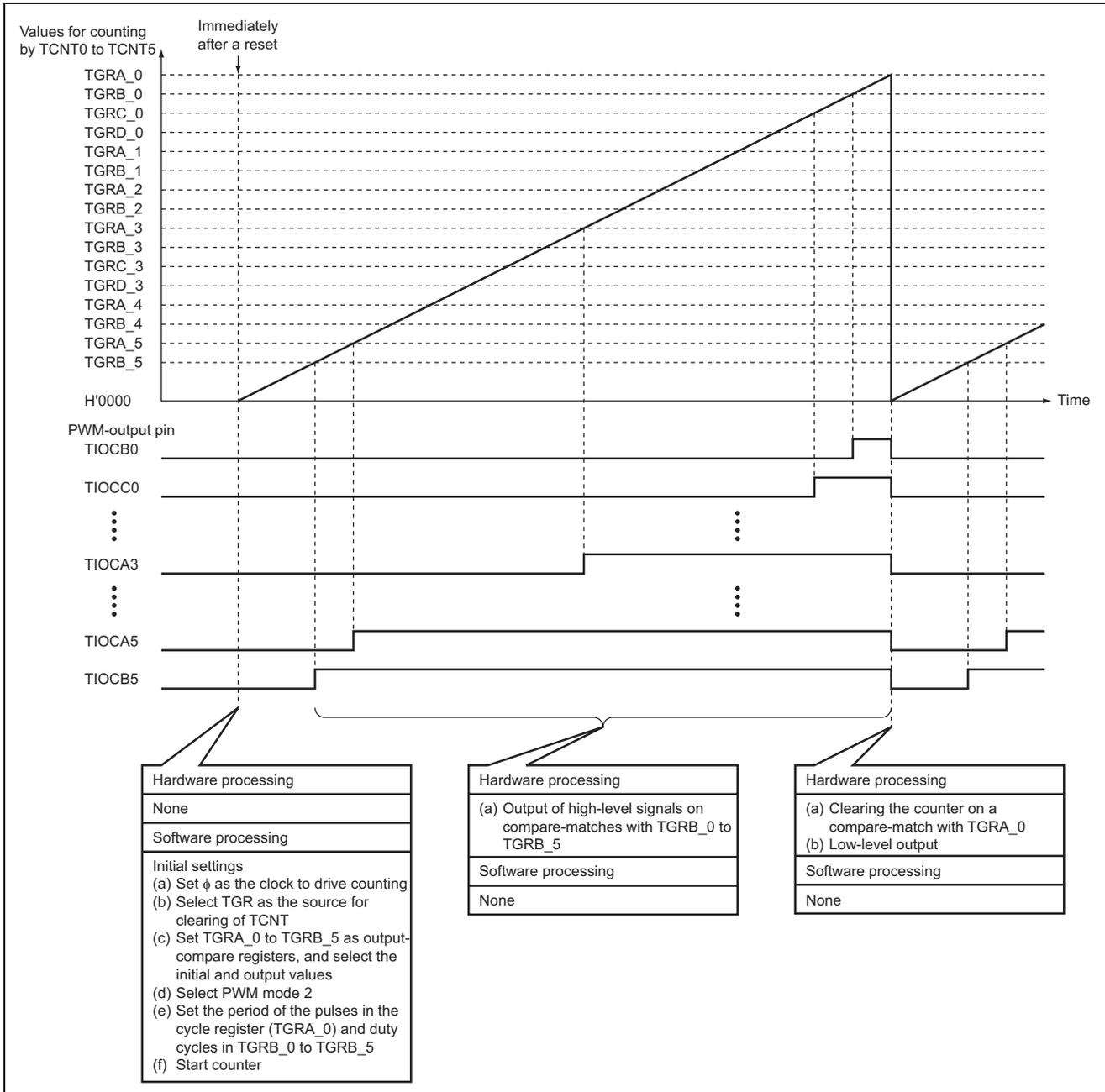


Figure 3 Principle of Operation for 15-Phase PWM Output

4. Software Description

(1) Function

Function	Label	Description
Main routine	pwrn15mn	Settings for simultaneous clearing of channels 0 to 5 and PWM output

(2) Arguments

Label	Description	Data Type	Used in	I/O
pwm[0] to pwm[14]	The timer-counter settings for high pulse width The following expression governs pulse width. Pulse width (ns) = timer-counter value x ϕ period (50 ns in operation at 20 MHz) x frequency divisor for the input clock on each channel	unsigned short	Main routine	Input
pwm_cycl	The timer-counter setting for PWM period. The following expression governs PWM period. PWM period (ns) = timer-counter value x ϕ period (50 ns in operation at 20 MHz) x frequency divisor for the input clock on each channel unsigned short	unsigned short	Main routine	Input

(3) Internal Registers

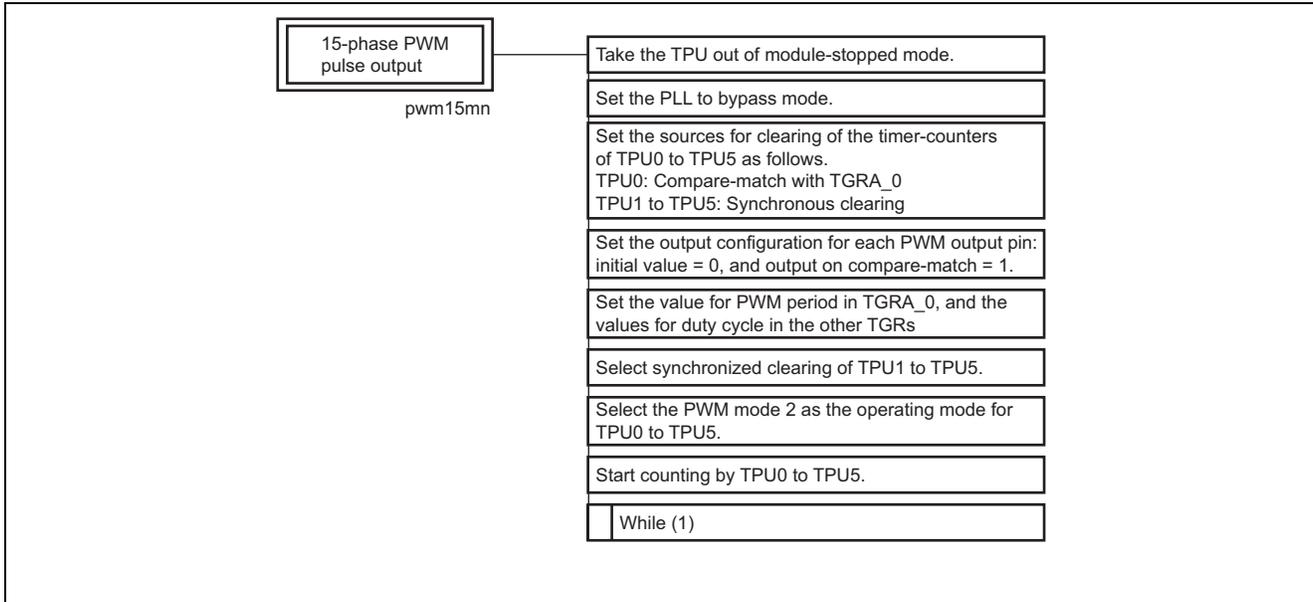
Register	Description	Used in
TSTR	Starts and stops counting by the timer counters of TPU0 to TPU5.	Main routine
TSYR	Selects synchronous operation for the timer counters of TPU0 to TPU5	Main routine
TCR0	Sets compare-match with TGRA_0 as the source for clearing the timer counters	Main routine
TCR1 to TCR5	Sets synchronous clearing as the source for clearing of the timer counters	Main routine
TIOR0 to TIOR5	Sets output on each of the PWM output pins	Main routine
TMDR0 to TMDR5	Selects PWM mode 2	Main routine
TGRA_0	Sets the PWM cycle	Main routine
TGRB_0 to TGRB_5	Sets the timer-counter values at which the levels on the PWM output pins go high	Main routine
MSTPCR	Takes the TPU out of module-stopped mode	Main routine

(4) RAM Usage

In this sample task, no RAM is used other than that for argument storage.

5. PAD

(1) Main routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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