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H8S/2200 Series

Key Input Recognition Processing by Means of the I/O Port

Introduction

A 4×4 key matrix is connected to the I/O port, and pressed keys are recognized.

Target Device

H8S/2215

Contents

| | |
|----------------------------------|---|
| 1. Overview..... | 2 |
| 2. Configuration | 2 |
| 3. Description of Functions..... | 3 |
| 4. Principles of Operation | 4 |
| 5. Sample Program | 6 |
| 6. Flowcharts | 7 |
| 7. Reference | 9 |

1. Overview

Sixteen keys (comprising a 4×4 key matrix) are connected to the I/O port, and pressed keys are recognized.

2. Configuration

The configuration on which the contents of this Application Note has been confirmed is shown below.

Table 1 Parts Used

| No. | Parts (Manufacturer) | Type Name | Specifications |
|-----|---|-----------------|---|
| 1 | H8S/2215 CPU board (from Hitachi ULSI Systems) | Solution Engine | Board power supply input: 5 VDC Operating frequency: 16 MHz MCU operating mode: 7 |
| 2 | 4 × 4 key matrix | — | Sixteen bipolar tactile switches |

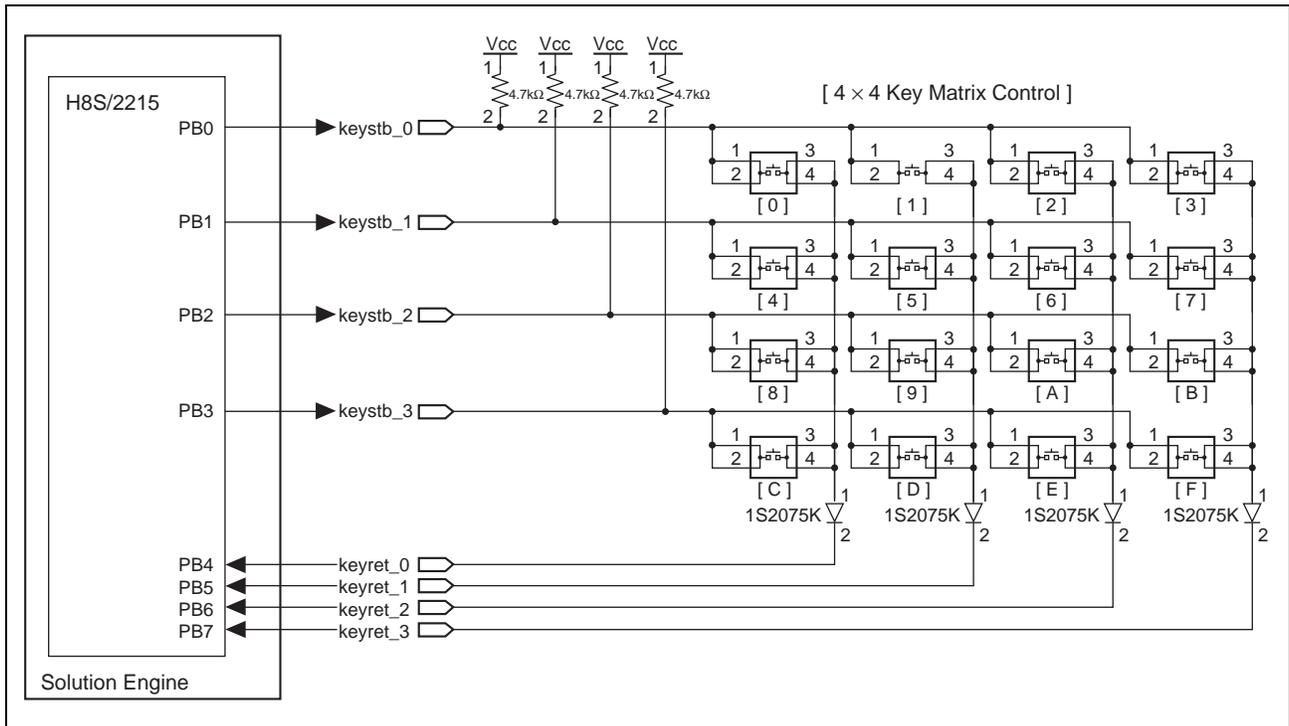


Figure 1

3. Description of Functions

Sixteen keys (comprising a 4×4 key matrix) are connected to the I/O port, and the pressed keys are recognized.

Key numbers are stored in an area assigned in the internal RAM.

If multiple keys are pressed simultaneously, the lowest key number is stored.

| Internal RAM Area Name | Data Length | Function |
|-------------------------------|--------------------|----------------------------------|
| key_no | unsigned char | Key number storage area (0 to F) |
| key_onf | int | "1" when a key is pressed |

4. Principles of Operation

4.1 Initialization Processing

Before key recognition processing is performed, the microcomputer is started up and the following initial internal register settings are made.

(1) Low-Power Consumption Control and Clock Oscillator Initialization

Register Name

| ← Set Value | Bit | Bit Name | Set Value | Description |
|-------------|---------|------------|------------|---|
| LPWRCR | 7:4 | — | 0000 | |
| ← H'03 | 3 | RFCUT | 0 | Uses internal feedback resistance control |
| | 2 | — | 0 | |
| | 1:0 | STC[1:0] | 11 | PLL is bypass |
| MSTPCRA | 7 | MSTPA7 | 0 | DMAC module operation |
| ← H'0D | 6 | MSTPA6 | 0 | DTC module operation |
| | 5 | MSTPA5 | 0 | TPU module operation |
| | 4 | MSTPA4 | 0 | TMR module operation |
| | 3:2 | MSTPA[3:2] | 11 | Reserved |
| | 1 | MSTPA1 | 0 | A/D converter operation |
| | 0 | MSTPA0 | 1 | Reserved |
| | MSTPCRB | 7 | MSTPB7 | 0 |
| ← H'1F | 6 | MSTPB6 | 0 | SCI_1 module operation |
| | 5 | MSTPB5 | 0 | SCI_2 module operation |
| | 4:1 | MSTPB[4:1] | 1111 | Reserved |
| | 0 | MSTPB0 | 1 | USB module stoppage |
| | MSTPCRC | 7:6 | MSTPC[7:6] | 11 |
| ← H'DF | 5 | MSTPC5 | 0 | D/A converter operation |
| | 4:0 | MSTPC[4:0] | 11111 | Reserved |

(2) I/O Port Initialization

The port B input/output mode is set.

| Port | Register Name | | | | |
|------|---------------|-----|------------|-----------|-------------|
| | ← Set Value | Bit | Bit Name | Set Value | Description |
| B | PBDDR | 7:4 | PB[7:4]DDR | 0000 | Input |
| | ← H'0F | 3:0 | PB[3:0]DDR | 1111 | Output |

4.2 Key Input Recognition Processing by Means of the I/O Port

(1) Overview

An interrupt is generated every 10 ms using the TMR_0 timer. Key input recognition processing is performed in the interrupt processing.

(2) TMR_0 Settings

Register settings are made so that 8-bit timer TMR_0 is interrupted every 10 ms.

| No. | Setting | Set Register |
|-----|--|--------------|
| 1 | TCORA_0 is set so that compare match A occurs approximately every 10 ms. Set value depends on microcomputer operating frequency and TCNT count cycle (values set to the CKS[2:0] bits of TCR). | TCORA_0 ← 20 |
| 2 | <ul style="list-style-type: none"> • Interrupt request by compare match A (CMFA) enabled • TCNT cleared by compare match A • TCNT count cycle set to $\phi/8192$ | TCR_0 ← H'4B |

(3) Key Number Recognition

In the interrupt processing for a TMR_0 compare match A interrupt generated every 10 ms, which key of the 4×4 key matrix was pressed is recognized. The key that was pressed is recognized by driving one of the pins in port B, PB[3:0] (keystb_[3:0]) low and reading one of the pins in port B, PB[7:4] (keyret_[3:0]).

If multiple keys are pressed simultaneously, the lowest key number is recognized.

| Port Name | Corresponding Signal Name | Pressed Key Number when PB7 = 0 | Pressed Key Number when PB6 = 0 | Pressed Key Number when PB5 = 0 | Pressed Key Number when PB4 = 0 |
|-----------|---------------------------|---------------------------------|---------------------------------|---------------------------------|---------------------------------|
| PB0←0 | Keystb_0 | 0 | 1 | 2 | 3 |
| PB1←0 | Keystb_1 | 4 | 5 | 6 | 7 |
| PB2←0 | Keystb_2 | 8 | 9 | A | B |
| PB3←0 | Keystb_3 | C | D | E | F |

To eliminate chattering, a key number is checked again 20 ms after it has been recognized, and the key number is stored in the area assigned in internal RAM only if the key number is the same on both occasions.

5. Sample Program

5.1 File Configuration

The sample program is provided as an HEW (High-performance Embedded Workshop) project. When h8s.hws is executed, HEW is started up and the source program can be referenced or modified. Users who do not have HEW should use an editor or similar software to refer directly to the following source files.

| No. | File Name | Purpose |
|-----|------------|--|
| 1 | resetprg.c | This file is executed from reset vector address 0 when a reset is input to the microcomputer. |
| 2 | intprg.c | This file is executed in the event of generation of an interrupt from an interrupt source other than a reset. |
| 3 | dbstc.c | Processing that sets the start address and end address of a section used by the _INITSTCT function in resetprg.c in the section initialization table. For the contents, see section 9.10 of the H8S, H8/300 Series C/C++ Compiler, Assembler, and Optimizing Linkage Editor User's Manual. This manual can be obtained from Renesas Technology's home page*. |
| 4 | key_scan.c | Main routine and interrupt processing routine of this Application Note |
| 5 | iodefne.h | H8S/2215 internal register structure definition file Partial modifications are added to the file generated automatically by HEW. See the source code for the location of the modifications. Modification locations are not directly relevant to this Application Note. |
| 6 | stacksct.h | Defines the stack size. |

Note: * <http://www.renesas.com>

5.2 Linkage

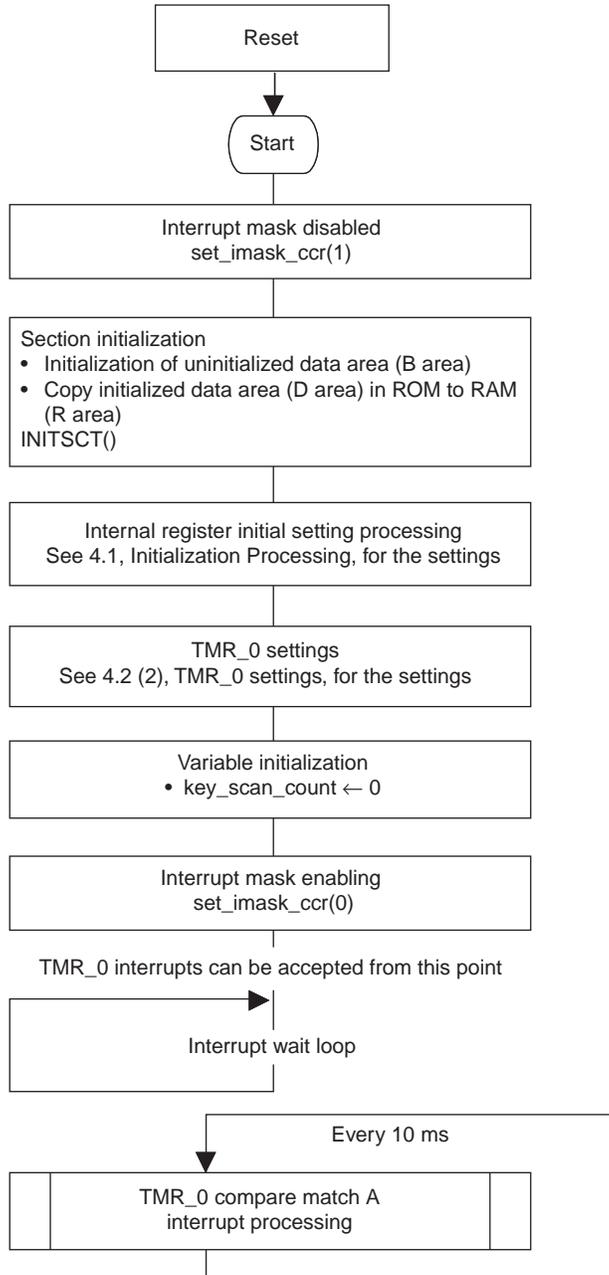
The linkage addresses of the various sections are shown below.

With the HEW project file, referencing and setting can be performed by selecting option –Standard Toolchain option — Link/Librarq tab — Category: section.

| Section | Start Address |
|-----------|---------------|
| PResetPRG | H'000400 |
| PIntPRG | |
| P | H'000800 |
| C | |
| C\$DSEC | |
| C\$BSEC | |
| D | |
| B | H'FFB000 |
| R | |
| S | H'FFEDB0 |

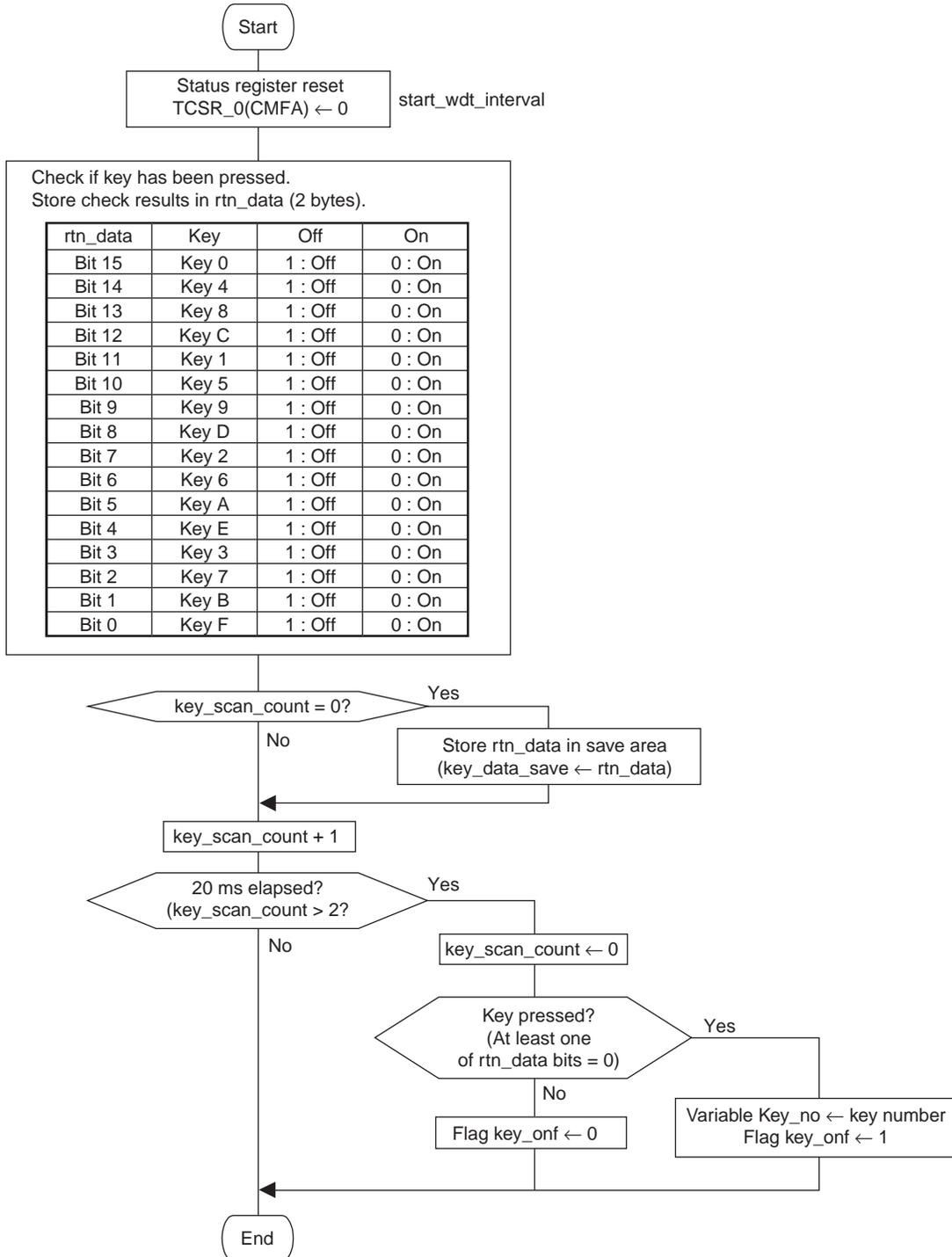
6. Flowcharts

(1) Overall Flow



(2) Interrupt Processing

TMR_0 compare match A interrupt processing (interrupt every 10 ms): tmr_cmia_0



7. Reference

| No. | Document Title | Source |
|-----|--|---|
| 1 | H8S/2215 Hardware Manual (REJ09B0140-0400O) | Can be downloaded from Renesas Technology's home page* |

Note: * [http:// www.renesas.com](http://www.renesas.com)

Revision Record

| Rev. | Date | Description | |
|------|-----------|-------------|----------------------|
| | | Page | Summary |
| 1.00 | Sep.03.04 | — | First edition issued |
| | | | |
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