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Renesas Electronics Corporation

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H8S/2200 Series

Blinking of LEDs Connected to I/O Ports

Introduction

Two LEDs connected to the ports of the H8S/2215 are alternately turned on and off. The interval of the on/off action is set by the watchdog timer.

Target Device

H8S/2215

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1. Specifications

1. As shown in figure 1, the two LEDs connected to the I/O ports are alternately turned on and off.
2. The watchdog timer is used to control the interval of the on/off action, and LED0 and LED1 are alternately turned on and off.
3. LED0 and LED1 are connected to the PA0 pin (pin 30) and PA1 pin (pin 31), respectively, of port A.

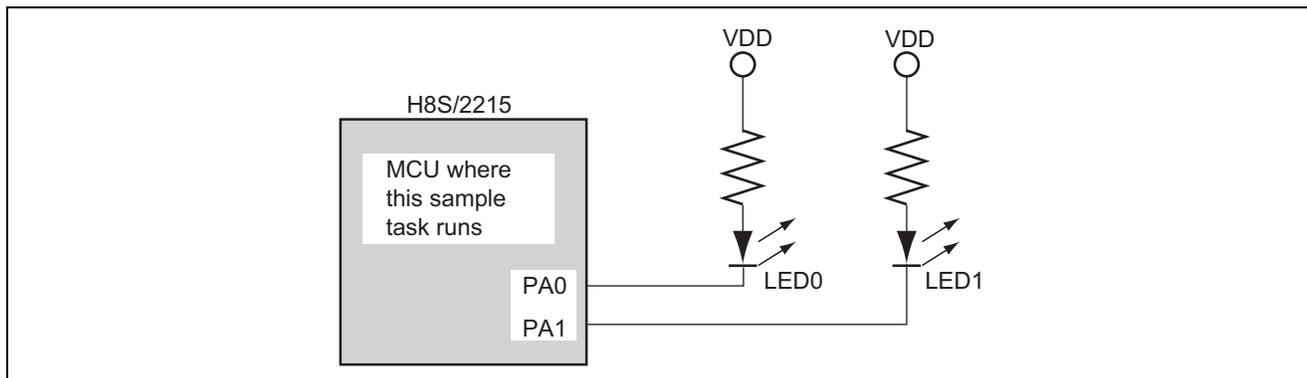


Figure 1 Blinking of LEDs Connected to I/O Ports

2. Description of Functions

1. The upper part of figure 2 shows the block diagram of the interval timer, and the following is the description of the block diagram:
 - The timer counter (TCNT) is an 8-bit up counter that can be read from or written to. TCNT is initialized to H'00 when the TME bit of the timer control/status register (TCSR) is 0.
 - The timer control/status register (TCSR) selects the input clock for TCNT, timer mode, etc.
 - The reset control/status register (RSTCSR) controls the generation of internal reset signal by TCNT overflow and selects the type of internal reset signal. RSTCSR is initialized to H'1F when a reset signal is input from the RES pin; however, it will not be initialized by the internal reset signal produced on WDT overflow.

To use WDT in interval timer mode, set WT/IT = 0 and TME = 1 in the TCSR register. In interval timer mode, an interval timer interrupt (WOVI) is generated every time TCNT overflows, which allows execution of interrupt operation at regular intervals.
2. The lower part of figure 2 shows the signal routes to port A, and the following is the description of port A registers:
 - The port A data direction register (PADDDR) bits specify input/output for individual pins of port A.
 - The port A data register (PADR) stores output data for each port A pin.
 - The port A register (PORTA) indicates port A pin states.

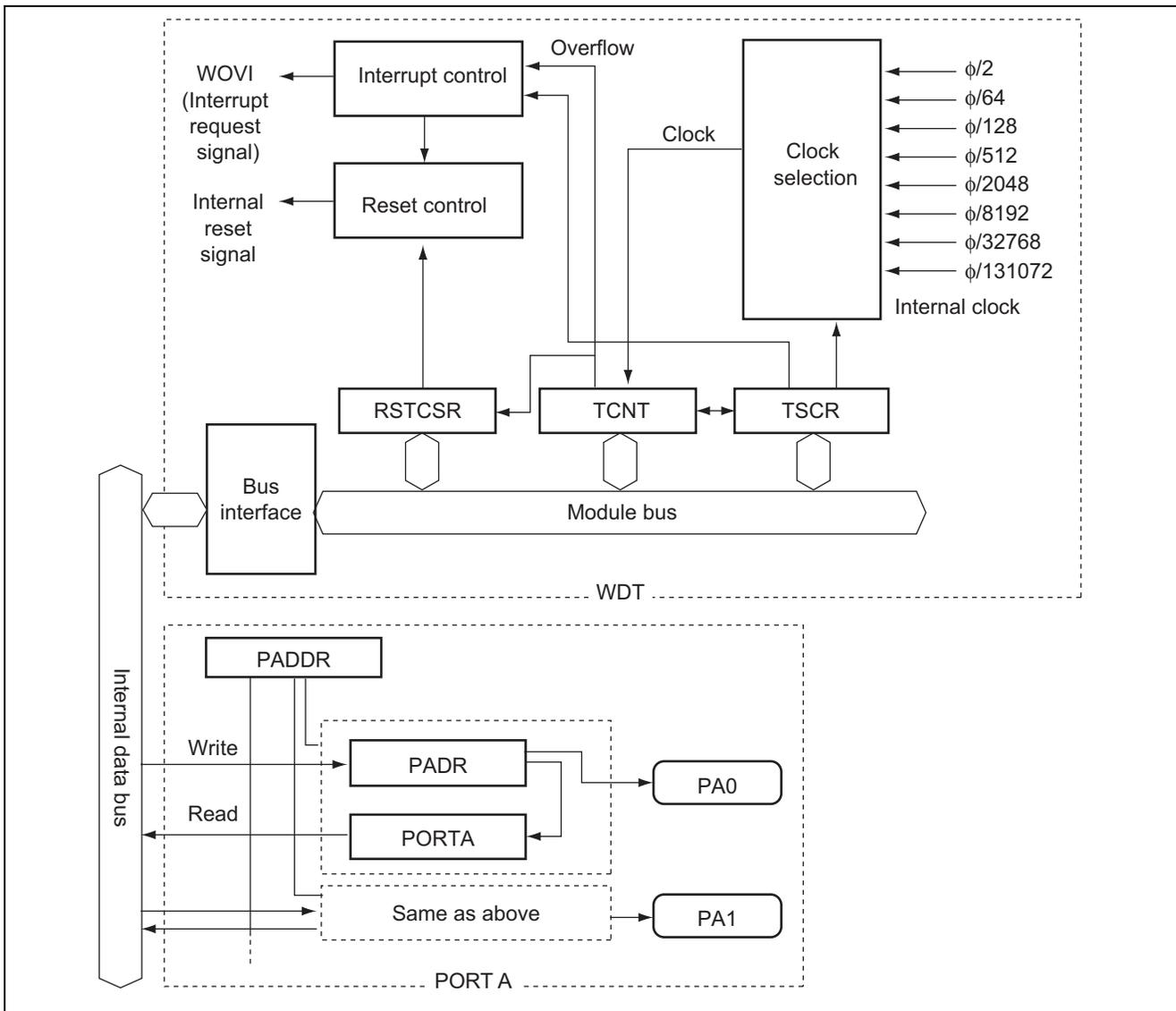


Figure 2 WDT and Signals Output from Port A Pins for This Sample Task

2. Table 1 shows the assignment of functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
TCNT	8-bit up counter
TCSR	Register that selects a clock input to TCNT and sets timer mode.
RSTCSR	Controls the internal reset signal produced on TCNT overflow.
PADDR	Sets the use of PA0 and PA1 pins.
PADR	Stores output data for each of the pins (PA0 to PA3).
PORTA	When read, states of port A pins or the states held in PADR can be read.

3. Principles of Operation

Figure 3 shows the principle of operation. LEDs connected to I/O ports are made to blink through the hardware and software processing shown in the figure.

1. Counting by the watchdog timer (WDT), set up as an interval timer, starts.
2. On an overflow of the timer counter, execution shifts to the LED blink processing routine.
3. In the LED blink processing routine, 1 and 0 are set alternately for output from the PA0 and PA1 pins of port A.

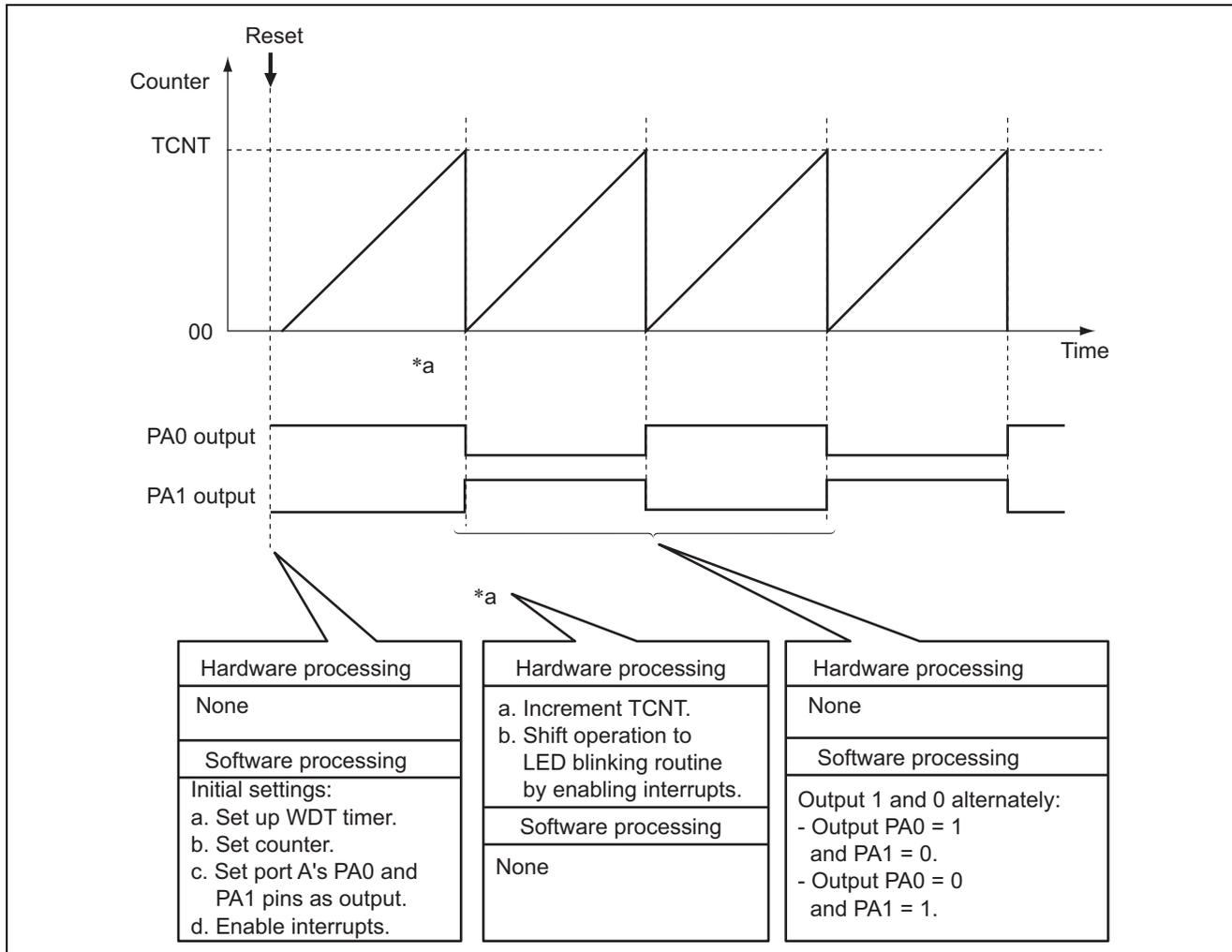


Figure 3 Blinking Operation of LEDs Connected to I/O Ports

4. Description of Software

4.1 Module

Table 2 describes the module used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Sets up the watchdog timer as an interval timer and executes counting. When the timer overflows, execution shifts to the LED blink processing routine.
LED blink processing	wovii	Timer interrupt processing routine that sets 0 or 1 alternately for the PA0 and PA1 pins of port A.

4.2 Arguments

This sample task does not use an argument.

4.3 Internal Registers

The internal registers used in this sample task are described in table 3.

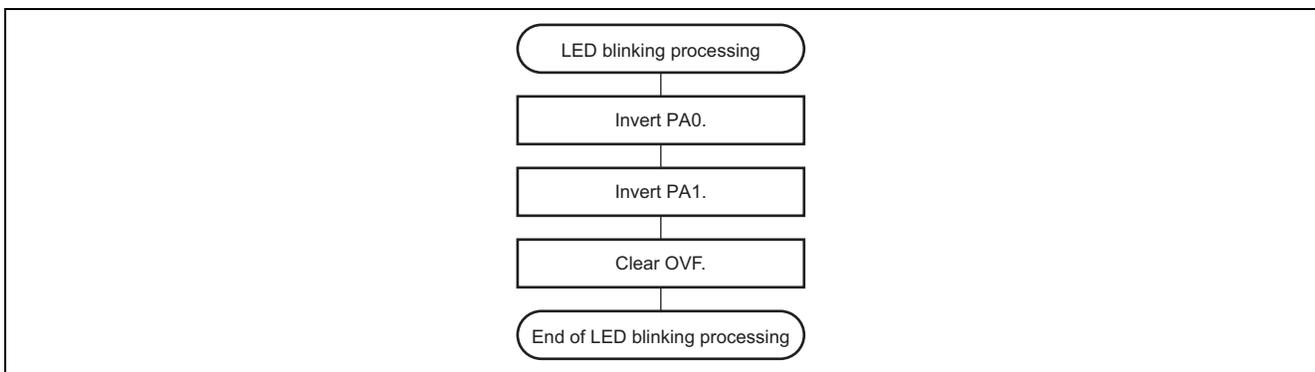
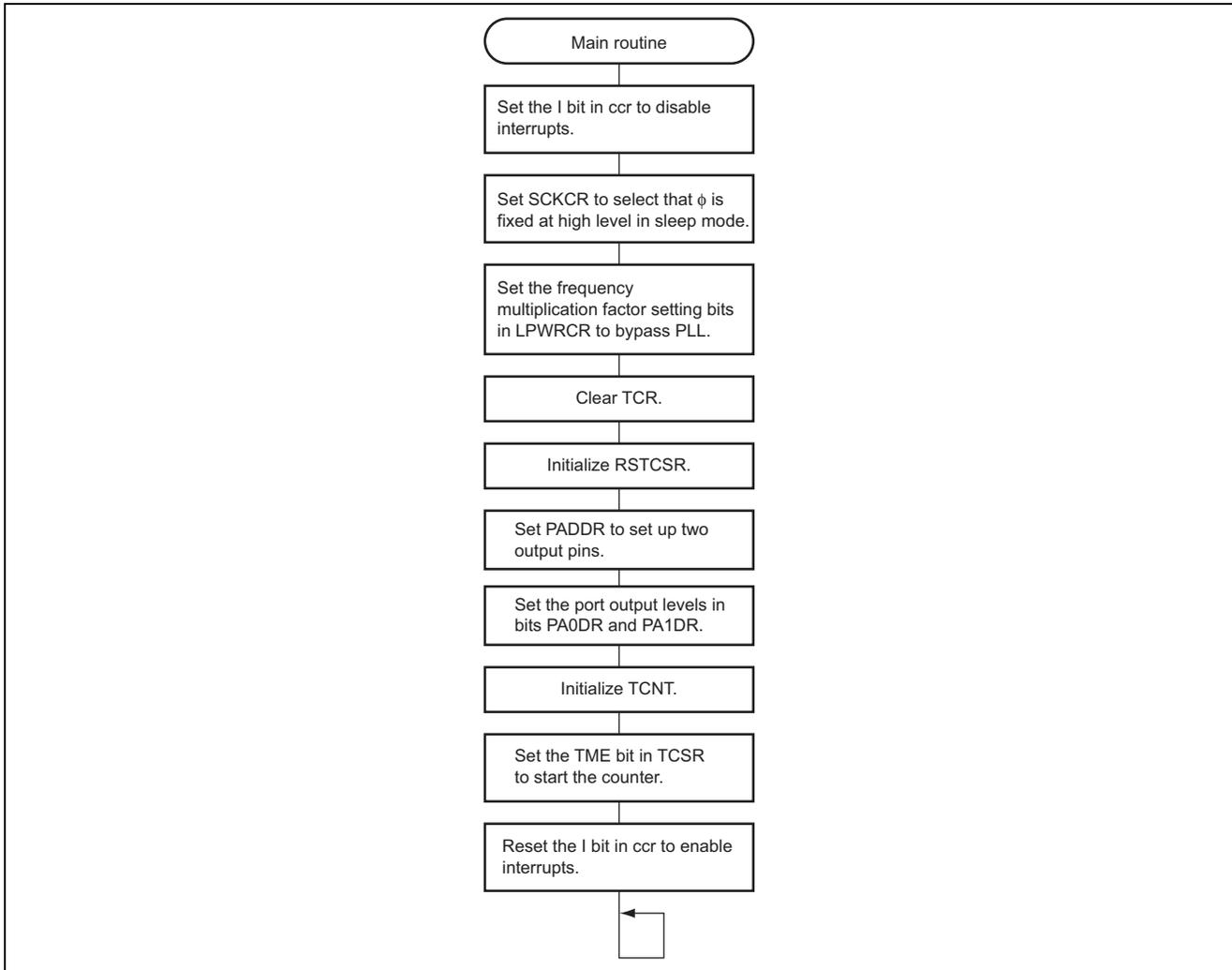
Table 3 Description of Internal Registers

Register	Function	Address	Setting
TCNT	Timer Counter 8-bit up counter that can be read from or written to	H'FFFF74 (for write) H'FFFF75 (for read)	H'00 when TME of TCSR is 0
TCSR	OVF Timer Control/Status Register (Overflow Flag) (Write is only possible for flag clearing.) OVF = 0 indicates that a TCNT overflow has not occurred. OVF = 1 indicates that a TCNT overflow has occurred.	H'FFFF74 Bit 7	0
	WT/ \overline{IT} Timer Control/Status Register (Timer Mode Select) When WT/ \overline{IT} = 0, interval timer mode is selected. When WT/ \overline{IT} = 1, watchdog timer mode is selected.	H'FFFF74 Bit 6	0
	TME Timer Control/Status Register (Timer Enable) When TME = 0, counting by TCNT is stopped. When TME = 1, counting by TCNT is started.	H'FFFF74 Bit 5	0
—	Timer Control/Status Register (Reserved) These bits cannot be written to; always read as "1".	H'FFFF74 Bits 4, 3	1, 1
CKS2	Timer Control/Status Register (Clock Select 2 to 0)	H'FFFF74	0, 0, 0
CKS1	These bits select an input clock among from eight clocks.	Bits 2, 1, 0	
CKS0	In this sample task, CKS2, CKS1 and CKS0 are set to 000, which sets overflow at $\phi/2$ (32 μ s) intervals. ϕ = 16 MHz		

Register	Function	Address	Setting
RSTCSR	WOVF	Reset Control/Status Register (Watchdog Timer Overflow Flag) (Write is only possible for flag clearing.) WOVF = 0 indicates that TCNT has not overflowed (or cleared). WOVF = 1 indicates that TCNT has overflowed (H'FF → H'00).	H'FFFF76 0 (for write) H'FFFF77 (for read) Bit 7
RSTCSR	RSTE	Reset Control/Status Register (Reset Enable) When RSTE = 0, only TCNT and TCSR are reset on TCNT overflow (internal reset is not induced). When RSTE = 1, an internal reset is induced on TCNT overflow.	Addresses 0 are same as above. Bit 6
RSTCSR	RSTS	Reset Control/Status Register (Reset Select) When RSTS = 0, power-on reset is selected. When RSTS = 1, manual reset is selected.	Addresses 0 are same as above. Bit 5
—	—	Reset Control/Status Register (Reserved) These bits cannot be written to; always read as "1".	Addresses 1, 1, 1, 1, 1 are same as above. Bits 4 to 0
PADDR	PA1DDR	Port A Data Direction Register (Port A Data Direction Register 1) When PA1DDR = 0, the PA1 pin is used as an input port. When PA1DDR = 1, the PA1 pin is used as an output port. Note: This applies when address output on this pin is disabled.	H'FFFE39 1 Bit 1
PADDR	PA0DDR	Port A Data Direction Register (Port A Data Direction Register 0) When PA0DDR = 0, the PA0 pin is used as an input port. When PA0DDR = 1, the PA0 pin is used as an output port. Note: This applies when address output on this pin is disabled.	H'FFFE39 1 Bit 0
PADR	—	Port A Data Register Stores output data for the pins used as general-purpose output ports	H'FFFF09 0, 0, 0, 0 Bit 3 to bit 0
PORTA	—	Port A Register If this register is read while PADDR bits are 0, the pin states are read. If this register is read while PADDR bits are 1, the value in PADR is read.	H'FFFFB9 0 Bit 3 to bit 0

5. Flowchart

1. Main routine and interrupt routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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