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Renesas Electronics Corporation

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H8S/2200 Series

D/A Conversion

Introduction

Starts the DMAC by the TPU and performs D/A conversion of data stored in the RAM.

Target Device

H8S/2215

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1. Specifications

1. As shown in figure 1, this sample task starts up the DMACs from ch0 and ch1 of the TPUs to perform D/A conversion of data stored in the RAM.
2. The RAM areas start with H'600000 and end with H'61FFFF.
3. The H8S/2215 runs at 16-MHz internal operating frequency.

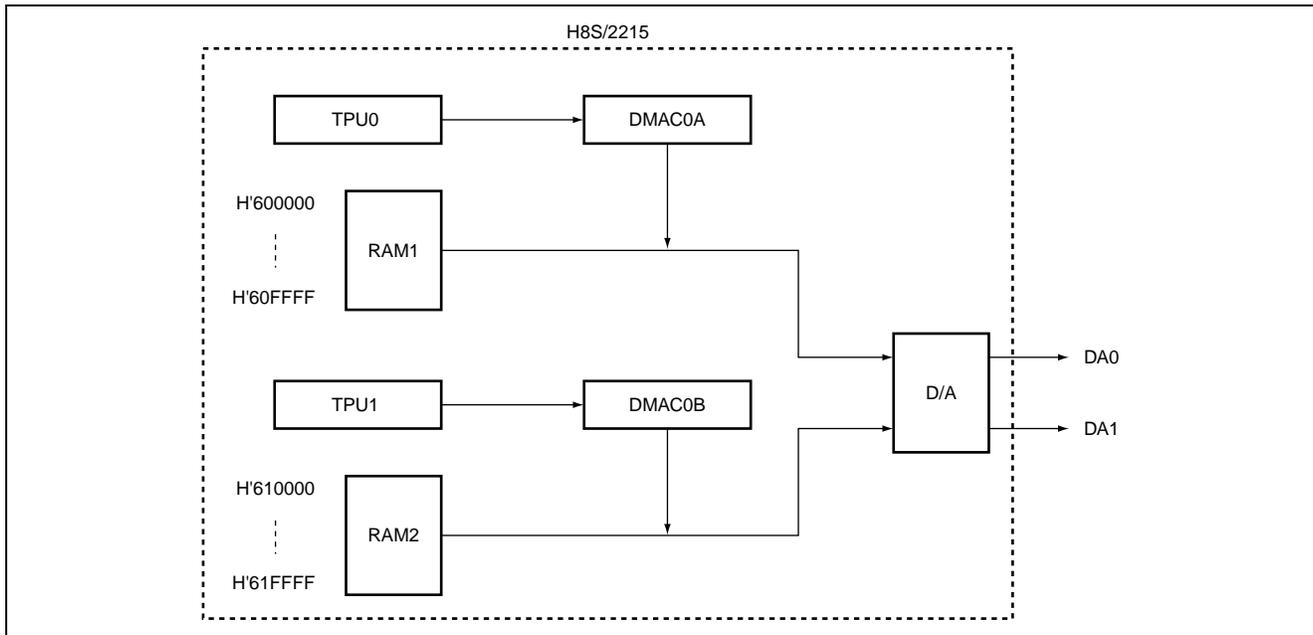


Figure 1 D/A Conversion Block Diagram

2. Description of Functions

- The block diagram of the DMACs, D/A, and TPUs to be used by this sample task is shown in figure 2. This sample task uses the H8S/2215 function as follows to perform D/A conversion:

[DMACs]

Start up by a TPU compare match A and transfers data in the data buffer to D/A DADR.

[TPUs]

Operate ch0 and ch1 synchronously to start up the DMACs.

Clear the timer counter each time a ch1 compare match A occurs.

[D/A]

Starts D/A conversion immediately after convert data is written in DADRs and outputs the conversion results after conversion time passes. An analog conversion voltage range can be set, using AVcc as the reference voltage.

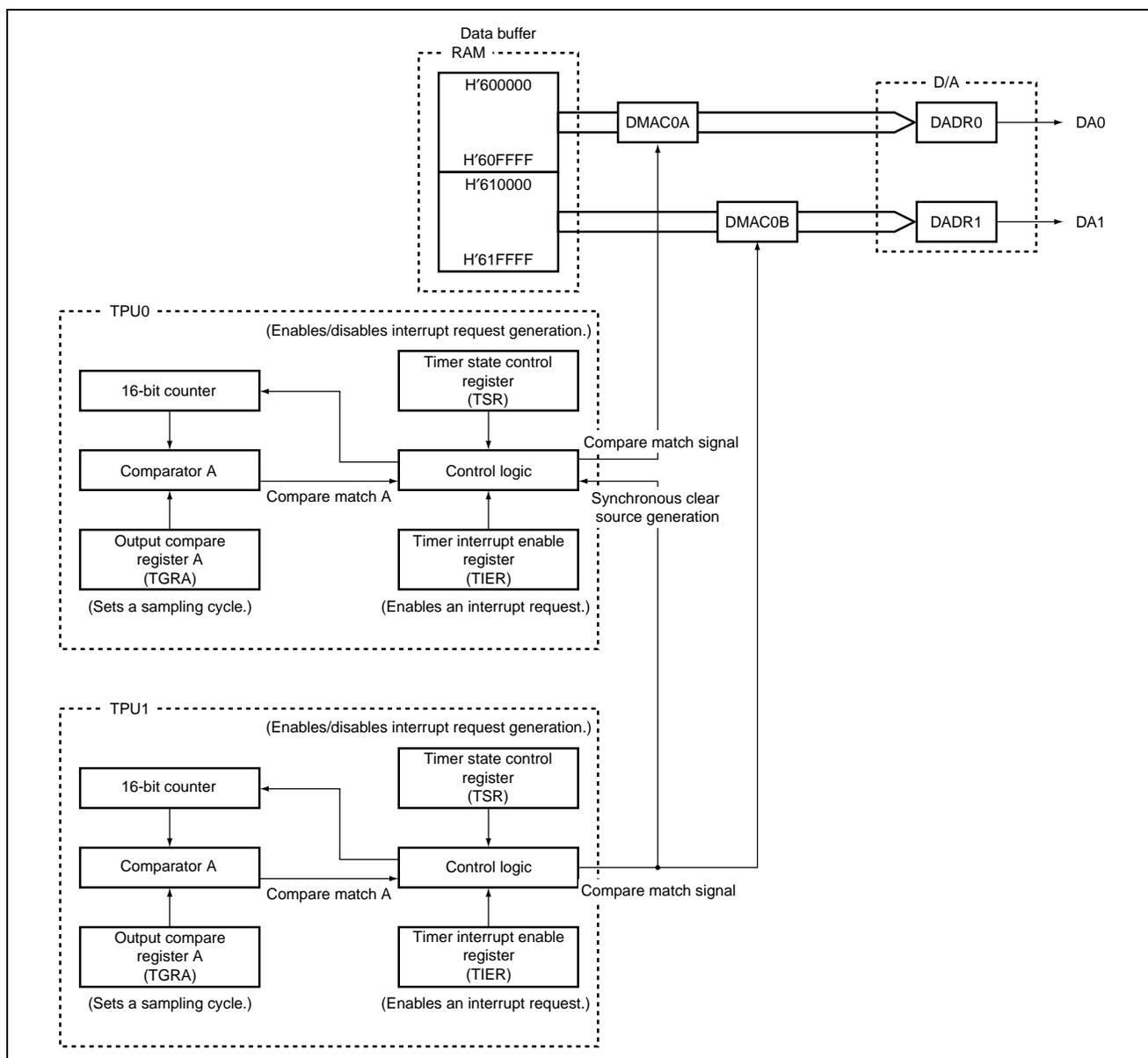


Figure 2 Block Diagram of Analog Output Circuit

2. Function allocation of this sample task is shown in table 1. This sample task allocates the H8S/2215 functions as shown in table 1 to perform D/A conversion.

Table 1 Assignment of Functions

Elements	Description		
TPU	TCNT0	16-bit counter	
	TGRA_0	Output compare register	
	TCR0	Selects the counter clock and counter clear source.	
	TSR0	Indicates the compare match and overflow state.	
	TIER0	Enables/disables an interrupt.	
	TCNT1	16-bit counter	
	TGRA_1	Output compare register	
	TCR1	Selects the counter clock and counter clear source.	
	TSR1	Indicates the compare match and overflow state.	
	TIER1	Enables/disables an interrupt.	
	TSYR	Sets ch0 and ch1 to synchronous operation.	
	DMAC	DMABCR	Controls operation of each channel.
		DMACR0	Sets the transfer mode to the sequential mode.
MAR0A		Sets the start address of data.	
MAR0B		Sets the start address of data.	
IOAR0A		Sets the DADR0 address.	
IOAR0B		Sets the DADR1 address.	
ETCR0A		Sets the transfer count.	
ETCR0B		Sets the transfer count.	
D/A	DADR0	Stores data to be converted (DA0 side).	
	DADR1	Stores data to be converted (DA1 side)	
	DACR	Controls operation of the D/A converter.	
	AVcc	Voltage and reference voltage of the analog part	
	AVss	Ground and reference voltage of the analog module	
	DA0	Analog output	
	DA1	Analog output	

3. Principles of Operation

The principles of operations used are shown in figure 3. This sample task performs hardware and software processing of the H8S/2215 as shown in figure 3 to perform D/A conversion.

1. Analog Output

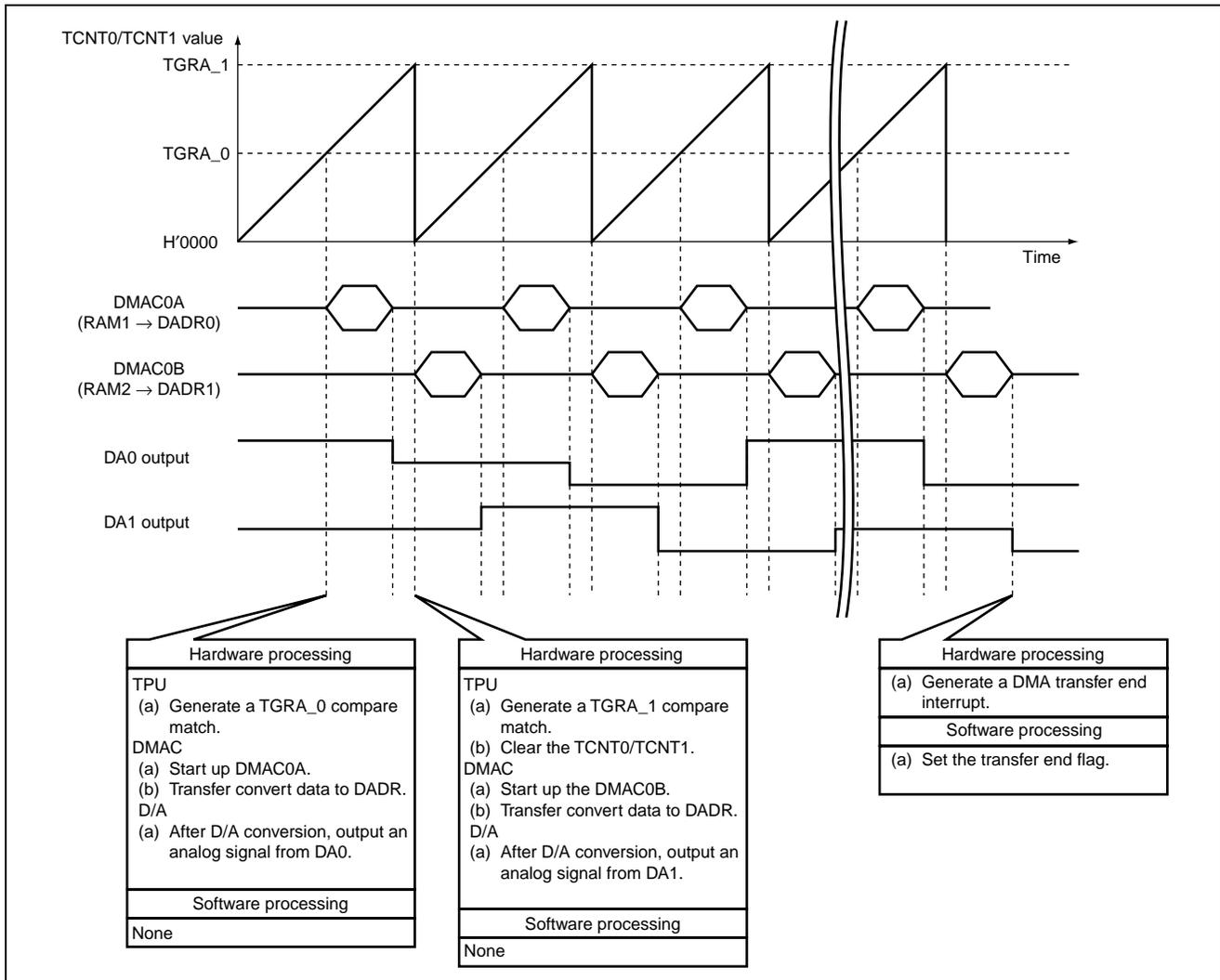


Figure 3 Principles of Operations Used for Analog Output

4. Description of Software

1. Description of Modules

Module Name	Label Name	Function
Main routine	dacvtmn	Performs initial setting of the TPU, DMAC, and D/A, and sets the RAM to be used.
D/A conversion end	datrend	Sets the D/A conversion end flag.

2. Description of Argument

Label Name	Function	Data Length	Used in	I/O
da_end	Indicates end of transfer of data in H'600000 to H'61FFFF. 1: Data transfer ended 0: Data transfer in progress	unsigned char	Main routine D/A conversion end	Input Output

3. Description of Internal Registers Used

Implemented Function	Register Name	Function	
TPU	TGRA_0	Sets the sampling cycle of D/A conversion.	
	TIER0	Enables a TGIA interrupt.	
	TCR0	Sets the TPU0 as follows: <ul style="list-style-type: none"> • Synchronous clear • Count by internal clock ϕ 	
	TIOR0	Sets TGRA_0 as the output compare register and disables pin output.	
	TGRA_1	Sets the sampling cycle of D/A conversion.	
	TIER1	Enables a TGIA interrupt.	
	TCR1	Sets the TPU0 as follows: <ul style="list-style-type: none"> • Counter clear by a TGRA_1 compare match • Count by internal clock ϕ 	
	TIOR1	Sets TGRA_1 as the output compare register and disables pin output.	
	TSTR	Enables count operation of the TCNT0 and TCNT1.	
	TSYR	Sets channels 0 and 1 to synchronous operation.	
	DMAC	DMABCR	Controls operation of each channel.
		DMACR0A	Sets the DMAC0A as follows: <ul style="list-style-type: none"> • Byte size transfer • Sequential mode • Enabling clear of the internal interrupt source during DMA transfer • Enabling data transfer
		DMACR0B	Sets the DMAC0B as follows: <ul style="list-style-type: none"> • Byte size transfer • Sequential mode • Enabling clear of the internal interrupt source during DMA transfer • Enabling data transfer and a transfer end interrupt
MAR0A		Sets the transfer source address (start address of RAM1)	
MAR0B		Sets the transfer source address (start address of RAM2)	
IOAR0A		Sets the transfer destination address (DADR0).	
IOAR0B		Sets the transfer destination address (DADR1).	
ETCR0A		Sets the transfer count (H'0000).	
ETCR0B		Sets the transfer count (H'0000).	
D/A		DACR0	Sets DACR as follows: <ul style="list-style-type: none"> • Enables D/A conversion of channel 0 and analog output from DA0.
		DADR0	Stores data to be converted.
		DADR1	Stores data to be converted.
MSTPCR			Cancels the module stop mode.

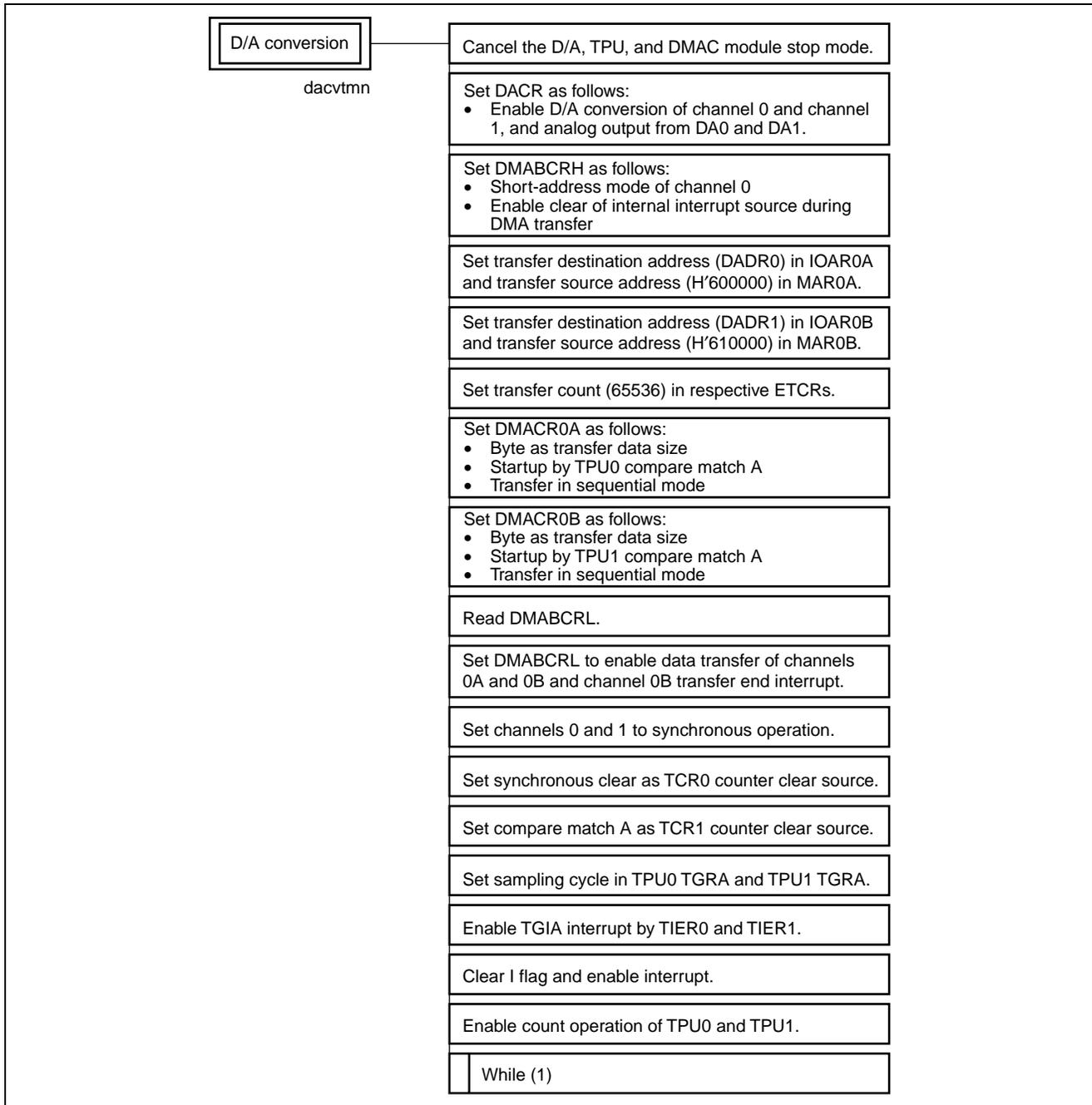
4. RAM Usage

Table below describes RAM usage in this sample task.

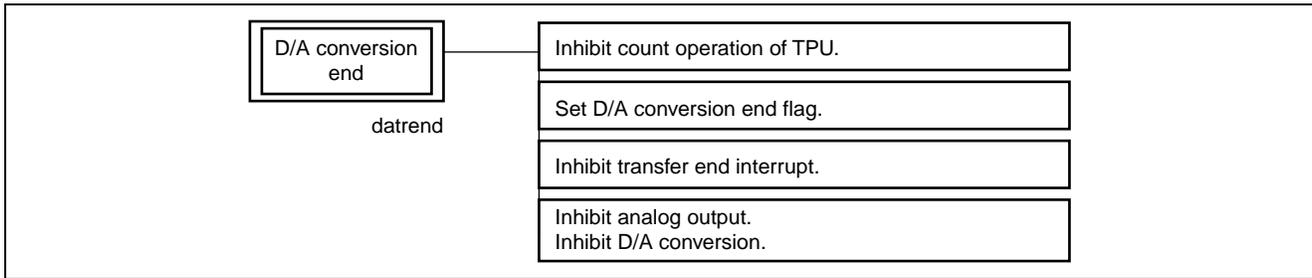
Label Name	Function	Data Length	Data Capacity
da_data1, 2	Stores D/A conversion data.	unsigned char	128 kbytes

5. PAD

1. Main Routine



2. D/A Conversion End



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16.04	—	First edition issued

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