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Renesas Electronics Corporation

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H8S/2200 Series

Handling Multiple Internally Generated Interrupts

Introduction

Using the watchdog timer in interval timer mode, a timer overflow interrupt is generated (primary interrupt), which triggers asynchronous serial transmission. On completion of the transmission, a transmission-end interrupt is generated as the secondary interrupt, and communication end processing is performed.

Target Device

H8S/2215

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1. Specifications

1. As shown in figure 1, an overflow interrupt (primary interrupt) is generated by the watchdog timer (WDT) which operates in interval timer mode.
2. Operation shifts to the SCI transmission routine (wdti) when the primary interrupt is generated, and transmission via the serial communication interface (SCI) is started.
3. When the SCI transmission ends, a transmission-end interrupt TEI2 (secondary interrupt) is generated, upon which the end_flg is set and operation ends.

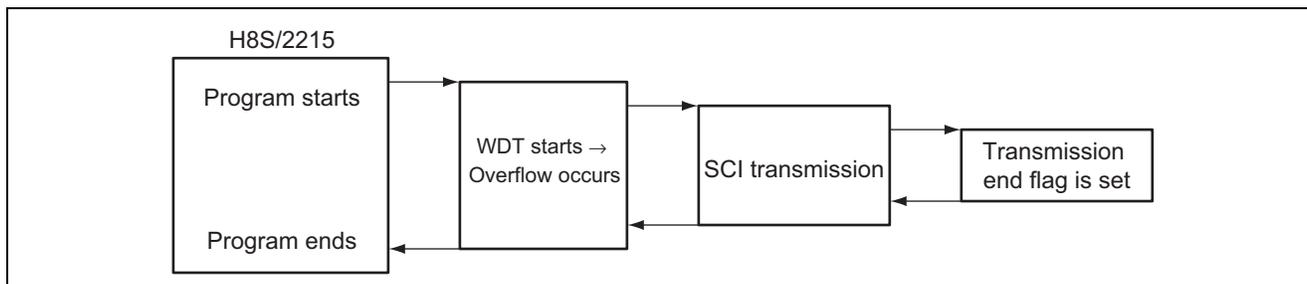


Figure 1 Example of Handling Multiple Interrupts

2. Description of Functions

1. Figure 2 shows a block diagram of the interrupt controller, and the following is the description of the interrupt controller registers used in the sample task:
 - The system control register (SYSCR) selects the interrupt control mode, sets the NMI detection edge, enables/disables the MRES pin input and enables/disables the on-chip RAM.
 - The interrupt priority register x (IPRx; x represents A to G, I to K, and M) sets the priority levels (7 to 0) of interrupts other than NMI. For details on IPR and corresponding interrupt sources, refer to the hardware manual. By setting a value from H'0 to H'7 to bits 6 to 4 and 2 to 0, the priority of the corresponding interrupt is decided.
 - The IRQ enable register (IER) enables IRQ7 to IRQ0 interrupt requests.
 - The IRQ sense control registers H and L (ISCRH and ISCRL) select the conditions for generation of interrupt requests by the IRQ7 to IRQ0 pins.
 - The IRQ status register (ISR) consists of IRQ7 to IRQ0 interrupt request flags.

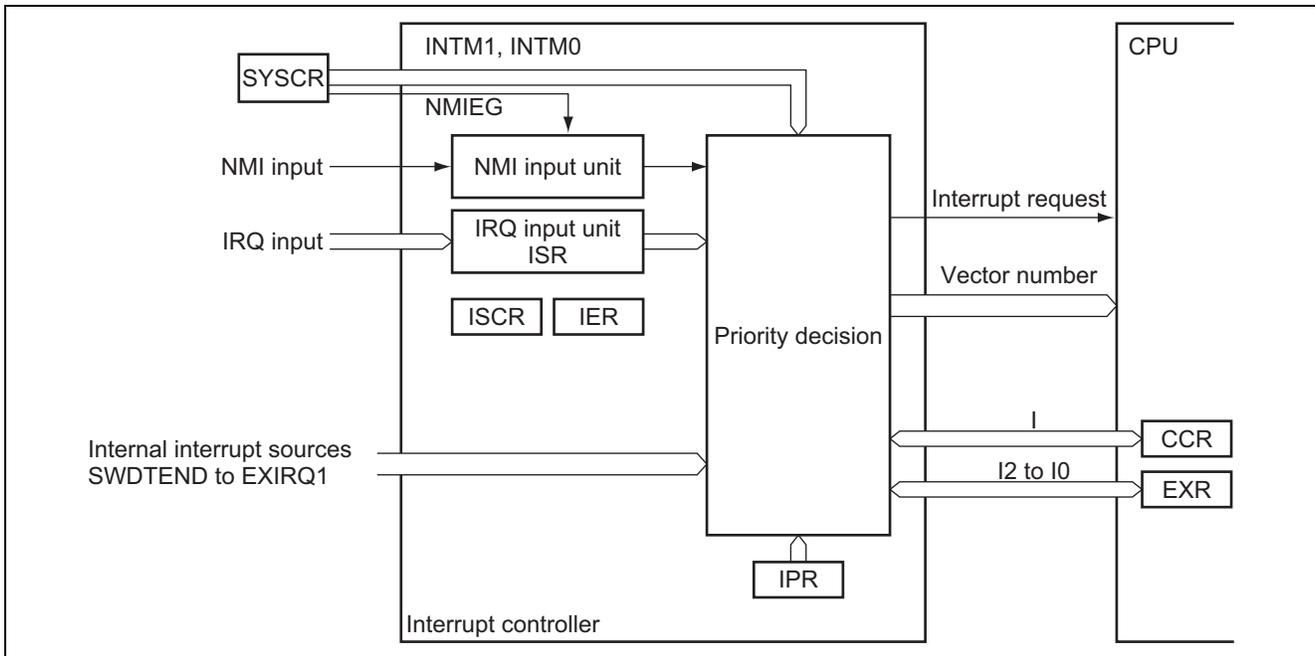


Figure 2 Block Diagram of Interrupt Controller

2. Table 1 shows the assignment of interrupt-related functions used in this sample task.

Table 1 Assignment of Functions

Elements	Description
SYSCR	Sets interrupt mode 2 and enables the on-chip RAM, etc.
IPRx	Sets IPRK (H'04) priority to be higher than that of IPRD (H'30).
IER	Disables IRQ7 to IRQ0 interrupts.
ISCRH and ISCR L	Disables input of interrupt signals on the $\overline{\text{IRQ7}}$ to $\overline{\text{IRQ0}}$ pins.
ISR	When an interrupt is generated by an externally input signal, the corresponding flag in this register is set.

3. Principles of Operation

Figure 3 shows the principle of operation of this sample task. Multiple internally generated interrupts are handled through the hardware and software processing shown in the figure.

1. An overflow interrupt (primary interrupt) is generated by the watchdog timer in interval timer mode.
2. Operation shifts to the SCI transmission routine (wdti) when the primary interrupt is generated, and transmission via the serial communication interface (SCI) is started.
3. When the SCI transmission ends, the transmission-end interrupt TEI2 (secondary interrupt) is generated, upon which the `end_flg` is set and operation ends.

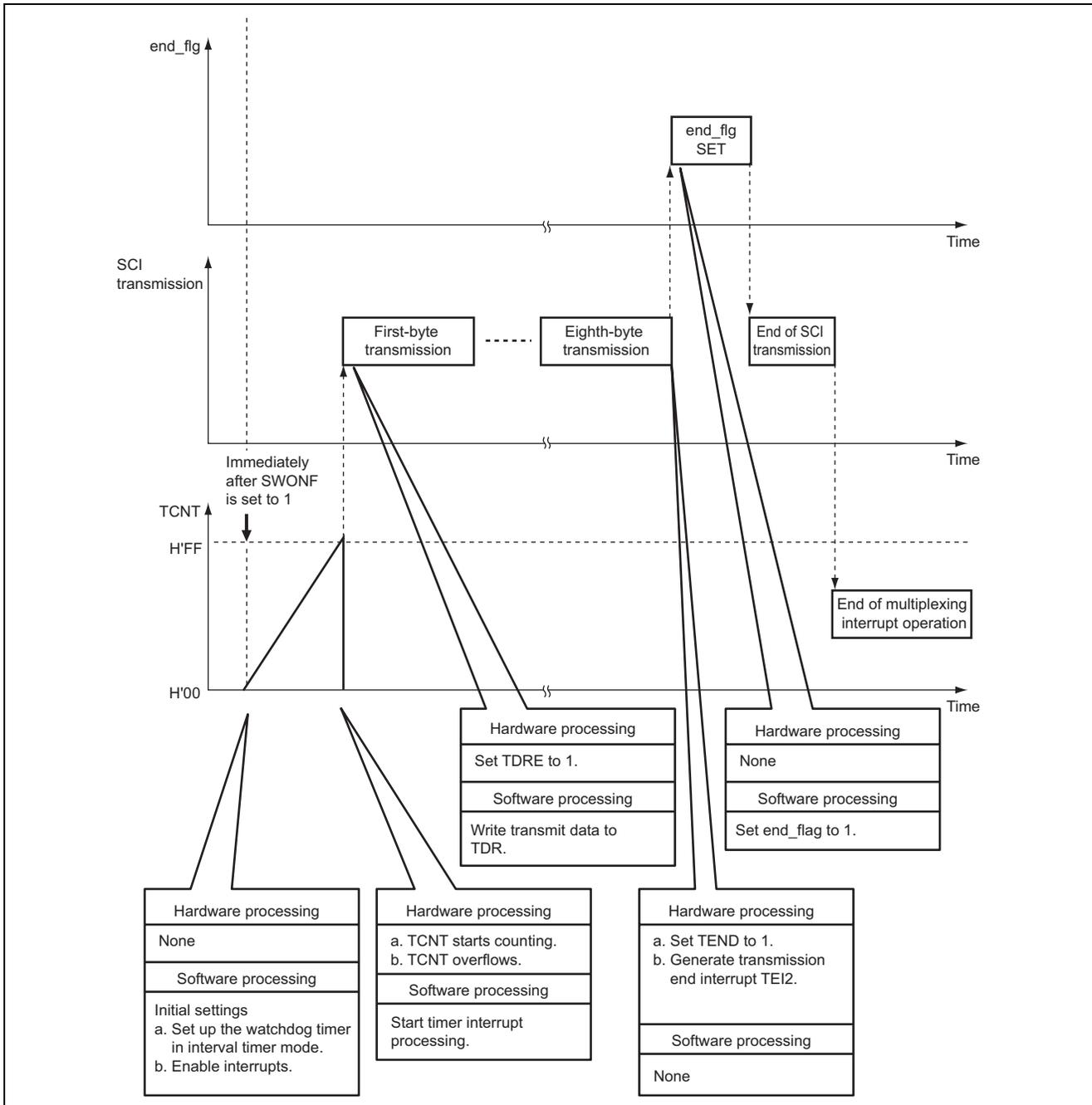


Figure 3.1 Setting `end_flg` by Multiple-Interrupt Handling

4. Description of Software

4.1 Modules

Table 2 describes the modules used in this sample task.

Table 2 Description of Modules

Module	Label	Function
Main routine	main	Sets up a watchdog timer counter. When the counter overflows, shifts to the SCI transmission routine (wdti).
SCI transmission routine	wdti	Starts asynchronous SCI transmission and shifts to the tei2 routine when 8 bytes of data have been transmitted.
end_flg routine	tei2	Sets the end_flg flag.

4.2 Arguments

This sample program does not use arguments.

4.3 Internal Registers

The interrupt-related internal registers used in this sample task are described in table 3.

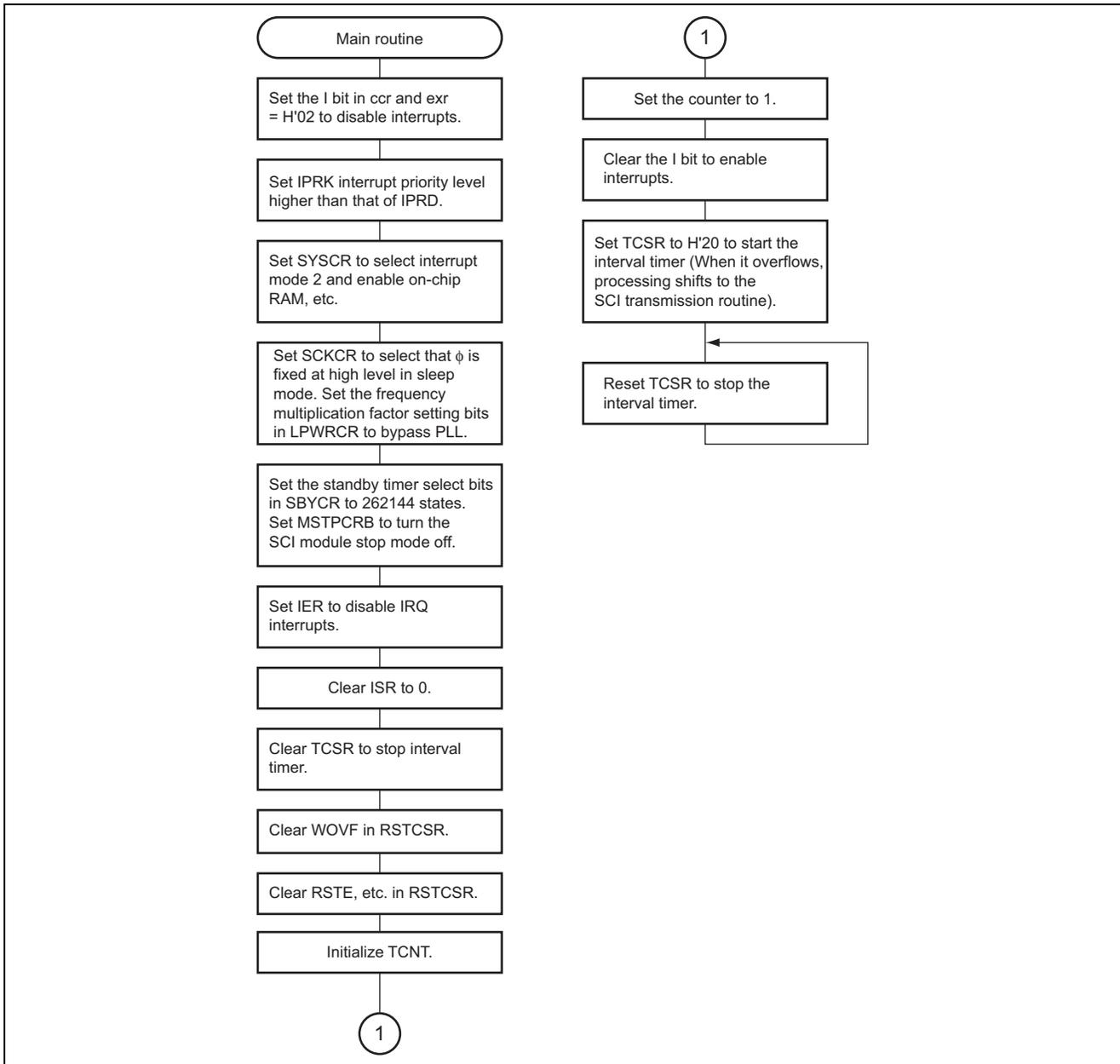
Table 3 Description of Internal Registers

Register	Function	Address	Setting
SYSCR	INTM1	System Control Register	H'FFFDE5 1, 0
	INTM0	Selects interrupt control mode for the interrupt controller.	Bit 5
		When INTM1 and INTM0 = 00, interrupt control mode 0 is selected. When INTM1 and INTM0 = 10, interrupt control mode 2 is selected. Note: Setting of 01 or 11 is prohibited.	Bit 4
NMIEQ	System Control Register (NMI Edge Select) When NMIEG = 0, an interrupt request is generated at the falling edge of NMI input. When NMIEG = 1, an interrupt request is generated at the rising edge of NMI input.	H'FFFDE5 Bit 3	0
MRESE	System Control Register (Manual Reset Select) When MRESE = 0, manual reset is disabled. When MRESE = 1, manual reset is enabled.	H'FFFDE5 Bit 2	0
RAME	System Control Register (RAM Enable) When RAME = 0, the on-chip RAM is disabled. When RAME = 1, the on-chip RAM is enabled.	H'FFFDE5 Bit 0	1
IER	IEQ Enable Register When IRQnE = 0, interrupt requests are disabled. When IRQnE = 1, interrupt requests are enabled. (n: 7 to 0)	H'FFFE14	H'00

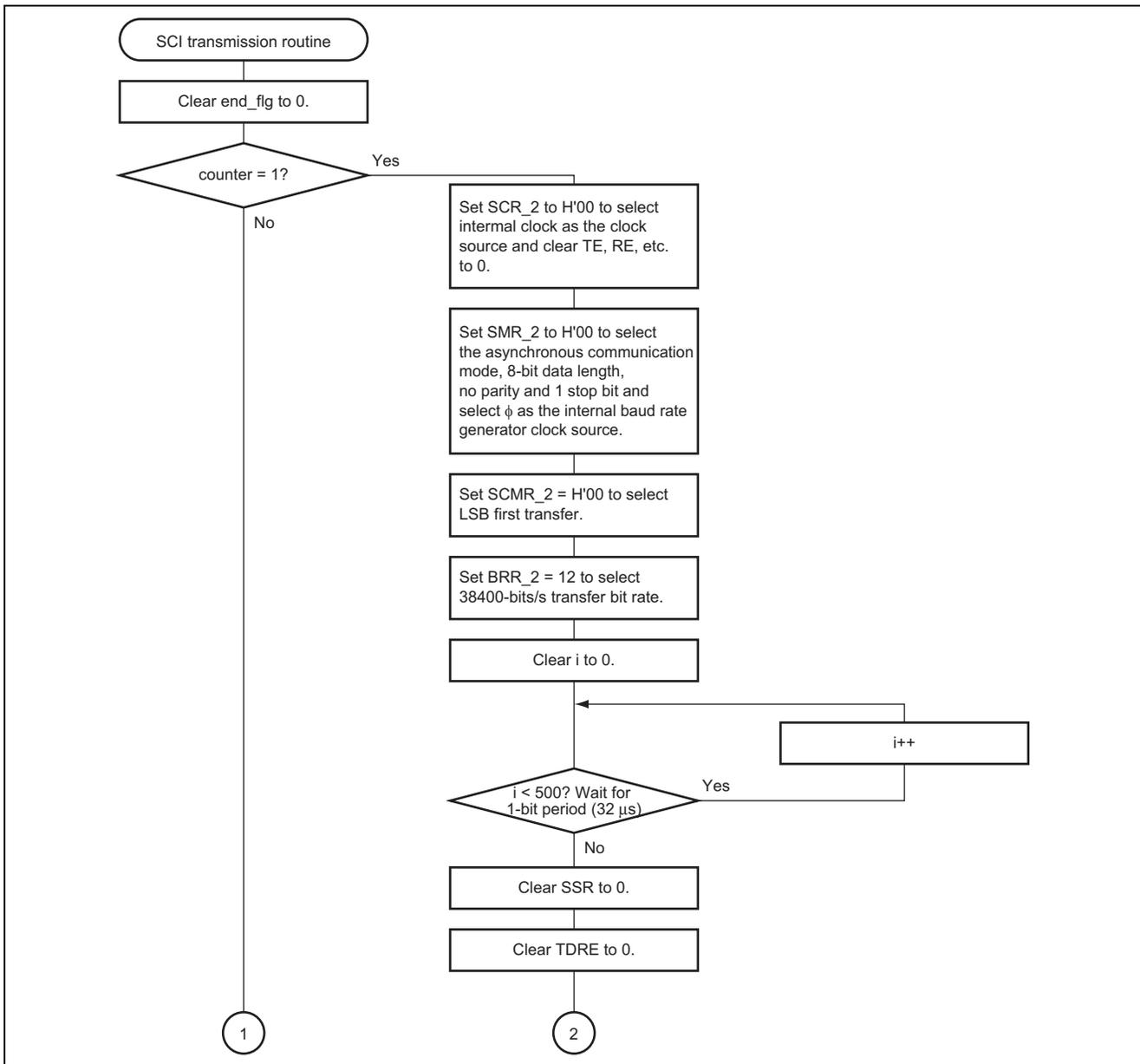
Register	Function	Address	Setting
ISCRH, ISCRL	IEQ Sense Control Registers H and L When bits IRQnSCB and IRQnSCA = 00, interrupt requests are generated on the low level of the IRQn input. (n: 7 to 0) ISCRH: IRQ7SCB, IRQ7SCA, ... IRQ4SCB and IRQ4SCA ISCRL: IRQ3SCB, IRQ3SCA, ... IRQ0SCB and IRQ0SCA	H'FFFE12 H'FFFE13	H'00 H'00
IPRD	Interrupt Priority Register D Bits IPR6 to IPR4 = 111 to 000: Sets priority of the WDT interrupt source. 111 sets the highest priority level (7) and 000 sets the lowest (0).	H'FFFE13 Bits 6 to 4	0, 1, 1
IPRK	Interrupt Priority Register K Bits IPR6 to IPR4 = 111 to 000: Sets priority of the TE2 interrupt source. 111 sets the highest priority level (7) and 000 sets the lowest (0).	H'FFFE1A Bits 2 to 0	1, 0, 0
ISR	IRQ Status Register When IRQnF = 0, the interrupt source has not been detected. When IRQnF = 1, the interrupt source selected with ISCR has been detected. (n: 7 to 0)	H'FFFE15 Bits 7 to 0	0 for each bit

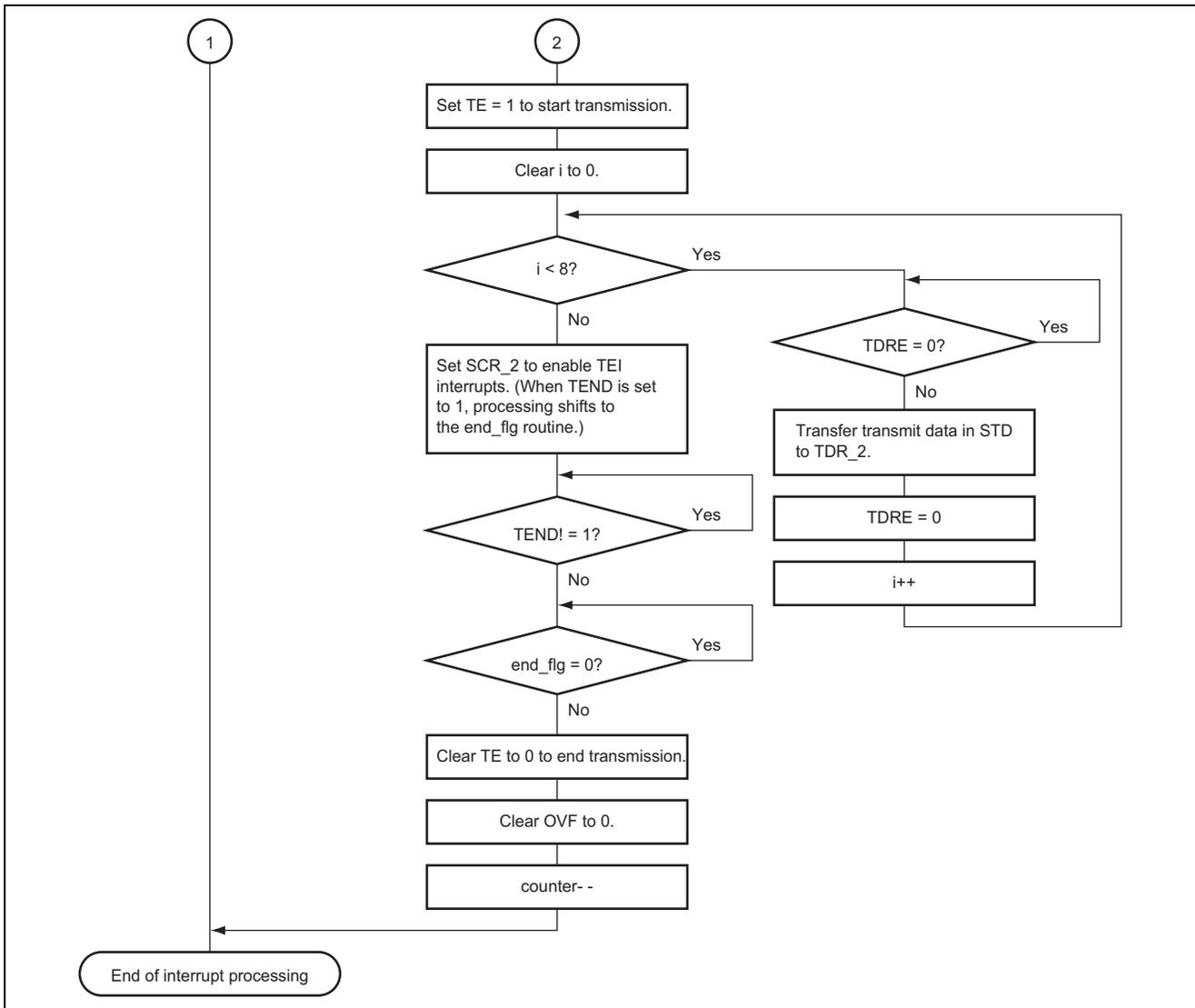
5. Flowchart

1. Main routine

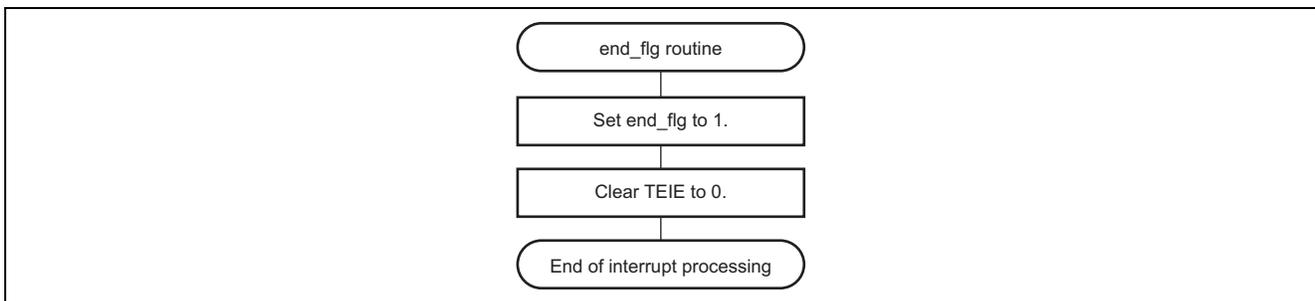


2. SCI transmission routine





3. end_flg routine



Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.16, 2004	—	First edition issued

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