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H8SX Family

Synchronous DRAM Operation after Cancellation of Deep Software Standby Mode

Introduction

This application note describes the method for accessing synchronous DRAM (SDRAM) after cancellation of deep software standby mode.

This method makes it possible to avoid problems related to the period of Bϕ and SDRAMϕ output instability (maximum of 1 cycle) that occurs immediately following cancellation of deep software standby mode.

Target Devices

H8SX/1668R Group

Preface

This program can be used with other H8SX Family MCUs that have the same internal I/O registers as the devices on which operation has been confirmed.

Check the latest version of the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Contents

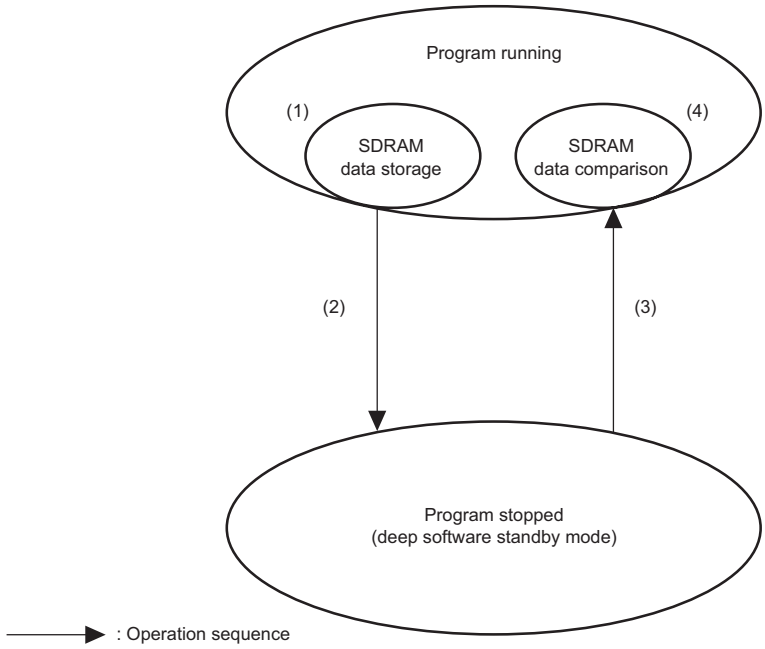
1. Specifications

First, a transition is made to deep software standby mode, then deep software standby mode is canceled by means of the IRQ0 interrupt. Next, the SDRAM data before the transition to and after cancellation of deep software standby mode are compared to determine if they match. Also, the comparison result is indicated by means of I/O ports.

Figure 1 shows an overview of the operations described in this application note.

The detailed specifications for the operations described in this application note are as follows:

- After the program is run, data is stored in the entire SDRAM area.
- Area 2 (addresses H'400000 to H'BFFFFF) is used as the SDRAM area.
- The data stored in the SDRAM area consists of H'00, H'01, …, H'0F, H'10, …, H'FF, H'00, ….
- After data is stored in the entire SDRAM area, a transition is made to deep software standby mode.
- An IRQ0 interrupt request is generated manually to cancel deep software standby mode.
- After cancellation of deep software standby mode, the data in the SDRAM is compared with the data stored before the transition to deep software standby mode to determine if they match.
- The result of the comparison of the SDRAM data before the transition to and after cancellation of deep software standby mode is output to a port. (P20 outputs a low-level signal if the data matches, and P21 outputs a low-level signal if the data does not match.)



[Legend]
(1) After program launch, data is stored in the SDRAM.
(2) SSBY and DPSBY are set to 1 and the SLEEP instruction is executed to transition to deep software standby mode.*
(3) Deep software standby mode is canceled by IRQ0.
(4) The SDRAM data before the transition to and after cancellation of deep software standby mode are compared.

Note: * For information on SSBY, see 5.3.3, init_reg Function, (4) Description of internal I/O registers used, Standby Control Register (SBYCR).
For information on DPSBY, see 5.3.3, init_reg Function, (4) Description of internal I/O registers used, Deep Standby Control Register (DPSBYCR).

Figure 1 Operation Overview

2. Applicable Conditions

Table 1 Applicable Conditions

Item	Description
Operating frequency	Input clock: 12.5 MHz System clock(Iϕ): 50 MHz (12.5 MHz multiplied by 4) Peripheral module clock (Pϕ): 25 MHz (12.5 MHz multiplied by 2) External bus clock (Bϕ): 50 MHz (12.5 MHz multiplied by 4)
Operating voltage	3.3V
Operating mode	Mode 6 (MD2 = 1, MD1 = 1, MD0 = 0, MD_CLK = 0)
Integrated development environment	High-performance Embedded Workshop (HEW) Ver.4.04.01
C/C++ compiler	Renesas Technology H8S/300, H8/300 C/C++ Compiler (V6.02.00)
Compile options	-cpu = H8SXA:24MD, -optimize = 1
Optimizing linkage editor	Renesas Technology Optimizing Linkage Editor (V9.03.00)
Linker options	start = PResetPRG,PIntPRG/0400, P,C$DSEC,C$BSEC,D/0800, B,R/0FF2000, S/0FFBE00

Table 2 SDRAM Specifications

Item	Description
Product name	K4S641632K-UC75 (Samsung Electronics)
Configuration	1M × 16 bit × 4 banks
Capacity	64 Mbits
CAS latency	2/3 (programmable)
Refresh interval	4,096 refresh cycles each 64 ms
Low address	A11 - A0
Column address	A7 - A0
Number of banks	4-bank operation controlled by BA0 and BA1

Table 3 SDRAM Mode Settings

Item	Description
Operation code (OPCODE)	Burst read/single write
CAS latency (LMODE)	2
Burst type (BT)	Sequential
Burst length (BL)	1
SDRAM access address	H'400440

3. Functions Used

3.1 Entry to Deep Software Standby Mode

If a SLEEP instruction is executed when the SSBY bit in SBYCR has been set to 1, a transition to software standby mode is made. In this state, if the CPSBY bit in DPSBYCR is set to 1, a transition to deep software standby mode is made.

3.2 Canceling Deep Software Standby Mode

Deep software standby mode is canceled by signal input to an external interrupt pin (NMI or $\overline{\text{IRQ0}}$-A to $\overline{\text{IRQ3}}$-A), by an internal interrupt signal (32K timer, USB suspend/resume), or by signal input to the $\overline{\text{RES}}$ pin or $\overline{\text{STBY}}$ pin.

3.3 Bϕ/SDRAMϕ Operation after Exit from Deep Software Standby Mode

When the IOKEEP bit is 0, BϕSDRAMϕ output is undefined for a maximum of one cycle immediately after exit from deep software standby mode. At this time, the output state cannot be guaranteed. Even when the IOKEEP bit is set to 1, Bϕ/SDRAMϕ output is undefined for a maximum of one cycle immediately after the IOKEEP bit is cleared to 0 after deep software standby mode was canceled, and the output state cannot be guaranteed.

However, clock can be normally output by canceling deep software standby mode with the IOKEEP bit set to 1 and then controlling the Bϕ/SDRAMϕ output with the IOKEEP and PSTOP1 bits. Following procedure takes Bϕ for example. (See figure 2)

1. Change the value of the PSTOP1 bit from 0 to 1 to fix the Bϕ output at the high level (given that the Bϕ output was already fixed high).
2. Clear the IOKEEP bit to 0 to end retention of the Bϕ state.
3. Clear the PSTOP1 bit to 0 to enable Bϕ output.

In case of the SDRAMϕ clock can be normally output by controlling the PSTOPϕ bit instead of the PSTOP1 bit in the same way as the procedure above mentioned.

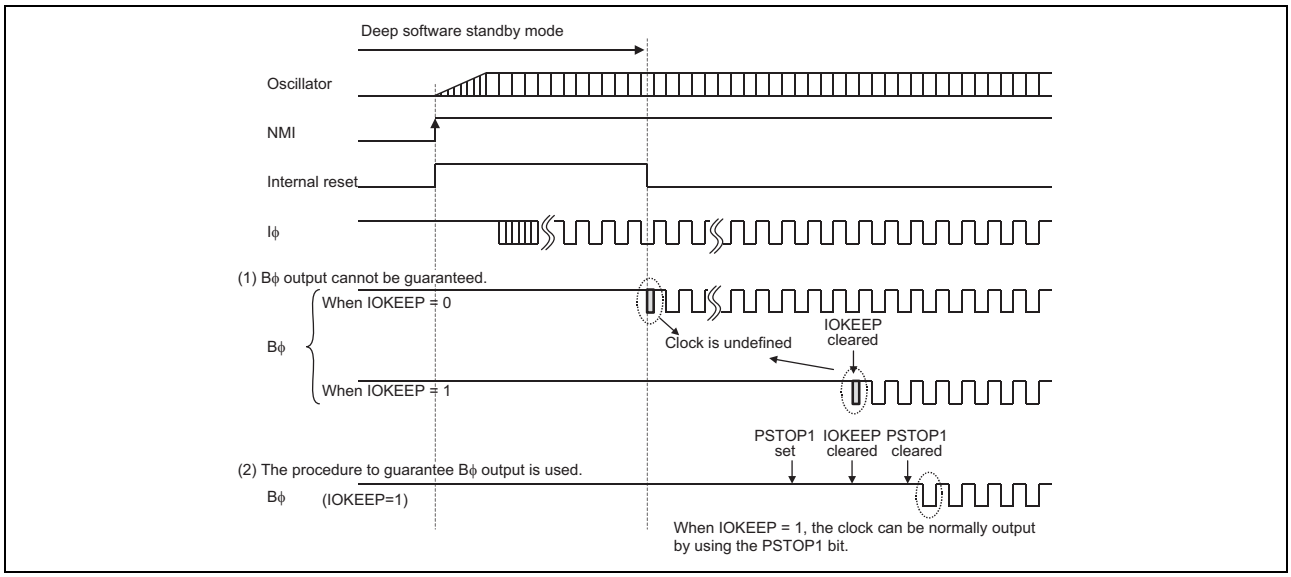


Figure 2 Bϕ Operation after Exit from Deep Software Standby Mode

4. Operation

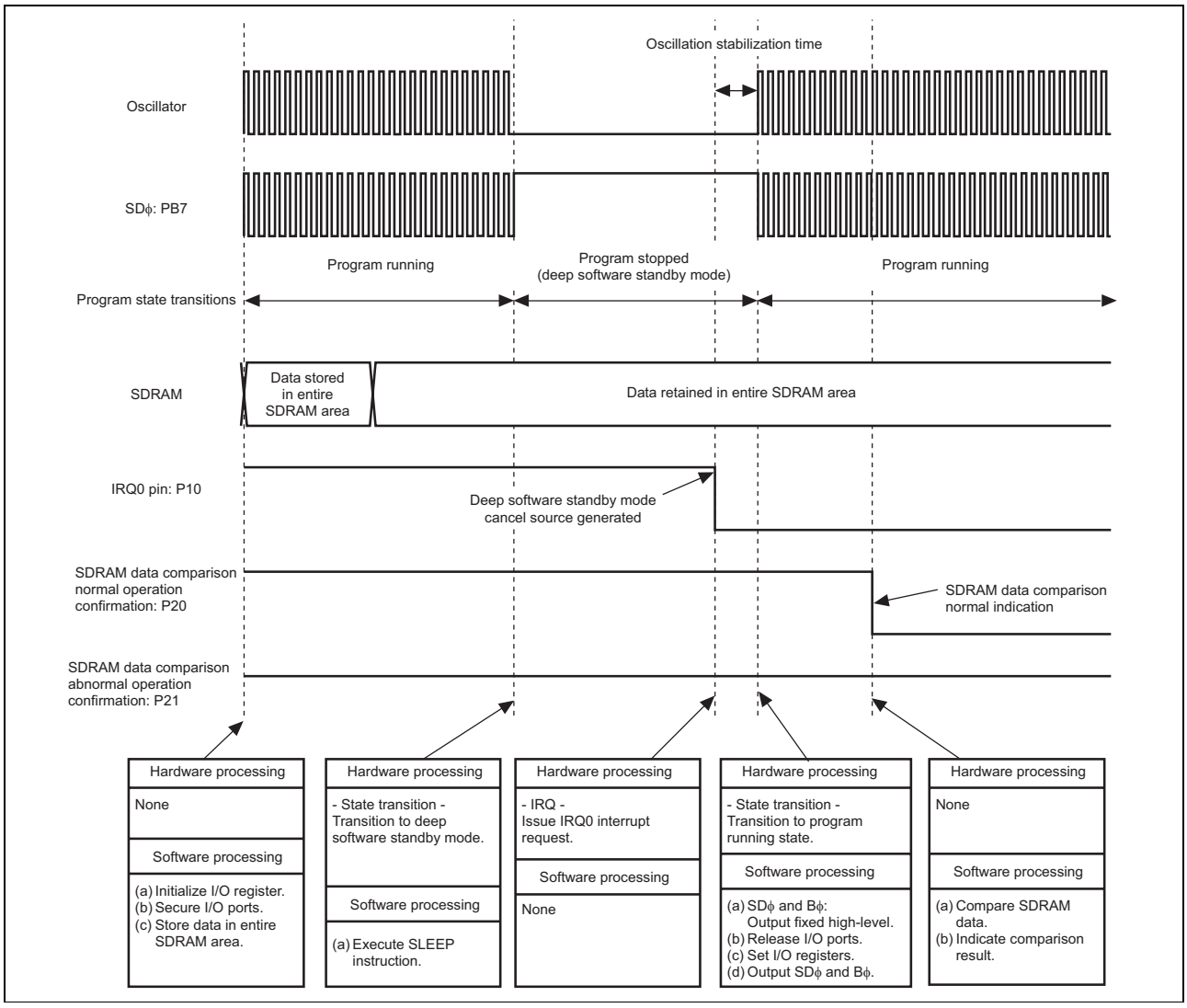


Figure 3 Operation

5. Software Description

5.1 Symbolic Constants

Table 4 List of Symbolic Constants

Constant Name	Setting Value	Description	Used by Functions
SDRAM_MODE_ADDRESS	H'400440	SDRAM mode setting address	init_reg
SDRAM_AREA_START_ADDRESS	H'400000	SDRAM area start address	init_ram, cmp_data
SDRAM_AREA_END_ADDRESS	H'C00000	SDRAM area end address + 1	init_ram, cmp_data

5.2 List of Functions

Table 5 List of Functions

Function Name	Description
PowerON_Reset	• Initial settings function Initializes status pointer (SP), sets interrupt mask bits, sets uninitialized/initialized data, calls main function.
main	• Main function Compares flag; calls init_reg function, init_ram function, init_exit_dps function, and cmp_data function; executes SLEEP instruction.
init_reg	• I/O register initialization function Initializes registers.
init_ram	• RAM initialization function Stores data in SDRAM area.
init_exit_dps	• I/O register initialization after cancellation of deep software standby mode function Initializes registers after cancellation of deep software standby mode.
cmp_data	• Data compare function Compares SDRAM data before the transition to and after cancellation of deep software standby mode.

5.3 Functions

5.3.1 PowerON_Reset Function

(1) Functional Overview

The PowerON_Reset function initializes the status pointer (SP) and uses embedded functions and standard library functions to set interrupt mask bits and set uninitialized/initialized data. Then it calls the main function.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

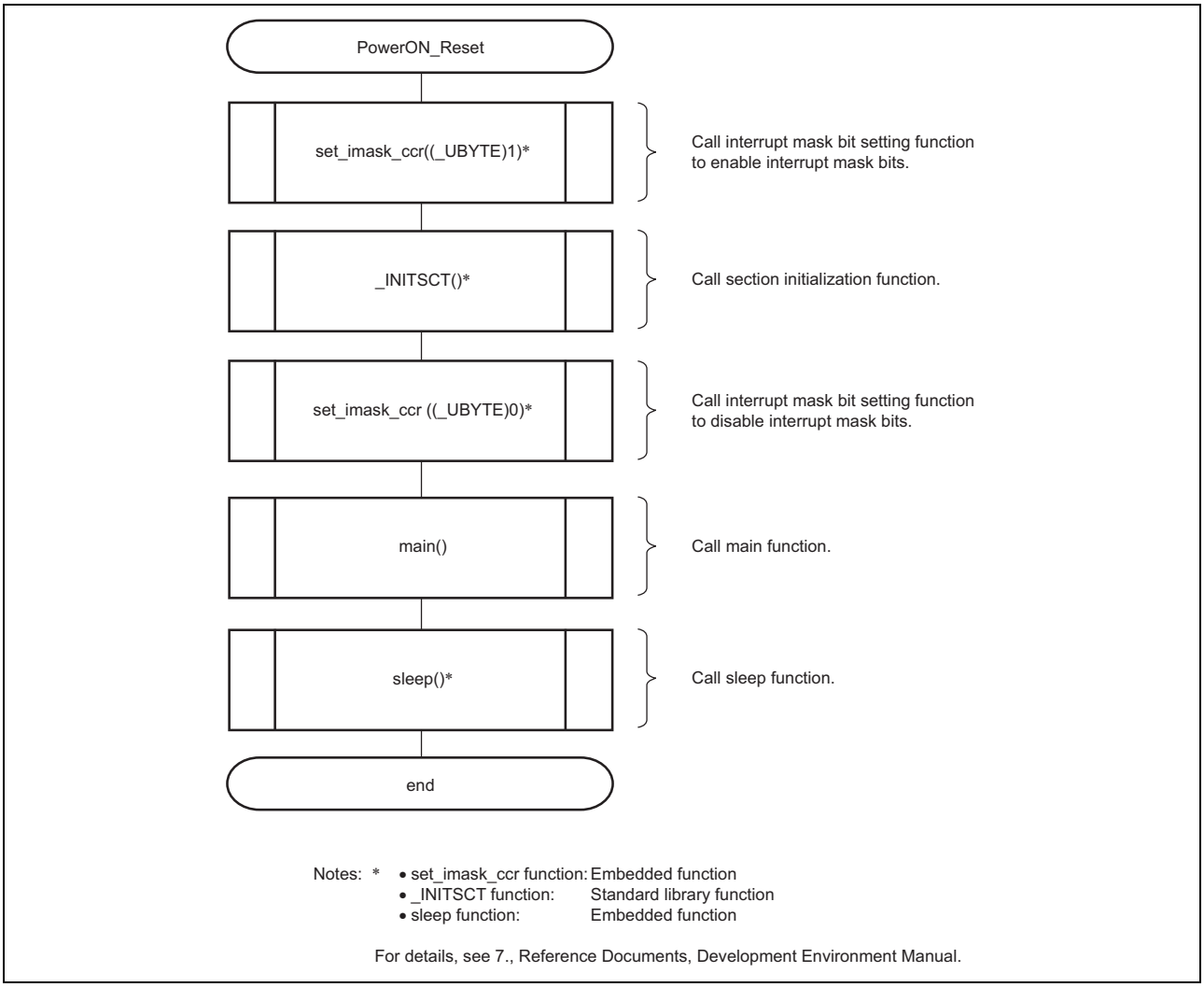


Figure 4 Flowchart (PowerON_Reset)

5.3.2 main Function

(1) Functional Overview

The main function initializes the registers and RAM, then transitions to deep software standby mode. After cancellation of deep software standby mode, it compares the SDRAM data before the transition to and after cancellation of deep software standby mode.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Reset Status Register (RSTSR) Number of bits: 8 Address: H'FFFE75

Bit	Bit Name	Set Value	R/W	Module
7	DPSRSTF	0	R/(W)	Deep Software Standby Reset Flag Indicates that deep software standby mode has been canceled by an interrupt source specified in DPSIER or DPSIEGR and an internal reset is generated. [Clearing condition] Writing a 0 to this bit after reading it as 1.

(5) Flowchart

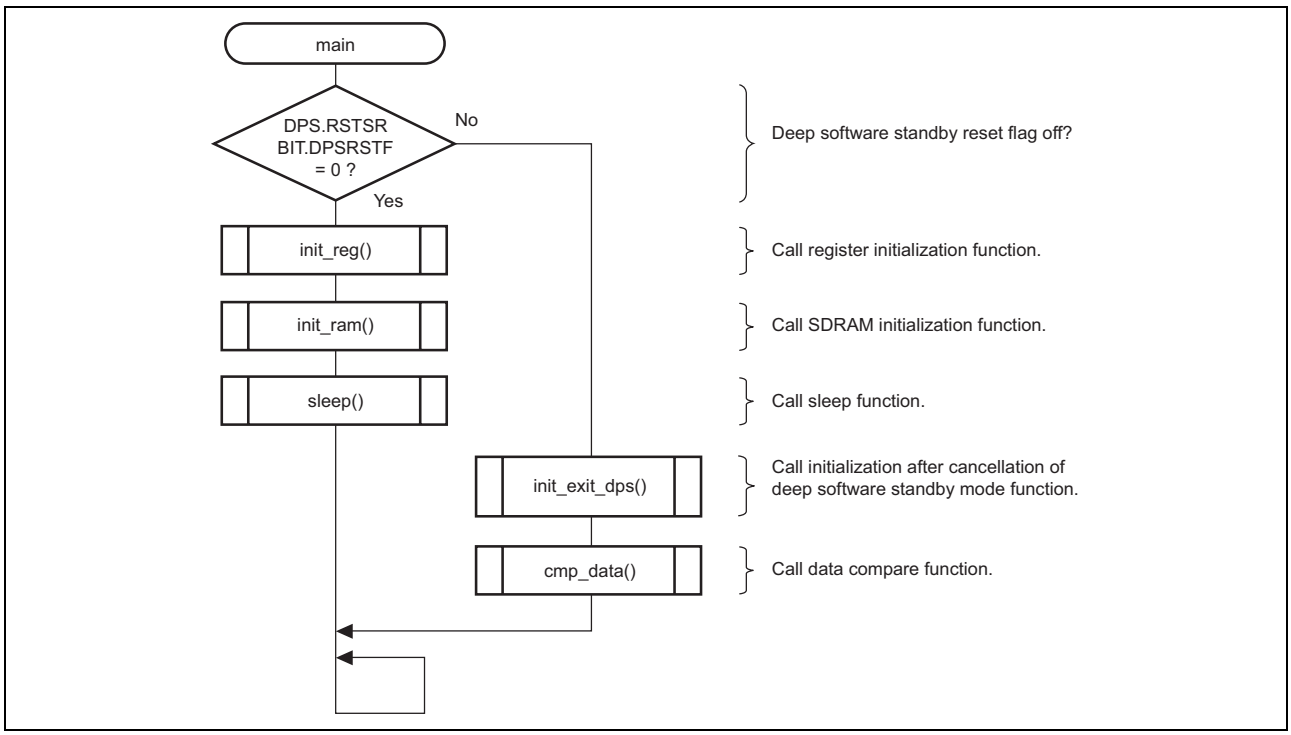


Figure 5 Flowchart (main)

5.3.3 init_reg Function

(1) Functional Overview

The init_reg function initializes various registers.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- System Clock Control Register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Set Value	R/W	Module
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to the
8	ICK0	0	R/W	CPU, DMAC, and DTC. 000: × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock.
4	PCK0	1	R/W	001: × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock.
0	BCK0	0	R/W	000: × 4

- Bus Width Control Register (ABWCR) Number of bits: 16 Address: H'FFFD84

Bit	Bit Name	Set Value	R/W	Module
10	ABWH2	0	R/W	Area 7 to 0 Bus Width Control These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space. ABWH2 ABWL2 0 1: Area 2 is designated as 16-bit access space
2	ABWL2	1	R/W	

- Access State Control Register (ASTCR) Number of bits: 16 Address: H'FFFD86

Bit	Bit Name	Set Value	R/W	Module
10	AST2	1	R/W	Area 7 to 0 Access State Control These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space. Wait cycle insertion is enabled or disabled at the same time. 1: Area 2 is designated as 3-state access space Wait cycle insertion in area 2 access is enabled

- Wait Control Register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Bit	Bit Name	Set Value	R/W	Module
10	W22	0	R/W	Area 2 Wait Control 2 to 0
9	W21	0	R/W	Setting of CAS latency (W22 is ignored.):
8	W20	1	R/W	01: SDRAM with a CAS latency of 2 is connected.

- Idle Control Register (IDLCR) Number of bits: 16 Address: H'FFFD90

Bit	Bit Name	Set Value	R/W	Module
14	IDLS2	0	R/W	Idle Cycle Insertion 2 Inserts an idle cycle between the bus cycles when the external write cycle is followed by external read cycle. 0: No idle cycle is inserted
12	IDLS0	0	R/W	Idle Cycle Insertion 0 Inserts an idle cycle between the bus cycles when the external read cycle is followed by external write cycle. 0: No idle cycle is inserted

- Endian Control Register (ENDIANCR) Number of bits: 16 Address: H'FFFD95

Bit	Bit Name	Set Value	R/W	Module
2	LE2	0	R/W	Little Endian Select Selects the endian for the corresponding area. 0: Data format of area 2 is specified as big endian

- SRAM Mode Control Register (SRAMCR) Number of bits: 16 Address: H'FFFD98

Bit	Bit Name	Set Value	R/W	Module
10	BCSEL2	0	R/W	Byte Control SRAM Interface Select Selects the bus interface for the corresponding area. 0: Area 2 is basic bus interface

- DRAM Control Register (DRAMCR) Number of bits: 16 Address: H'FFFDA0

Bit	Bit Name	Set Value	R/W	Module
15	DRAME	1	R/W	Area 2 DRAM Interface Select Selects whether or not area 2 is specified as the DRAM/SDRAM interface. When this bit is set to 1, select the type of DRAM to be used in area 2 with the DTYPE bit. 1: DRAM/SDRAM interface
14	DTYPE	1	R/W	DRAM Select Selects the type of DRAM to be used in area 2. 1: SDRAM is used in area 2
11	OEE	1	R/W	$\overline{OE}$ Output Enable The $\overline{OE}$ signal is output when DRAM with the EDO page mode is connected, whereas the CKE signal is output when SDRAM is connected. 1: $\overline{OE}$/CKE signal enabled
7	BE	1	R/W	Burst Access Enable Enables or disables a burst access to the DRAM/SDRAM. The DRAM/SDRAM is accessed in high-speed page mode. When DRAM with the EDO page mode is used, connect the $\overline{OE}$ signal of this LSI to the $\overline{OE}$ signal of DRAM. 1: DRAM/SDRAM is accessed in high-speed page mode
6	RCDM	1	R/W	RAS Down Mode Selects the $\overline{RAS}$ signal state while a DRAM access is halted when a basic bus interface area or an on-chip I/O register is accessed: keep the $\overline{RAS}$ signal low (RAS down mode) and high (RAS up mode). 1: RAS down mode when the DRAM/SDRAM is accessed
1	MXC1	0	R/W	Multiplexed Address Bit Select
0	MXC0	0	R/W	Select the number of bits by which a row address multiplexed with a column address is shifted to the lower side. At the same time, these bits select row address bits compared during a burst access to the DRAM/SDRAM interface. 00: A23 to A9 are compared for 16-bit access space

- DRAM Access Control Register (DRACCR) Number of bits: 16 Address: H'FFFDA2

Bit	Bit Name	Set Value	R/W	Module
13	TPC1	0	R/W	Precharge Cycle Control
12	TPC0	0	R/W	Select the number of RAS precharge cycles on a normal access and a refresh cycle. 00: One cycle
9	RCD1	0	R/W	$\overline{RAS}$-$\overline{CAS}$ Wait Control
8	RCD0	0	R/W	Select the number of wait cycles inserted between $\overline{RAS}$ and $\overline{CAS}$ cycles. 00: No wait cycle inserted

- Refresh Control Register (REFCR) Number of bits: 16 Address: H'FFFDA6

Bit	Bit Name	Set Value	R/W	Module
10	RTCK2	0	R/W	Refresh Counter Clock Select
9	RTCK1	1	R/W	Select the clock used to count up the refresh counter from the
8	RTCK0	0	R/W	seven internal clocks generated by dividing the on-chip peripheral module clock (Pϕ). When the clock is selected, the refresh counter starts to count up. 010: Counts on Pϕ/8
7	RFSHE	1	R/W	Refresh Control Enables or disables refresh control. 1: Refresh control disabled
6	RLW2	0	R/W	Refresh Cycle Wait Control
5	RLW1	0	R/W	Select the number of wait cycles during a CAS before RAS refresh
4	RLW0	0	R/W	cycle for the DRAM interface and an auto-refresh cycle for the SDRAM interface. 000: No wait cycle inserted
3	SLFRF	1	R/W	Self-Refresh Enable Selects the self-refresh mode for the DRAM/SDRAM interface when a transition to the software standby mode is made with this bit set to 1. To perform a self-refresh cycle when the SDRAM interface is selected, enable the CKE output by setting the OEE bit in DRAMCR. 1: Enables self-refresh
2	TPCS2	0	R/W	Precharge Cycle Control during Self-Refresh
1	TPCS1	0	R/W	Selects the number of precharge cycles immediately after a self-
0	TPCS0	0	R/W	refresh cycle. 000: No wait cycle inserted

- Refresh Timer Counter (RTCNT) Number of bits: 8 Address: H'FFFDA8
  Function: RTCNT increments the internal clock selected by bits RTCK2 to RTCK0 in REFCR.
  Setting value: H'00

- Refresh Time Constant Register (RTCOR) Number of bits: 8 Address: H'FFFDA9
  Function: RTCOR specifies the interval at which a compare match with RTCNT is generated.
  Setting value: H'30 (refresh interval: 15.68 μs)

- Deep Standby Wait Control Register (DPSWCR) Number of bits: 8 Address: H'FFFE71

Bit	Bit Name	Set Value	R/W	Module
5	WTSTS5	0	R/W	Deep Software Standby Wait Time Setting Bits
4	WTSTS4	0	R/W	These bits specify the amount of time the MCU waits for the clock
3	WTSTS3	1	R/W	to stabilize when deep software standby mode is canceled by an
2	WTSTS2	1	R/W	interrupt.
1	WTSTS1	0	R/W	001101: Wait time = 131,072 states
0	WTSTS0	1	R/W	

- Standby Control Register (SBYCR) Number of bits: 16 Address: H'FFFDC6

Bit	Bit Name	Set Value	R/W	Module
15	SSBY	1	R/W	Software Standby Specifies the transition mode after executing the SLEEP instruction. 1: Shifts to software standby mode after the SLEEP instruction is executed
14	OPE	1	R/W	Output Port Enable Specifies whether the output of the address bus and bus control signals is retained or these lines are set to the high-Z state in software standby mode or deep software standby mode. 1: In software standby mode or deep software standby mode, output states of address bus and bus control signals are retained.

- Deep Standby Control Register (DPSBYCR) Number of bits: 8 Address: H'FFFE70

Bit	Bit Name	Set Value	R/W	Module
7	DPSBY	1	R/W	Deep Software Standby When the SSBY bit in SBYCR has been set to 1, executing the SLEEP instruction causes a transition to software standby mode. At this time, if there is no source to clear software standby mode and this bit is set to 1, a transition to deep software standby mode is made. SSBY DPSBY 1 1: Enters deep software standby mode after execution of a SLEEP instruction.
6	IOKEEP	1	R/W	I/O Port Retention In deep software standby mode, the ports retain the states that were held in software standby mode. This bit specifies whether or not the state that has been held in deep software standby mode is retained after exit from deep software standby mode. 1: The retained port states are released when a 0 is written to this bit following exit from deep software standby mode.

- Deep Standby Interrupt Edge Register (DPSIEGR) Number of bits: 8 Address: H'FFFE74

Bit	Bit Name	Set Value	R/W	Module
0	DIRQ0EG	0	R/W	IRQ0 Interrupt Edge Select Selects the active edge for IRQ0 pin input. 0: The interrupt request is generated by a falling edge.

- Deep Standby Interrupt Enable Register (DPSIER) Number of bits: 8 Address: H'FFFE72

Bit	Bit Name	Set Value	R/W	Module
0	DIRQ0E	1	R/W	IRQ0 Interrupt Enable Enables or disables exit from deep software standby mode by IRQ0. 1: Enables exit from deep software standby mode by IRQ0.

- Deep Standby Interrupt Flag Register (DPSIFR) Number of bits: 8 Address: H'FFFE73

Bit	Bit Name	Set Value	R/W	Module
0	DIRQ0F	0	R/W	IRQ0 Interrupt Flag [Clearing condition] Writing a 0 to this bit after reading it as 1.

- Port Function Control Register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Set Value	R/W	Module
2	CS2E	1	R/W	CS2 Enable These bits enable/disable the corresponding $\overline{CS2}$ output. 1: Pin functions as $\overline{CS2}$ output pin

- Port Function Control Register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Set Value	R/W	Module
6	CS2S	1	R/W	$\overline{CS2}$ Output Pin Select Selects the output pin for $\overline{CS2}$ when $\overline{CS2}$ output is enabled (CS2E = 1) 1: Specifies pin PB1 as $\overline{CS2}$-B output pin

- Port Function Control Register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Set Value	R/W	Module
7 to 0	A23E to A16E	All 1	R/W	Address A23 to A16 Enable Enables/disables the address output (A23 to A16) 1: Enables the A23 to A16 output

- Port Function Control Register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Set Value	R/W	Module
0	ITS0	0	R/W	$\overline{\text{IRQ0}}$ Pin Select Selects an input pin for $\overline{\text{IRQ0}}$. 0: Selects pin P10 as $\overline{\text{IRQ0}}$-A input

- Data Direction Register (PDDDR) Number of bits: 8 Address: H'FFFB8C
- Data Direction Register (PEDDR) Number of bits: 8 Address: H'FFFB8D
- Data Direction Register (PFDDR) Number of bits: 8 Address: H'FFFB8E

  Function: The DDRs are 8-bit write-only registers whose bits specify the input or output status of the corresponding ports.

  Setting value: H'FF

- Input Buffer Control Register (P1ICR) Number of bits: 8 Address: H'FFFB90

  Function: ICR is an 8-bit readable/writable register that controls the port input buffers.

  Setting value: H'01

- Synchronous DRAM Control Register (SDCR) Number of bits: 16 Address: H'FFFDA4

Bit	Bit Name	Set Value	R/W	Module
15	MRSE	1/0	R/W	Mode Register Set Enable Enables the setting in the SDRAM mode register. 0: Disables to set the SDRAM mode register 1: Enables to set the SDRAM mode register

(5) Flowchart

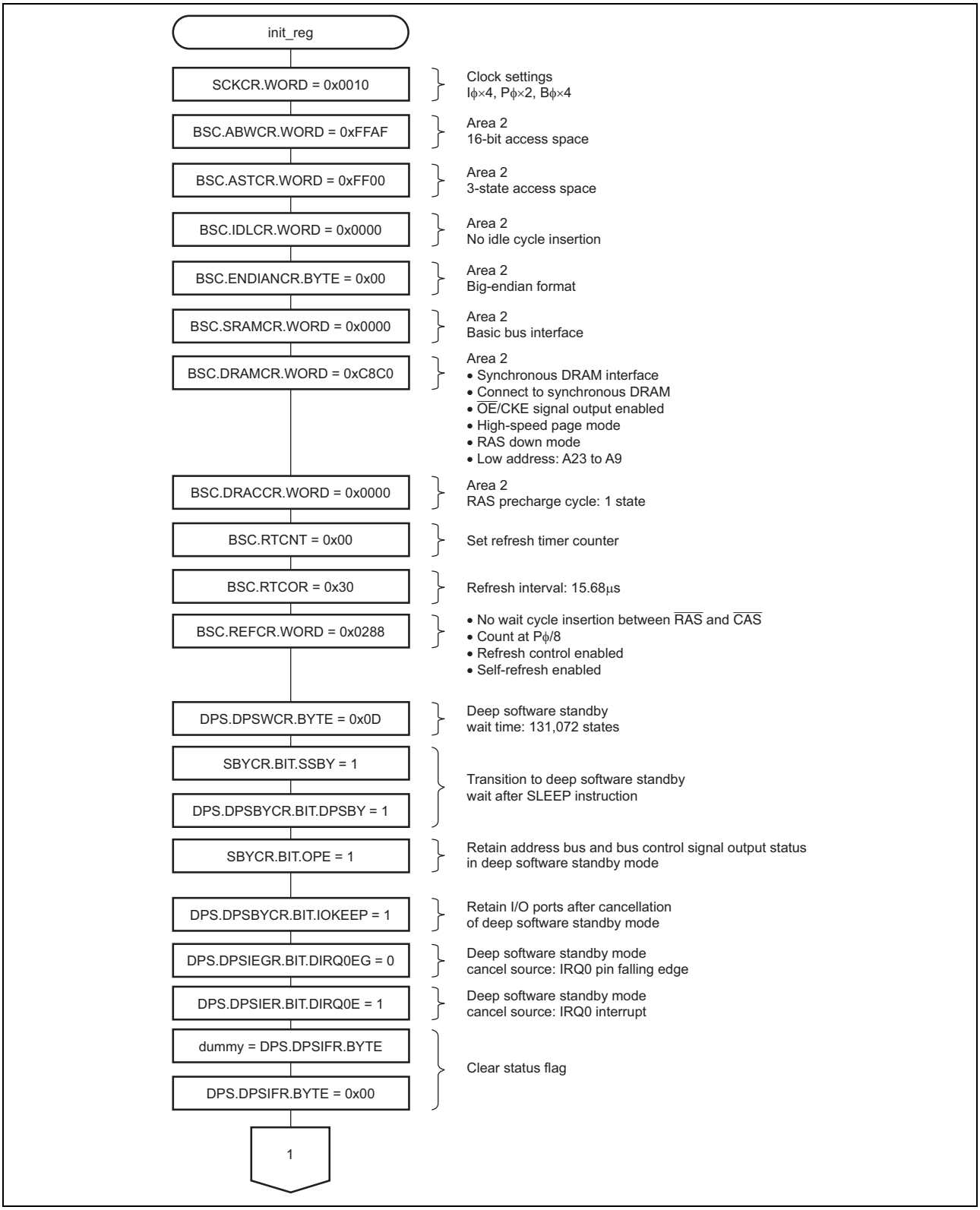


Figure 6 Flowchart (init_reg)

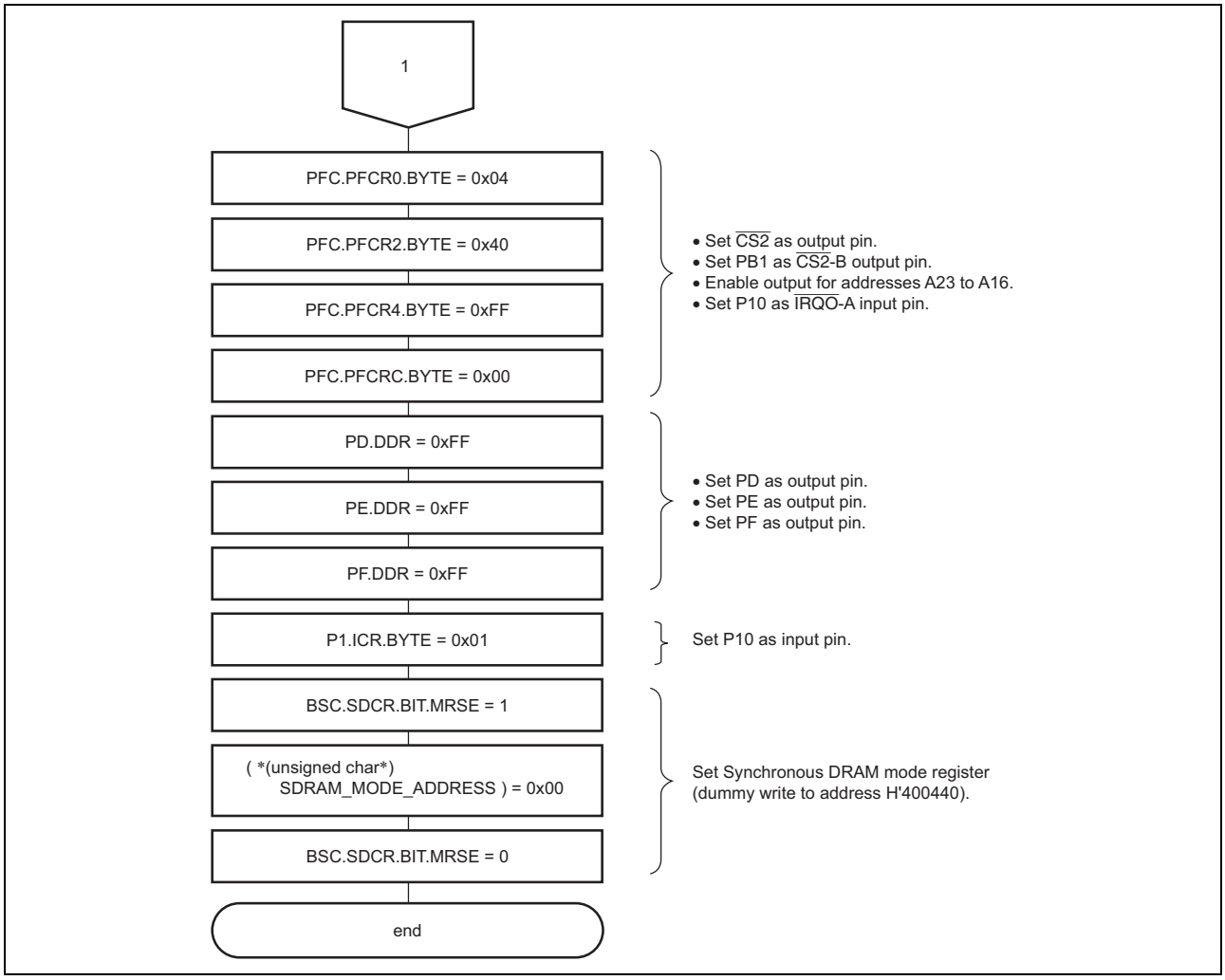


Figure 7 Flowchart (init_reg)

5.3.4 init_ram Function

(1) Functional Overview

The init_ram function stores values in the entire SDRAM area.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

None

(5) Flowchart

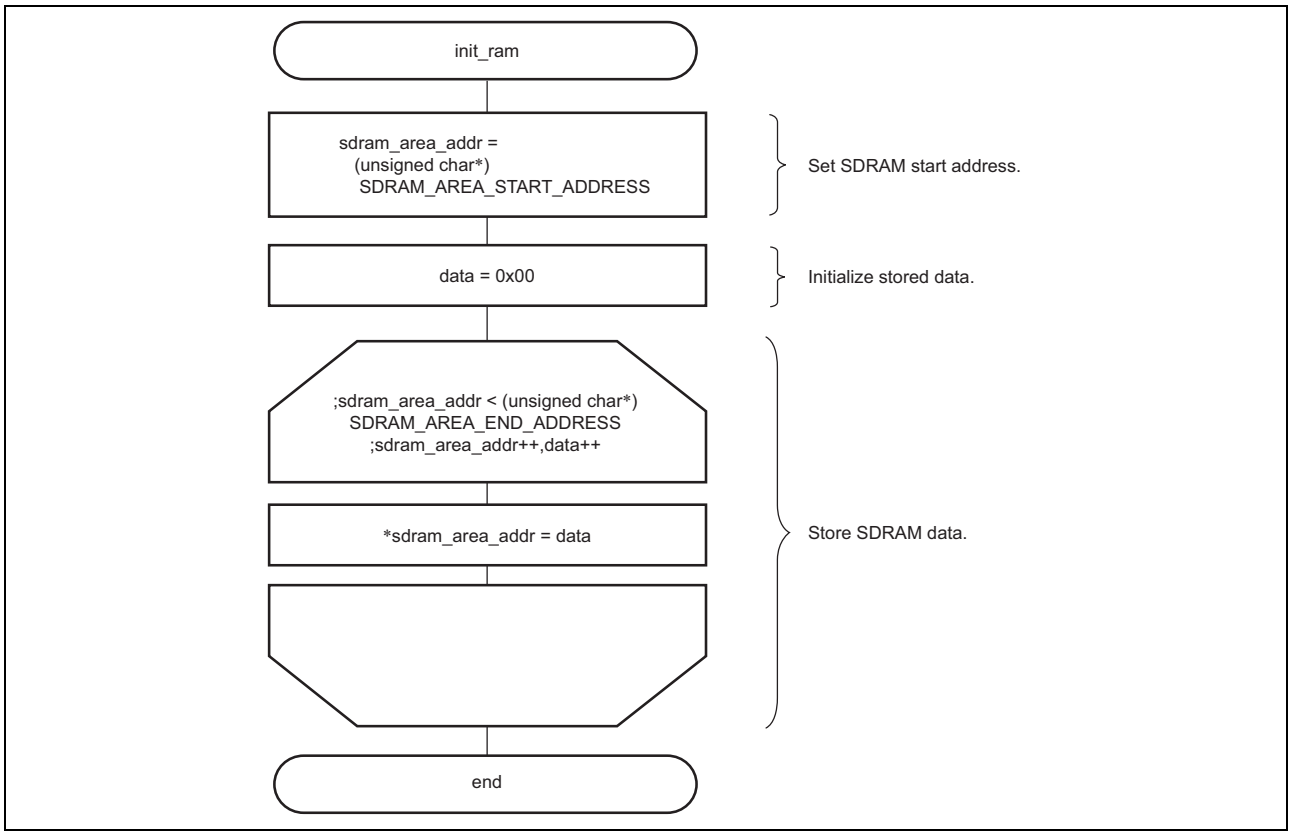


Figure 8 Flowchart (init_ram)

5.3.5 init_exit_dps Function

(1) Functional Overview

The init_exit_dps function initializes various registers after cancellation of deep software standby mode.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- System Clock Control Register (SCKCR) Number of bits: 16 Address: H'FFFDC4

Bit	Bit Name	Set Value	R/W	Module
15	PSTOP1	0/1	R/W	Bϕ Clock Output Enable Controls ϕ output on PA7. • Normal operation 0: ϕ output 1: Fixed high
14	PSTOP0	0/1	R/W	ϕ Clock Output Enable Controls ϕ output (SDϕ) on PB7. • Normal operation 0: ϕoutput 1: Fixed high
10	ICK2	0	R/W	System Clock (Iϕ) Select
9	ICK1	0	R/W	These bits select the frequency of the system clock provided to the
8	ICK0	0	R/W	CPU, EXDMAC, DMAC, and DTC. The ratio to the input clock is as follows: 000: × 4
6	PCK2	0	R/W	Peripheral Module Clock (Pϕ) Select
5	PCK1	0	R/W	These bits select the frequency of the peripheral module clock. The
4	PCK0	1	R/W	ratio to the input clock is as follows: 001: × 2
2	BCK2	0	R/W	External Bus Clock (Bϕ) Select
1	BCK1	0	R/W	These bits select the frequency of the external bus clock. The ratio
0	BCK0	0	R/W	to the input clock is as follows: 000: × 4

- Reset Status Register (RSTSR) Number of bits: 8 Address: H'FFFE75

Bit	Bit Name	Set Value	R/W	Module
7	DPSRSTF	0	R/(W)	Deep Software Standby Reset Flag Indicates that deep software standby mode has been canceled by an interrupt source specified in DPSIER or DPSIEGR and an internal reset is generated. [Clearing condition] Writing a 0 to this bit after reading it as 1.

- Deep Standby Interrupt Flag Register (DPSIFR) Number of bits: 8 Address: H'FFFE73

Bit	Bit Name	Set Value	R/W	Module
0	DIRQ0F	0	R/W	IRQ0 Interrupt Flag [Clearing condition] Writing a 0 to this bit after reading it as 1.

- Port Function Control Register 0 (PFCR0) Number of bits: 8 Address: H'FFFBC0

Bit	Bit Name	Set Value	R/W	Module
2	CS2E	1	R/W	CS2 Enable These bits enable/disable the corresponding $\overline{CS2}$ output. 1: Pin functions as $\overline{CS2}$ output pin

- Port Function Control Register 2 (PFCR2) Number of bits: 8 Address: H'FFFBC2

Bit	Bit Name	Set Value	R/W	Module
6	CS2S	1	R/W	$\overline{CS2}$ Output Pin Select Selects the output pin for $\overline{CS2}$ when $\overline{CS2}$ output is enabled (CS2E = 1) 1: Specifies pin PB1 as $\overline{CS2}$-B output pin

- Port Function Control Register 4 (PFCR4) Number of bits: 8 Address: H'FFFBC4

Bit	Bit Name	Set Value	R/W	Module
7 to 0	A23E to A16E	All 1	R/W	Address A23 to A16 Enable Enables/disables the address output (A23 to A16) 1: Enables the A23 to A16 output

- Port Function Control Register C (PFCRC) Number of bits: 8 Address: H'FFFBCC

Bit	Bit Name	Set Value	R/W	Module
0	ITS0	0	R/W	$\overline{IRQ0}$ Pin Select Selects an input pin for $\overline{IRQ0}$. 0: Selects pin P10 as $\overline{IRQ0}$-A input

- Data Direction Register (P2DDR) Number of bits: 8 Address: H'FFFB81
- Data Direction Register (PBDDR) Number of bits: 8 Address: H'FFFB8A
- Data Direction Register (PDDDR) Number of bits: 8 Address: H'FFFB8C
- Data Direction Register (PEDDR) Number of bits: 8 Address: H'FFFB8D
- Data Direction Register (PFDDR) Number of bits: 8 Address: H'FFFB8E

  Function: The DDRs are 8-bit write-only registers whose bits specify the input or output status of the corresponding ports.

  Setting value: H'FF

- Data Register (P2DR) Number of bits: 8 Address: H'FFFF51
- Data Register (PBDR) Number of bits: 8 Address: H'FFFF5A

  Function: The DRs are 8-bit readable/writable registers that store output data for pins used as general output ports.

  Setting value: H'FF (P2DR), H'02 (PBDR)

- Deep Standby Control Register (DPSBYCR) Number of bits: 8 Address: H'FFFE70

Bit	Bit Name	Set Value	R/W	Module
6	IOKEEP	0	R/W	I/O Port Retention In deep software standby mode, the ports retain the states that were held in software standby mode. This bit specifies whether or not the state that has been held in deep software standby mode is retained after exit from deep software standby mode. 0: The retained port states are released simultaneously with exit from deep software standby mode.

- Bus Width Control Register (ABWCR) Number of bits: 16 Address: H'FFFD84

Bit	Bit Name	Set Value	R/W	Module
10	ABWH2	0	R/W	Area 7 to 0 Bus Width Control These bits select whether the corresponding area is to be designated as 8-bit access space or 16-bit access space. ABWH2 ABWL2 0 1: Area 2 is designated as 16-bit access space
2	ABWL2	1	R/W	

- Access State Control Register (ASTCR) Number of bits: 16 Address: H'FFFD86

Bit	Bit Name	Set Value	R/W	Module
10	AST2	1	R/W	Area 7 to 0 Access State Control These bits select whether the corresponding area is to be designated as 2-state access space or 3-state access space. Wait cycle insertion is enabled or disabled at the same time. 1: Area 2 is designated as 3-state access space Wait cycle insertion in area 2 access is enabled

- Wait Control Register B (WTCRB) Number of bits: 16 Address: H'FFFD8A

Bit	Bit Name	Set Value	R/W	Module
10	W22	0	R/W	Area 2 Wait Control 2 to 0
9	W21	0	R/W	Setting of CAS latency (W22 is ignored.):
8	W20	1	R/W	01: SDRAM with a CAS latency of 2 is connected.

- Idle Control Register (IDLCR) Number of bits: 16 Address: H'FFFD90

Bit	Bit Name	Set Value	R/W	Module
14	IDLS2	0	R/W	Idle Cycle Insertion 2 Inserts an idle cycle between the bus cycles when the external write cycle is followed by external read cycle. 0: No idle cycle is inserted
12	IDLS0	0	R/W	Idle Cycle Insertion 0 Inserts an idle cycle between the bus cycles when the external read cycle is followed by external write cycle. 0: No idle cycle is inserted

- Endian Control Register (ENDIANCR) Number of bits: 16 Address: H'FFFD95

Bit	Bit Name	Set Value	R/W	Module
2	LE2	0	R/W	Little Endian Select Selects the endian for the corresponding area. 0: Data format of area 2 is specified as big endian

- SRAM Mode Control Register (SRAMCR) Number of bits: 16 Address: H'FFFD98

Bit	Bit Name	Set Value	R/W	Module
10	BCSEL2	0	R/W	Byte Control SRAM Interface Select Selects the bus interface for the corresponding area. 0: Area 2 is basic bus interface

- DRAM Control Register (DRAMCR) Number of bits: 16 Address: H'FFFDA0

Bit	Bit Name	Set Value	R/W	Module
15	DRAME	1	R/W	Area 2 DRAM Interface Select Selects whether or not area 2 is specified as the DRAM/SDRAM interface. When this bit is set to 1, select the type of DRAM to be used in area 2 with the DTYPE bit. 1: DRAM/SDRAM interface
14	DTYPE	1	R/W	DRAM Select Selects the type of DRAM to be used in area 2. 1: SDRAM is used in area 2
11	OEE	1	R/W	$\overline{OE}$ Output Enable The $\overline{OE}$ signal is output when DRAM with the EDO page mode is connected, whereas the CKE signal is output when SDRAM is connected. 1: $\overline{OE}$/CKE signal enabled
7	BE	1	R/W	Burst Access Enable Enables or disables a burst access to the DRAM/SDRAM. The DRAM/SDRAM is accessed in high-speed page mode. When DRAM with the EDO page mode is used, connect the $\overline{OE}$ signal of this LSI to the $\overline{OE}$ signal of DRAM. 1: DRAM/SDRAM is accessed in high-speed page mode
6	RCDM	1	R/W	RAS Down Mode Selects the $\overline{RAS}$ signal state while a DRAM access is halted when a basic bus interface area or an on-chip I/O register is accessed: keep the $\overline{RAS}$ signal low (RAS down mode) and high (RAS up mode). 1: RAS down mode when the DRAM/SDRAM is accessed
1	MXC1	0	R/W	Multiplexed Address Bit Select
0	MXC0	0	R/W	Select the number of bits by which a row address multiplexed with a column address is shifted to the lower side. At the same time, these bits select row address bits compared during a burst access to the DRAM/SDRAM interface. 00: A23 to A9 are compared for 16-bit access space

- DRAM Access Control Register (DRACCR) Number of bits: 16 Address: H'FFFDA2

Bit	Bit Name	Set Value	R/W	Module
13	TPC1	0	R/W	Precharge Cycle Control
12	TPC0	0	R/W	Select the number of RAS precharge cycles on a normal access and a refresh cycle. 00: One cycle
9	RCD1	0	R/W	$\overline{RAS}$-$\overline{CAS}$ Wait Control
8	RCD0	0	R/W	Select the number of wait cycles inserted between $\overline{RAS}$ and $\overline{CAS}$ cycles. 00: No wait cycle inserted

- Refresh Control Register (REFCR) Number of bits: 16 Address: H'FFFDA6

Bit	Bit Name	Set Value	R/W	Module
10	RTCK2	0	R/W	Refresh Counter Clock Select
9	RTCK1	1	R/W	Select the clock used to count up the refresh counter from the
8	RTCK0	0	R/W	seven internal clocks generated by dividing the on-chip peripheral module clock (Pϕ). When the clock is selected, the refresh counter starts to count up. 010: Counts on Pϕ/8
7	RFSHE	1	R/W	Refresh Control Enables or disables refresh control. 1: Refresh control disabled
6	RLW2	0	R/W	Refresh Cycle Wait Control
5	RLW1	0	R/W	Select the number of wait cycles during a CAS before RAS refresh
4	RLW0	0	R/W	cycle for the DRAM interface and an auto-refresh cycle for the SDRAM interface. 000: No wait cycle inserted
3	SLFRF	1	R/W	Self-Refresh Enable Selects the self-refresh mode for the DRAM/SDRAM interface when a transition to the software standby mode is made with this bit set to 1. To perform a self-refresh cycle when the SDRAM interface is selected, enable the CKE output by setting the OEE bit in DRAMCR. 1: Enables self-refresh
2	TPCS2	0	R/W	Precharge Cycle Control during Self-Refresh
1	TPCS1	0	R/W	Selects the number of precharge cycles immediately after a self-
0	TPCS0	0	R/W	refresh cycle. 000: No wait cycle inserted

- Refresh Timer Counter (RTCNT) Number of bits: 8 Address: H'FFFDA8
  Function: RTCNT increments the internal clock selected by bits RTCK2 to RTCK0 in REFCR.
  Setting value: H'00

- Refresh Time Constant Register (RTCOR) Number of bits: 8 Address: H'FFFDA9
  Function: RTCOR specifies the interval at which a compare match with RTCNT is generated.
  Setting value: H'30 (refresh interval: 15.68 μs)

(5) Flowchart

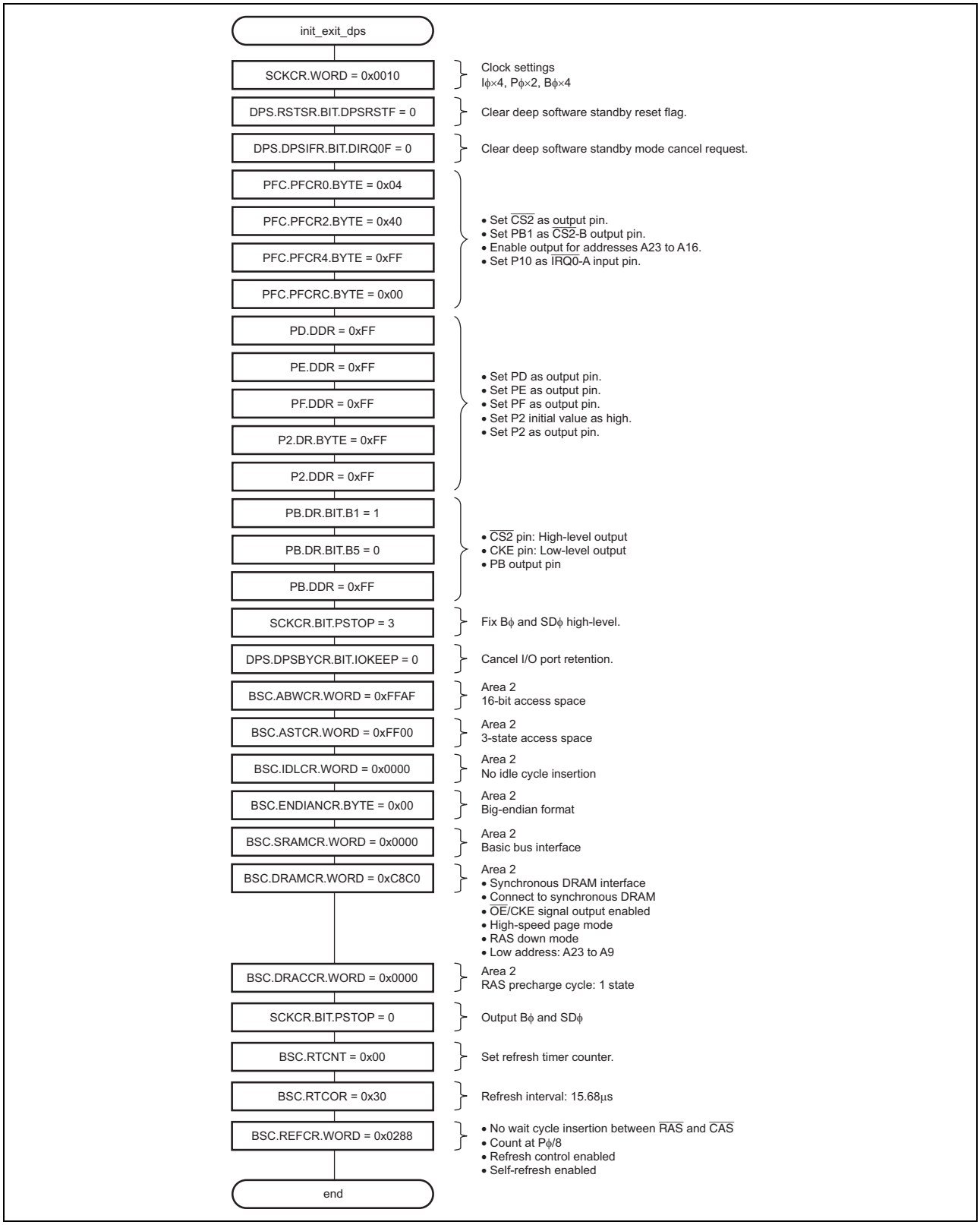


Figure 9 Flowchart (init_exit_dps)

5.3.6 cmp_data Function

(1) Functional Overview

The cmp_data function compares the SDRAM data before the transition to and after cancellation of deep software standby mode. Then it indicates the comparison result.

(2) Arguments

None

(3) Returned values

None

(4) Description of internal I/O registers used

The internal I/O registers used by this function are shown below. Note that the setting values shown are those used for this sample task and differ from the initial values.

- Data Register (P2DR) Number of bits: 8 Address: H'FFFF51
  Function: The DRs are 8-bit readable/writable registers that store output data for pins used as general output ports.
  Setting value: H'FE (OK indication), H'FD (error indication)

(5) Flowchart

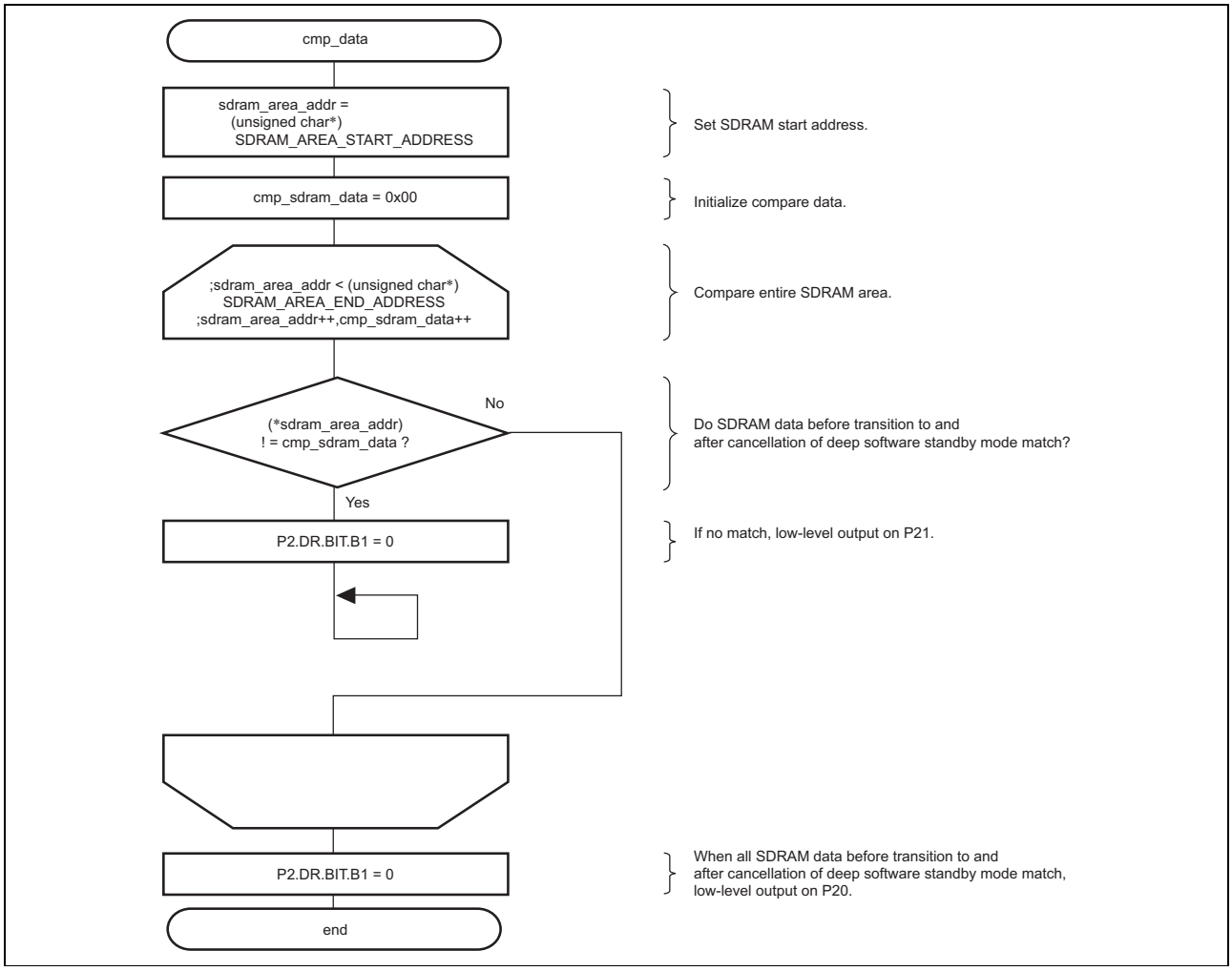


Figure 10 Flowchart (cmp_data)

6. Notes

(1) Only write to SDCR when the synchronous DRAM area is not being accessed. Also, SDCR must be set to the default value when the synchronous DRAM interface is not used. For details, see the hardware manual.
(2) When REFCR, RTCNT, and RTCOR are set to enable refresh after cancellation of deep software standby mode, ensure that the interval from the change in the state of the CKE signal to auto-refresh fits within the specification for the synchronous DRAM refresh interval. For details, see the hardware manual.

7. Reference Documents

- Hardware Manual
  H8SX/1668R Group Hardware Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Development Environment Manual
  H8S/300, H8/300 Series C/C++ Compiler Package User's Manual
  (The latest version can be downloaded from the Renesas Technology Web site.)
- H8SX Family Application Note
  Synchronous DRAM Interface, document No: RJJ06B0791
  (The latest version can be downloaded from the Renesas Technology Web site.)
- Technical News/Technical Updates
  (The latest information can be downloaded from the Renesas Technology Web site.)

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