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M32C/85 Group

Intelligent I/O - Use of 2 Channels for Clock Synchronous Serial Communication and 4 Channels for PWM Output (Variable PWM Cycle)

1. Abstract

This application note describes a procedure to use 2 channels for clock synchronous serial communication and 4 channels for PWM output (variable PWM cycle).

2. Introduction

The explanation of this issue is applied to the following condition:
Applicable MCU: M32C/85 Group, 144-pin package
(In a 100-pin package, eight intelligent I/O waveform output ports and five out of six intelligent I/O serial communication ports are shared)
System clock: 30 MHz

The program on this application note can also be used when operating other microcomputers within the M16C Family, provided they have the same SFRs (Special Function Registers) as the M32C/85 Group. However, some functions may have been modified. Refer to each device's hardware manual for details. Use functions covered in this application note only after careful evaluation.

3. Detailed Description

The intelligent I/O includes followings.

- 16-bit base timer register for free-running operation x 1
- 16-bit register for time measurement or waveform generation x 8
- A set of two 8-bit shift register for communications x 2

The OUTC1j (j = 4 to 7) pin outputs PWM waveform signal with variable cycle and variable duty ratio.
The transmit data for the clock synchronous serial communication is output from the ISTxDi (i = 0,1) pin and the transfer clock is output from the ISCLKi pin while the received data is input to the ISRxDi pin.

Table 1 lists pin settings for a sample program in this application note.

Figure 1. Assigned Pin Settings

Category	Pin No.	Pin Name	Port No.
Serial Communication Channel 1	34	ISTxD1	P73
	33	ISCLK1	P74
	32	ISRxD1	P75
Serial Communication Channel 0	31	ISTxD0	P76
	30	ISCLK0	P77
	29	ISRxD0	P80
Variable PWM Cycle Output	14	OUTC14	P140
	13	OUTC15	P141
	12	OUTC16	P142
	11	OUTC17	P143

Table 2 to Table 4 list selectable functions. The sample program is for when the checked functions are selected in those tables.

Table 2. PWM Output Channel j (j=4 to 7) Selectable Functions in Phase-Delayed Waveform Output Mode

Item	Settings	√
Default Output	"L" output as default	√
	"H" output as default	
Inverse Output Level	Output level is not inversed	√
	Output level is inversed	

Table 3. Selectable Functions in Communication 0 Clock Synchronous Serial Interface Mode

Item	Settings	√
Count Source		Cannot be selected
Divide Ratio of Count Source		Cannot be selected
Transfer Clock	Internal clock	√
	External clock	
Transfer Clock Setting	f8	
	f2n (n=15)	√
	Input from ISCLK0	
Transfer Format	LSB first	√
	MSB first	
ISRxD, ISTxD Polarity Inverse	No inverse	√
	Inverse	
Transmit Interrupt Cause	No data in the G0TB register	
	Transmission is completed	√

Table 4. Selectable Functions in Communication Unit 1 Clock Synchronous Serial Interface Mode

Item	Settings	√
Count Source	Stop clock	
	Apply two-phase pulse	
	f1	√
Divide Ratio of Count Source	Divide-by-2	
	:	
	Divide-by-64	
	No division	√
Transfer Clock	Internal clock	√
	External clock	
Transfer Clock Setting	Generate in channel 3 phase-delayed waveform output mode	√
	f8	
	f2n	
	Input from ISCLK0	
Transfer Format	LSB first	√
	MSB first	
ISRxD, ISTxD Polarity Inverse	No inverse	√
	Inversed	
Transmit Interrupt Cause	No data in the G1TB register	
	Transmission is completed	√

(1) Settings for PWM Cycle by Channel 0 and Transfer Speed of Communication Unit 1

Set the FSC0 bit in the G1FS register to 0 (selects the waveform generating function).
Set bits MOD 2 to 0 in the G1POCRj (j = 0 to 7) register to 111b.
Data output for communication unit 1 is automatically selected as to the ISTxD1 pin.
Set the RST1 bit in the G1BCR1 register to 0 (the base timer is not reset by matching with the G1PO0 register).
The base timer stays free-running.

(2) Output Setting for the ISCLK1 Pin

Set the FSC1 in the G1FS register to 0 (selects the waveform generating function).
Set bits MOD 2 to 0 in the G1POCRj (j = 0 to 7) register to 111b.
Clock output for communication unit 1 is automatically selected as to the ISCLK1 pin.

(3) Transfer Clock Generation by Channel 3 (Communication Unit 1)

The transfer clock is generated in phase-delayed waveform output mode of the channel 3 waveform generating function.
The G1PO3 register value is rewritten in the channel 3 waveform generating interrupt mode.
Figure 1 shows a flow chart for the G1PO3 register setting.

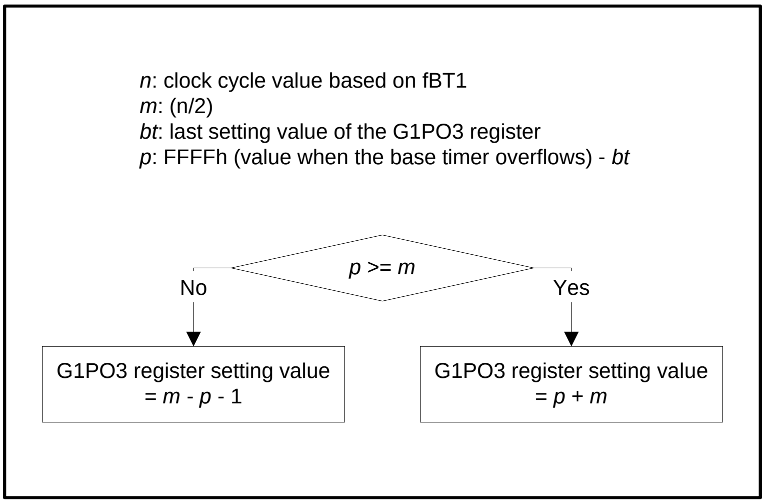

Figure 1. G1PO3 Register Setting

When fBT1 is the count source of base timer and *n* is a setting value of clock cycle based on fBT1, transfer speed of communication unit 1 (transfer clock cycle) can be calculated by the following equation.

$$\text{Transfer speed: } \frac{fBT1}{n}$$

(4) Low-level ("L") and High-level("H") Widths Setting of PWM Pulse by Channel j(j=4 to 7)

Set the "L" and "H" widths of PWM output in phase-delayed waveform output mode of channel j waveform generating function.

The G1POj register value is rewritten in the channel j waveform generating interrupt mode.

Figure 2 shows a flow chart for the G1POj register setting.

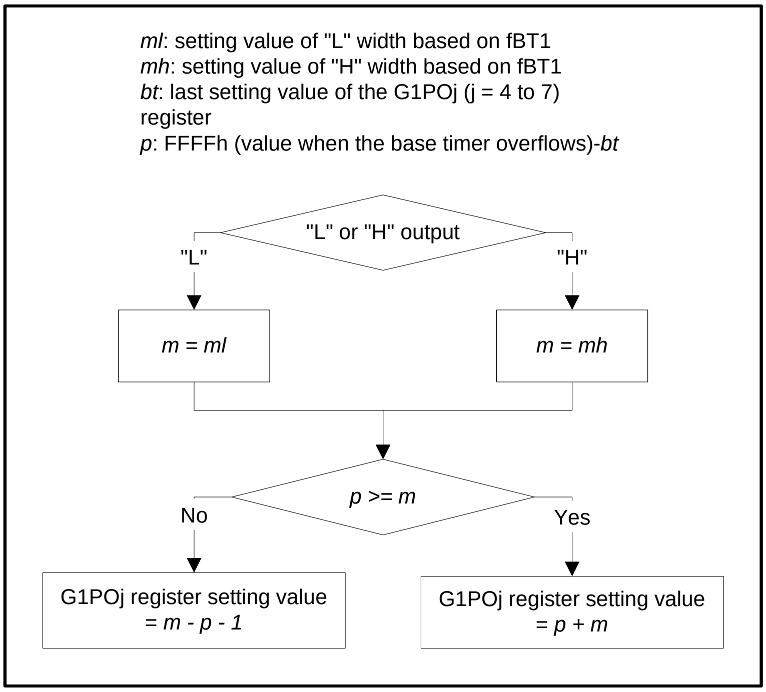

Figure 2. G1POj Register Setting

When fBT1 is the count source of base timer, *ml* is a setting value of an "L" width based on fBT1, and *mh* is a setting value of an "H" width, PWM cycle can be calculated by the following equation.

$$\text{PWM cycle}: \frac{ml + mh}{\text{fBT1}}$$

4. Settings for Sample Program

- Communication unit 1 bit rate: approx. 9600 bps
- Communication unit 1 bit rate: 1 Mbps

Sample program has the definition values as listed in Table 5. The "H" width ratio of channel j (j = 4 to 7) PWM output is increased in the sample program. When the frequency of duty ratio change reaches the set value ("3" for an example in Table 5), the ratio is back to the default. This routine is repeated.
The setting ranges of the definition values are based on the following conditions.

- Base timer count source frequency: approx. 33.3ns
- the maximum interrupt processing time: approx. 20μs

Obtain the "H" width and "L" width from the following equations and set the values to the G1POj (j=4 to 7) register.

$$\text{"H" width: Channel j PWM cycle} \times \frac{\text{Channel j "H" width ratio}}{100}$$

"L" width: Channel j PWM cycle - "H" width

Table 5. Definition Value of Sample Program

Item	Definition Value	Setting Range Conditions
Communication unit 1 transfer clock cycle(s)/2	1562	Approximately between 601 and 64984
Channel 4 PWM cycle	3000	Setting range of the G1PO4 register is approximately between 700 and 64900 (hecto-unit)
Channel 4 "H" width initial ratio (%)	60	Setting range of the G1PO4 register is approximately between 601 and 64984
Channel 4 PWM cycle increment	120	〃
Channel 4 "H" width increment ratio (%)	10	〃
Channel 5 PWM cycle	3000	Setting range of the G1PO5 register is approximately between 700 and 64900 (hecto-unit)
Channel 5 "H" width initial ratio (%)	50	Setting range of the G1PO5register is approximately between 601 and 64984
Channel 5 PW cycle increment	120	〃
Channel 5 "H" width increment ratio (%)	10	〃
Channel 6 PWM cycle	3000	Setting range of the G1PO6 register is approximately between 700 and 64900 (hecto-unit)
Channel 6 "H" width initial ratio (%)	40	Setting range of the G1PO6 register is approximately between 601 and 64984
Channel 6 PWM cycle increment	120	〃
Channel 6 "H" width increment ratio (%)	10	〃
Channel 7 PWM cycle	3000	Setting range of the G1PO5 register is approximately between 700 and 64900 (hecto-unit)
Channel 7 "H" width initial ratio (%)	40	Setting range of the G1PO7 register is approximately between 601 and 64984
Channel 7 PWM cycle increment	120	〃
Channel 7 "H" width increment ratio (%)	10	〃
Frequency of duty ratio change	3	Setting range of the G1POj (j = 4 to 7) register is approximately between 601 and 64984

4.1 Sample Program – CPU Utilization

The CPU utilization ratio of sample program is listed in Table 7. Table 6 shows the measuring conditions for CPU utilization. (Values of parameter measured are used as reference)

Table 6. Measuring Conditions for CPU Utilization

System clock	30MHz
Peripheral clock f2n	n = 15
Base timer count source cycle	1s ÷ 30 M = approx. 33.3ns
Base timer overflow cycle	33.3 ns × FFFFh = approx.2,182μs
Frequency of interrupts (z) to generate one PWM cycle and one communication unit 1 transfer clock cycle	Z = 2
Transfer clock of communication unit 0	30 M ÷ f2 n = 1 Mbps
Transfer clock of communication unit 1	Approx. 9600 bps
Value (x) to be set the G1PO3 register	x = 30 M ÷ 9600 ÷ z x = approx.1562 (round down to the whole number)
Frequency of Intelligent I/O waveform generating function 3 interrupt	FFFFh ÷ x = 41
Frequency of intelligent I/O communication unit 1 transmit interrupt	FFFFh ÷ (x × z × 8 bit) = 2
Frequency of intelligent I/O communication unit 1 receive interrupt	〃
PWM cycle	99900 ns
Value (y) of PWM cycle j (j = 4 to 7) based on fBT1	Y = 99900 ns ÷ 33.3ns y = 3000
Frequency of intelligent I/O waveform generating function j interrupt (j = 4 to 7)	FFFFh ÷ y × z = 43

Table 7. CPU Utilization

Interrupt Processing	Processing Time (μs)	Interrupt Frequency	Total Processing Time (μs)	CPU Utilization
Intelligent I/O communication unit 0 transmit interrupt	1.6	168	268.8	12.31 %
Intelligent I/O communication unit 0 receive interrupt	1.6	168	268.8	12.31 %
Intelligent I/O waveform generating function 3 interrupt (Communication unit 1 transfer clock generation)	1.8	41	73.8	3.38 %
Intelligent I/O communication unit 1 transmit interrupt	1	2	2	0.09 %
Intelligent I/O communication unit 1 receive interrupt	1	2	2	0.09 %
Intelligent I/O waveform generating function 4 interrupt	3.2	43	137.6	6.30 %
Intelligent I/O waveform generating function 5 interrupt	3.2	43	137.6	6.30 %
Intelligent I/O waveform generating function 6 interrupt	3.2	43	137.6	6.30 %
Intelligent I/O waveform generating function 7 interrupt	3.2	43	137.6	6.30 %
Total	19.8	553	1165.8	53 %

$$\text{CPU utilization: } \frac{\text{Total processing time}}{\text{Base timer overflow period (2,182 μs)}}$$

Interrupt frequency: number of times that interrupt is generated in a base timer overflow period

Figure 3 to Figure 6 show timing diagrams of the sample program

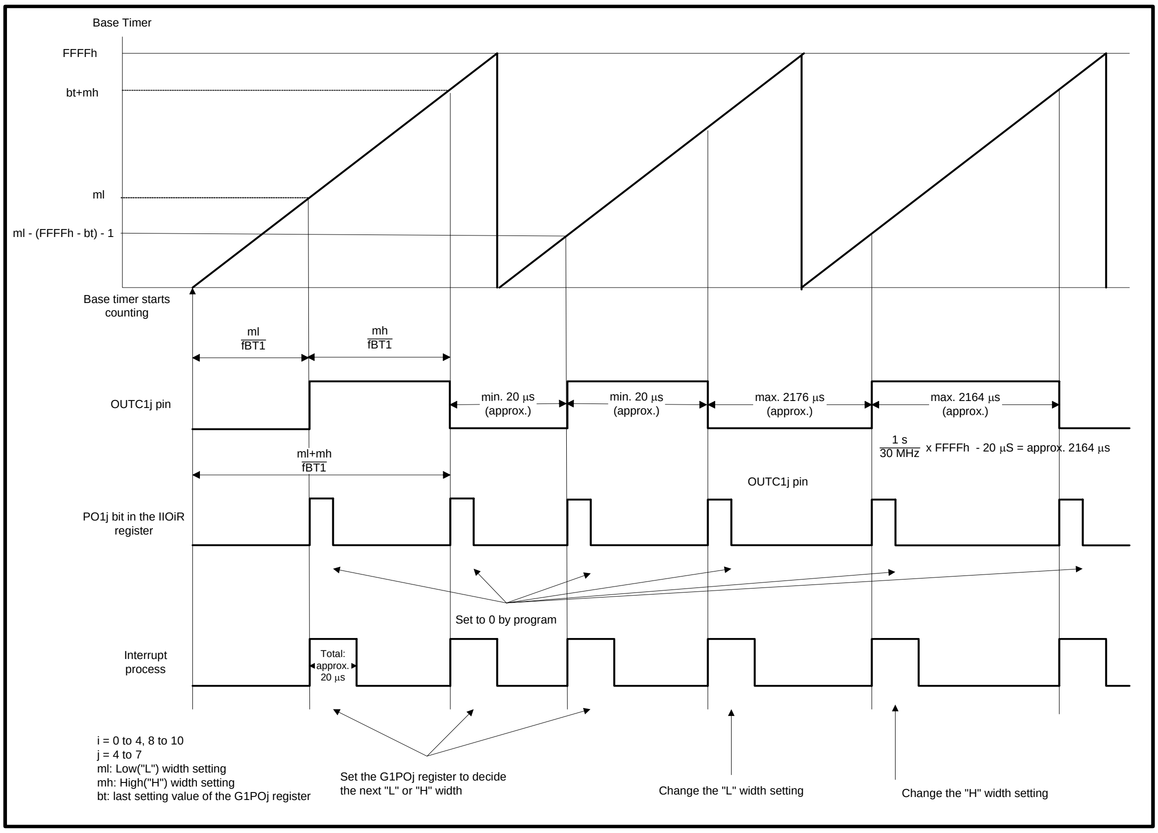

Figure 3. PWM Waveform Timing

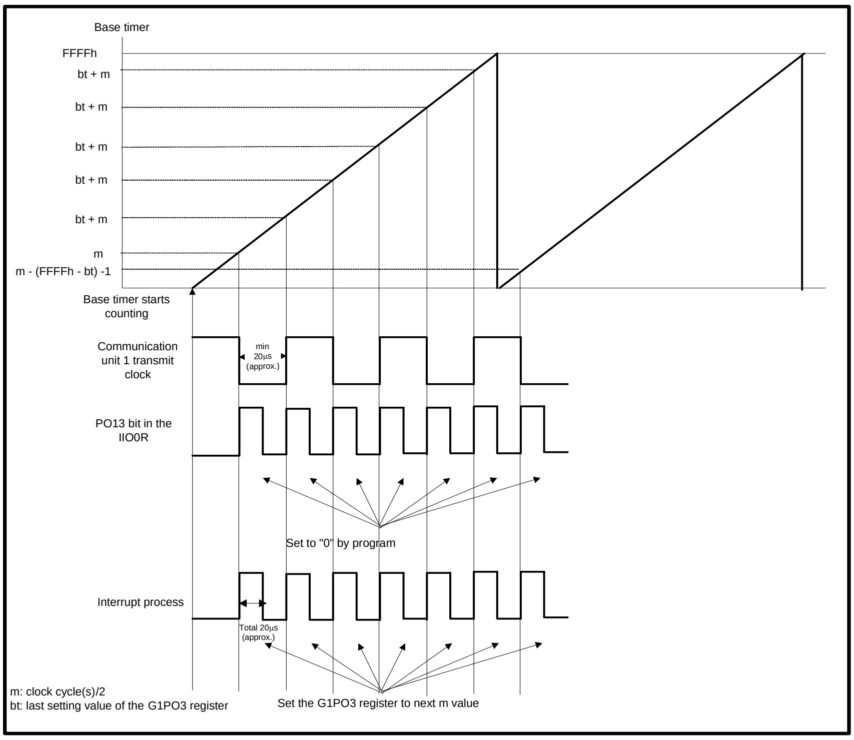

Figure 4. Transfer Clock Generating Timing of Communication Unit 1

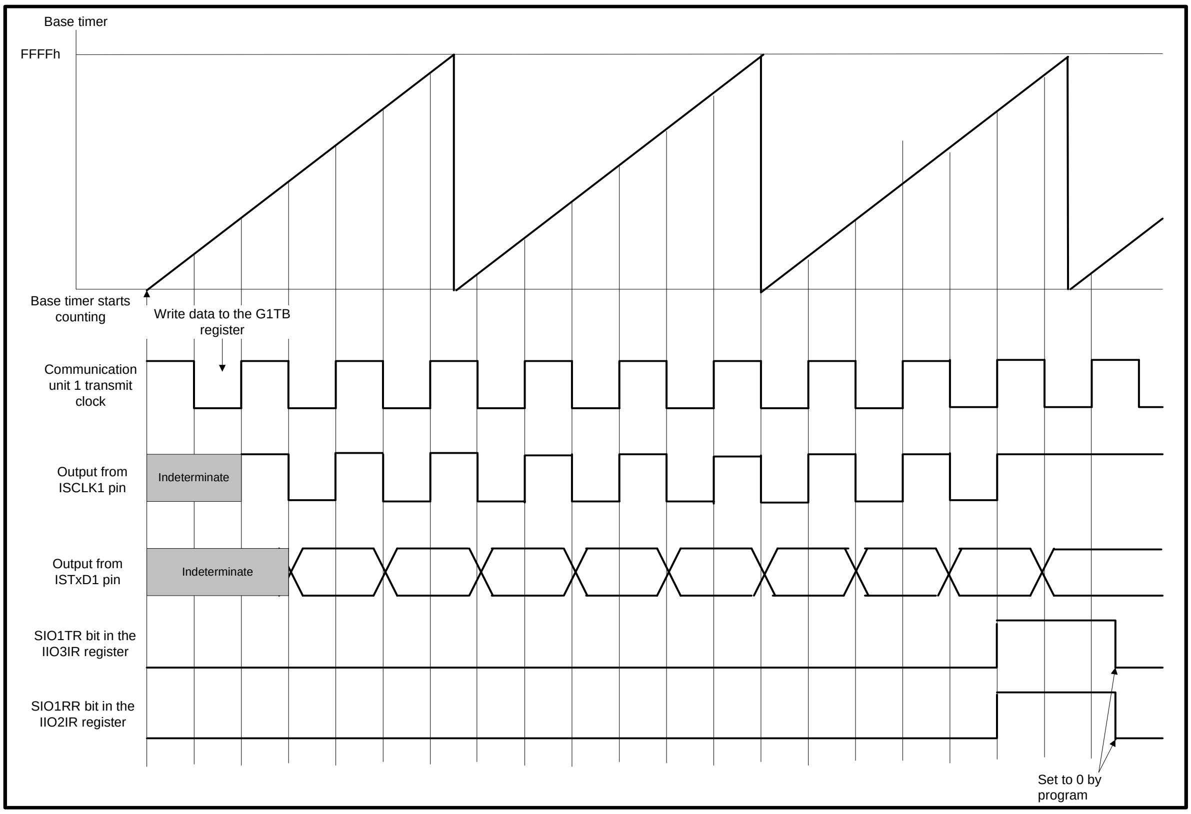

Figure 5. Transmit/Receive Timing of Communication Unit 1

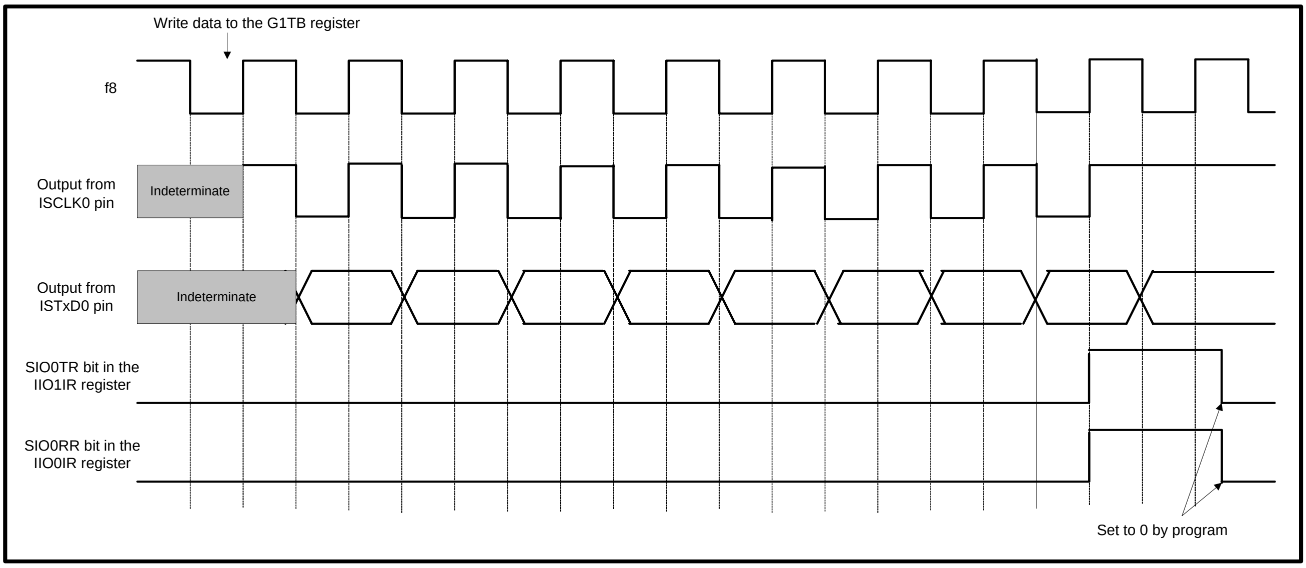

Figure 6. Transmit/Receive Timing of Communication Unit 0

Figure 7 to Figure 11 show flow charts of register settings.

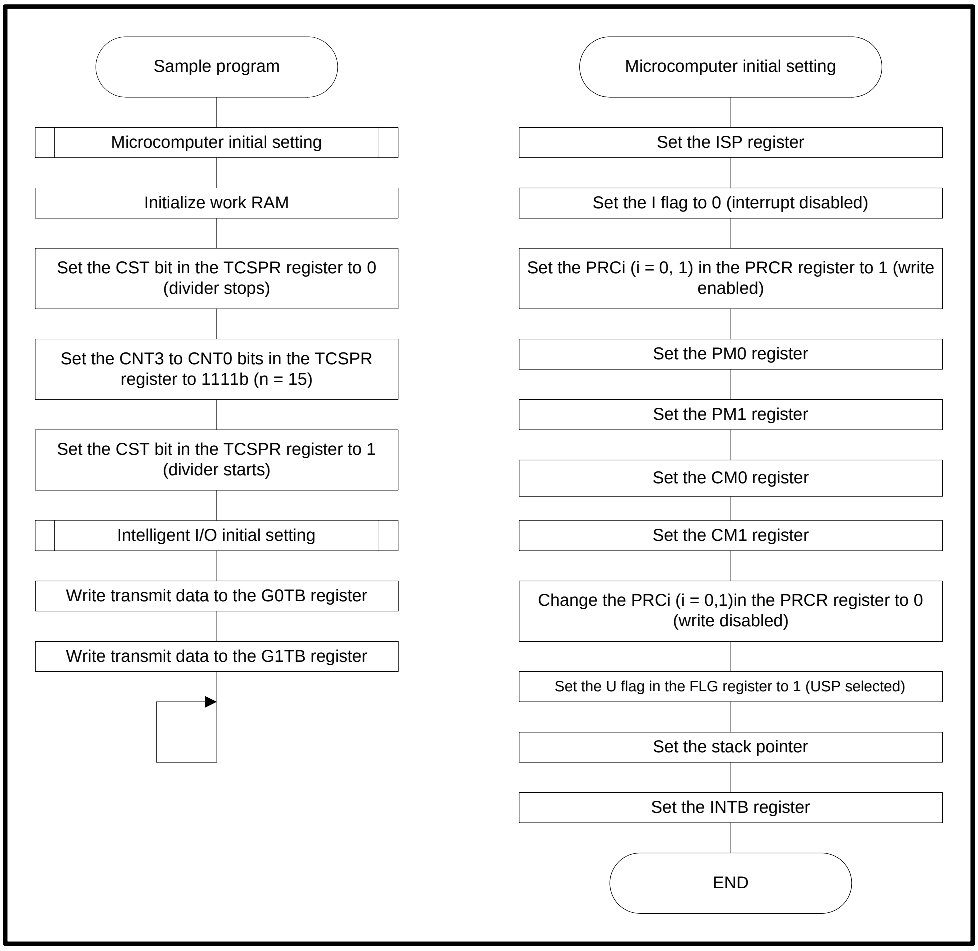

Figure 7. Register Setting (1)

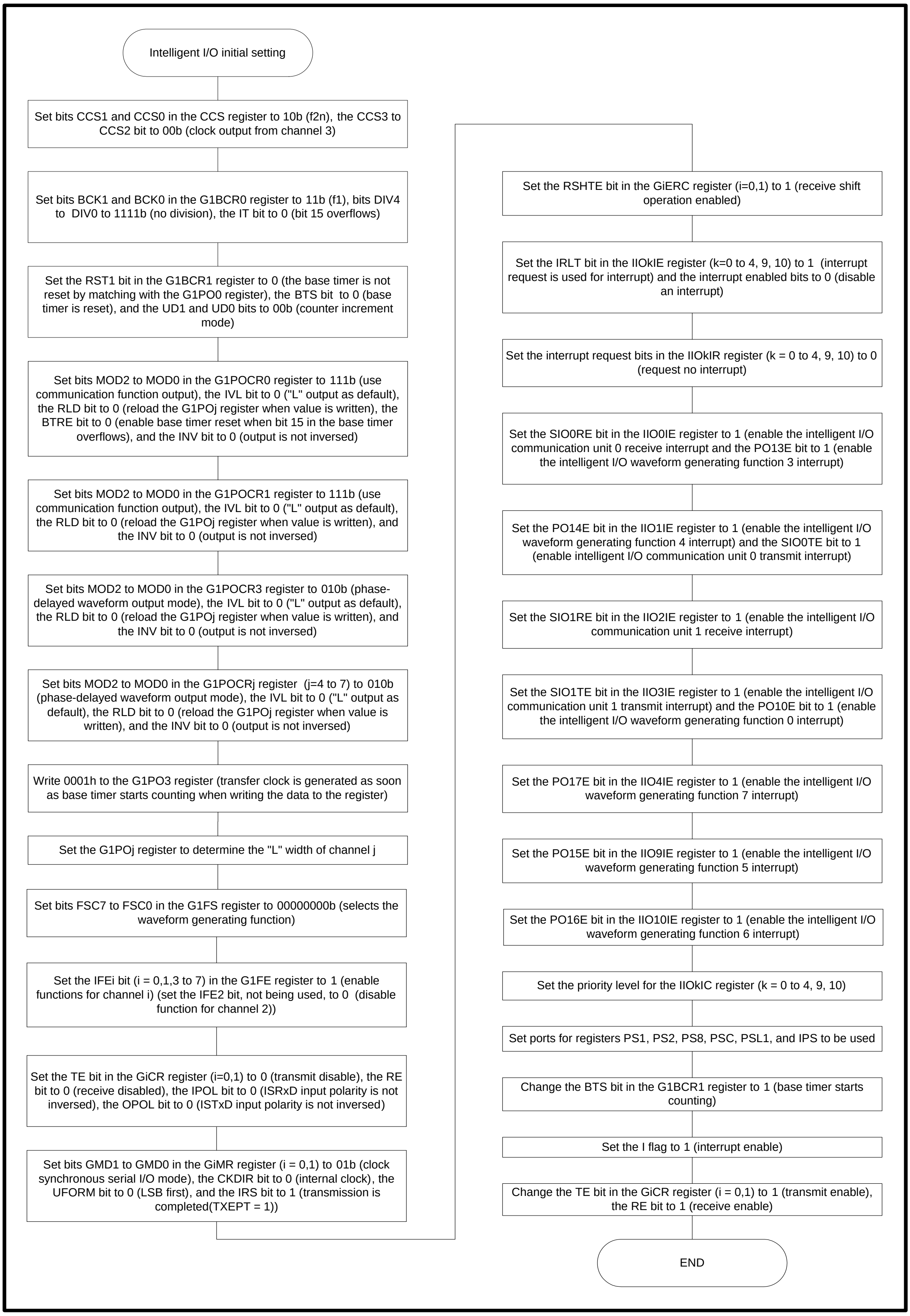

Figure 8. Register Settings (2)

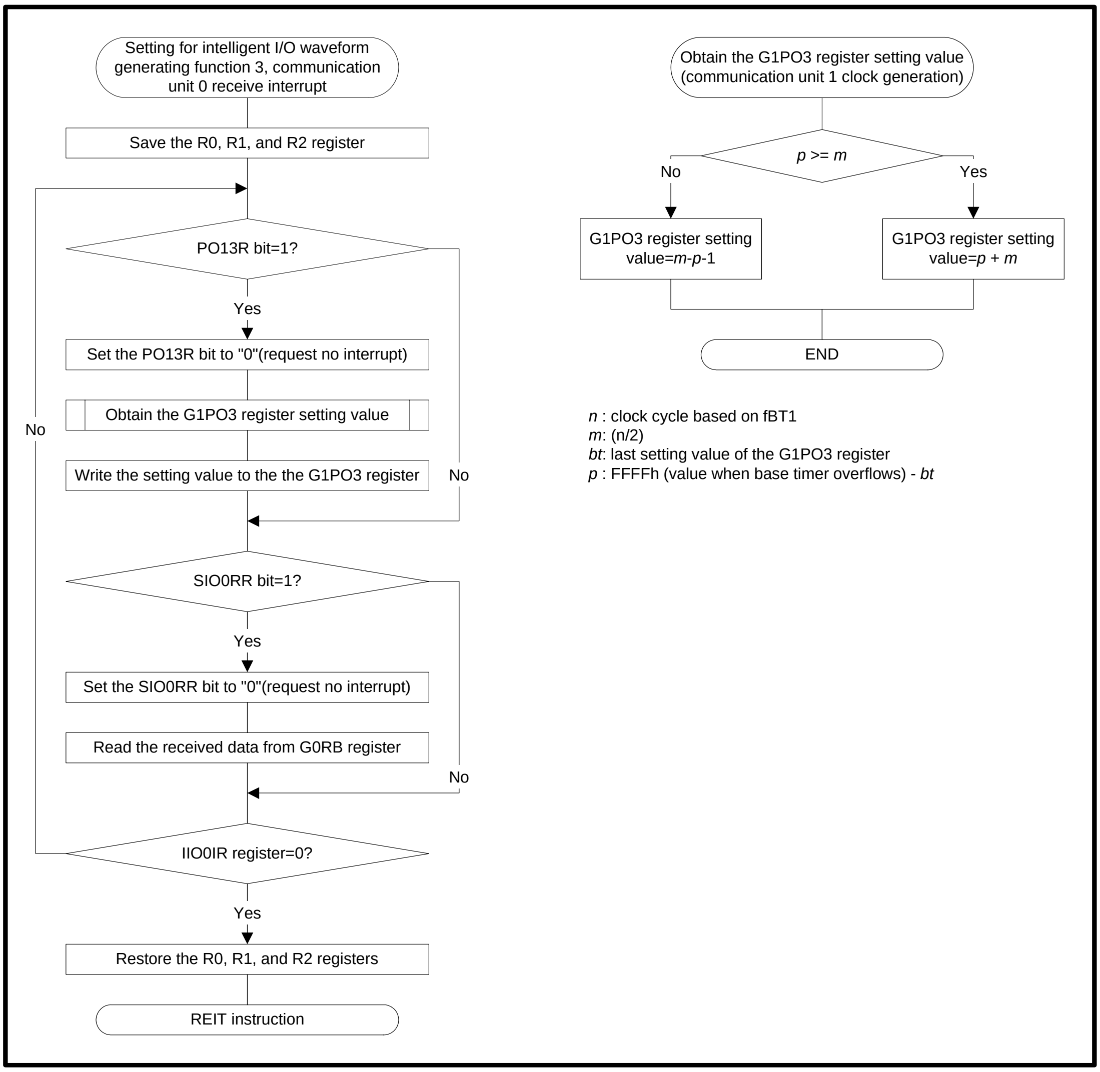

Figure 9.Register Settings (3)

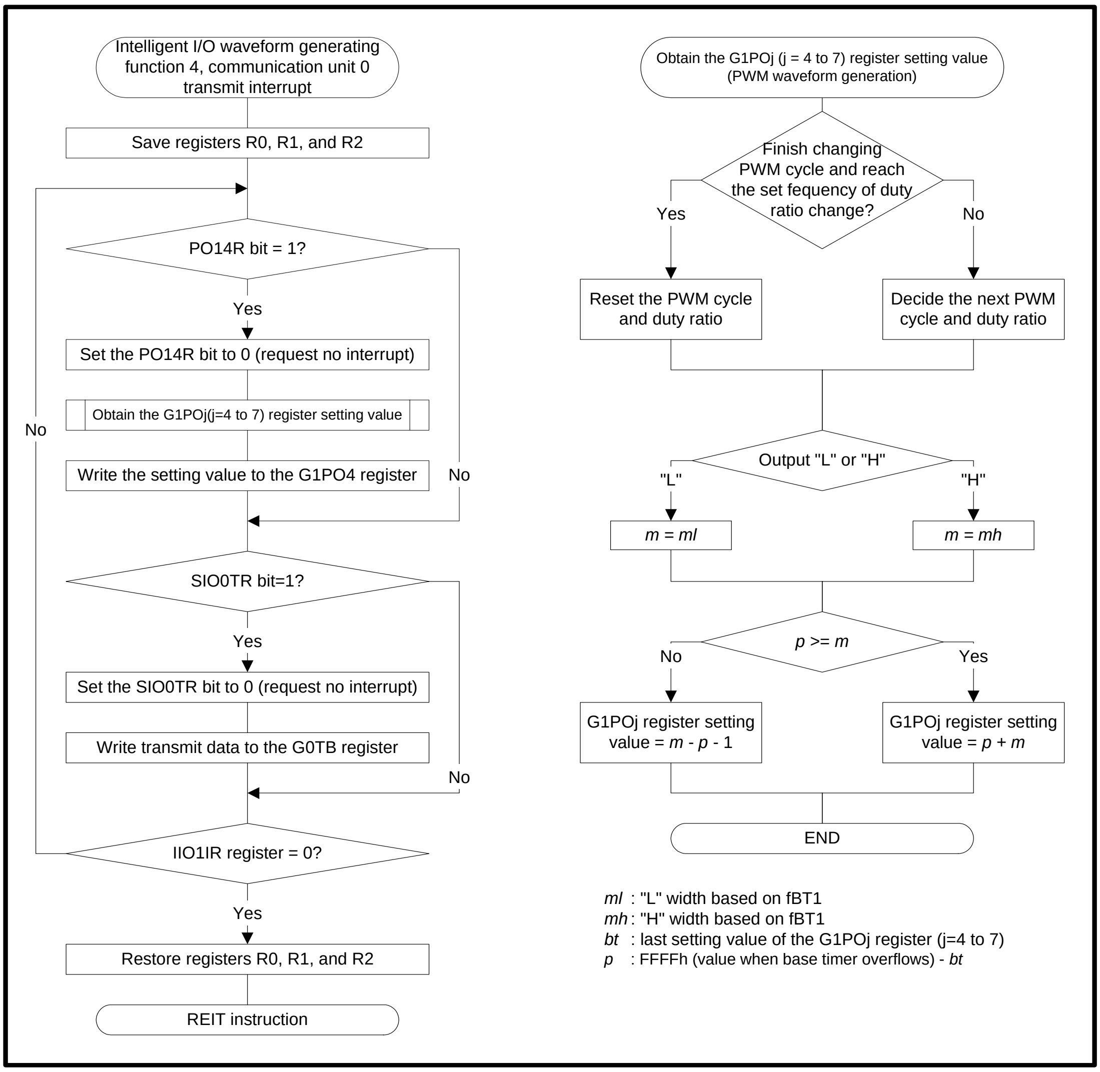

Figure 10. Register Settings (4)

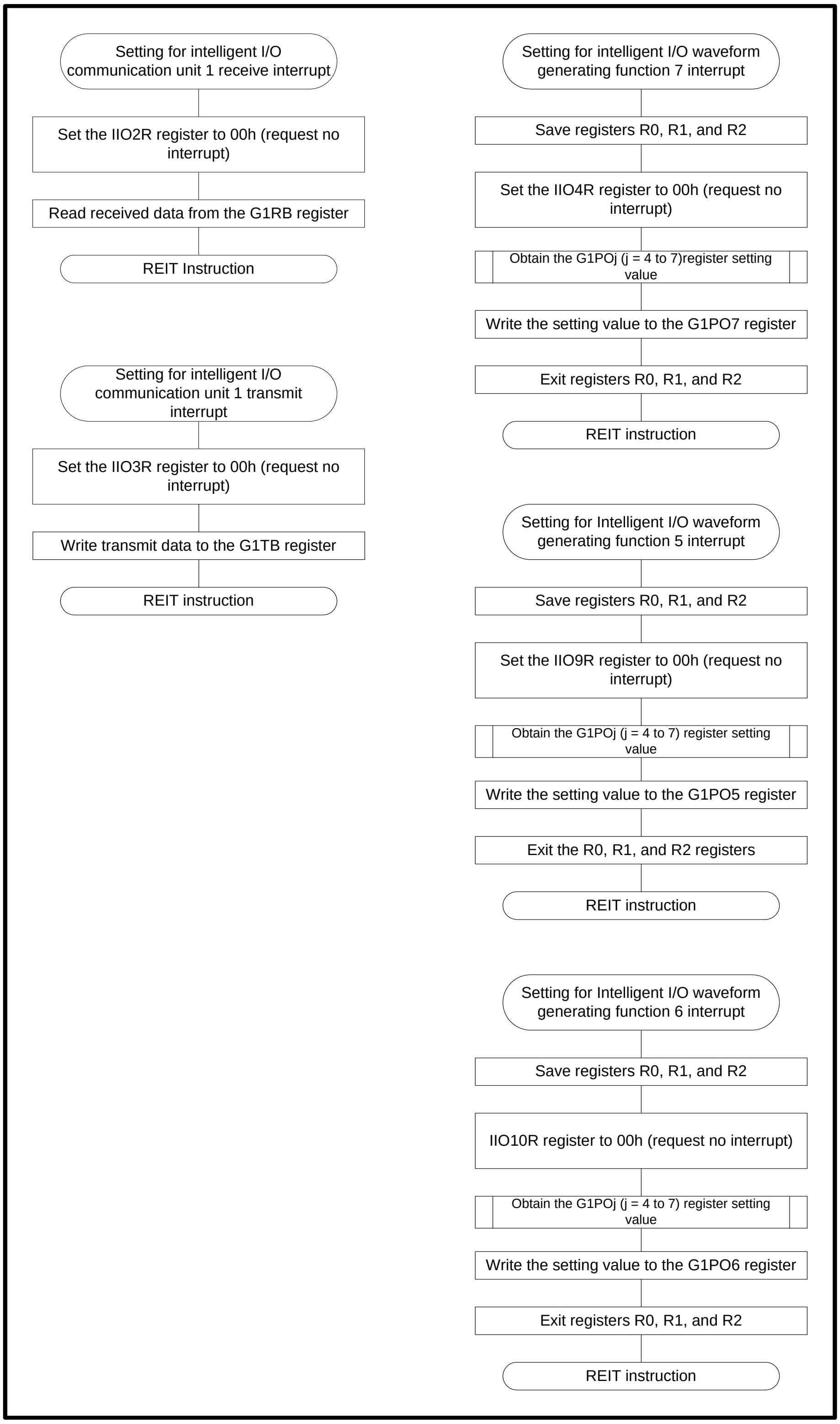

Figure 11. Register Settings (5)

5. Reference Program

Please find the reference program from the Renesas Technology Web site.
Click Application Note in the left menu of the M32C/80 Series top page.

6. Reference Documents

Hardware manual
M32C/85 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update
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csc@renesas.com

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