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# H8/300H Tiny Series

## Measuring the Pulse Cycle Using Input Capture Timer W

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### Introduction

You can use input capture timer W to measure the cycle of a pulse entered into the input capture input pin (FTIOA).

### Target Device

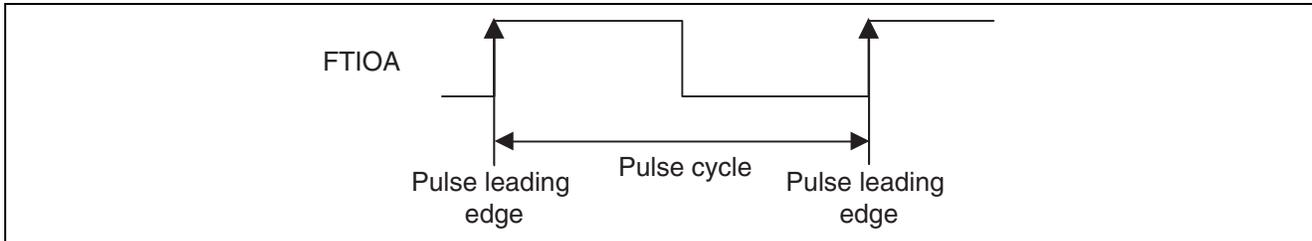
H8/300H Tiny Series H8/36014 CPU

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## 1. Specifications

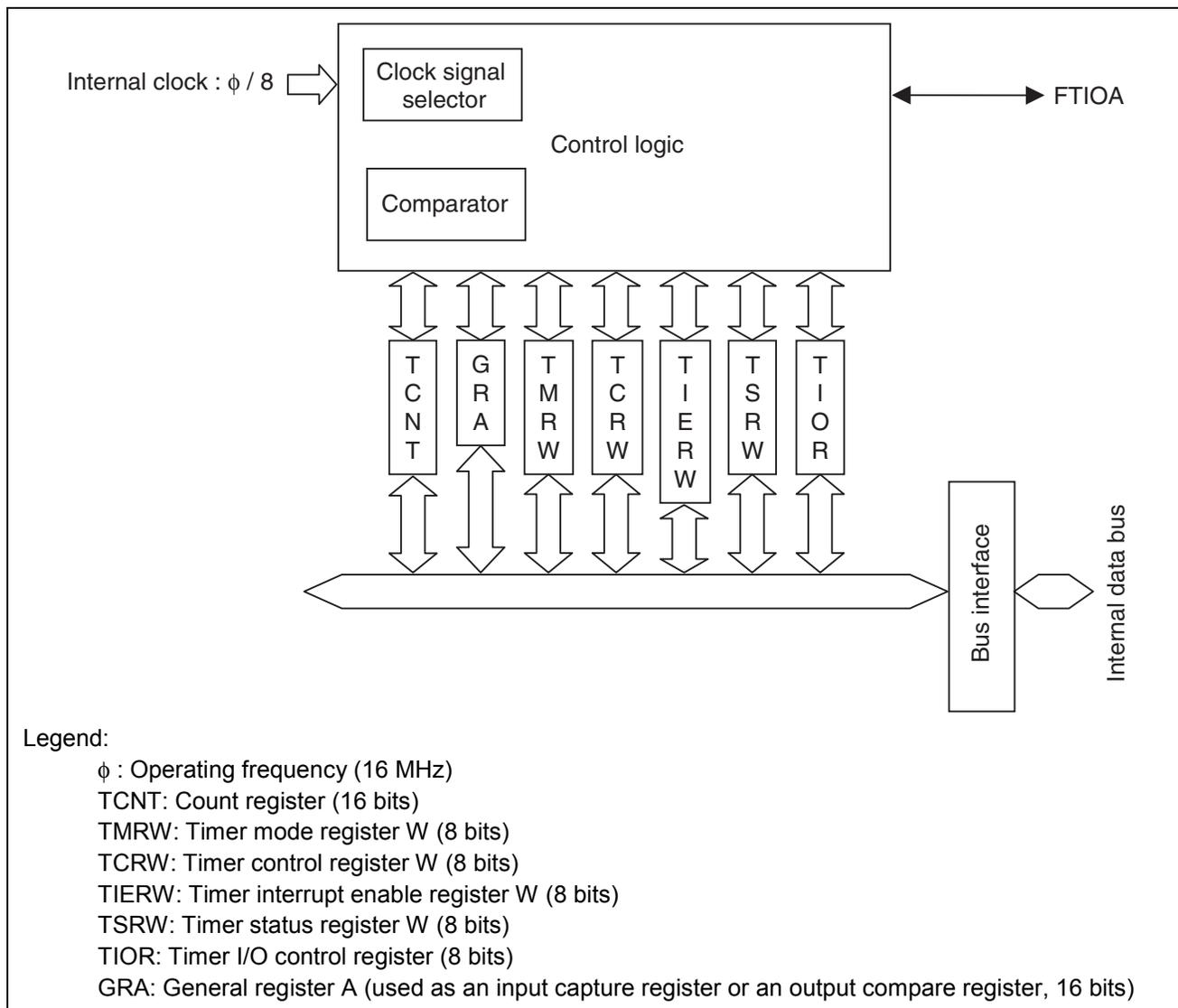
- As shown in Figure 1, you can use input capture timer W to measure the cycle of a pulse entered into the GRA input capture input pin (FTIOA).
- Input capture timer W measures the time between the leading edges of two pulses and stores it in RAM. You can determine the cycle of a pulse using the measured time.
- Since it may take some time before the leading edge of the first target pulse occurs after input capture timer W starts measurement, the measurable maximum pulse cycle changes between 32.768 and 65.535 ms. The variance is  $\pm 0.5 \mu\text{s}$ .



**Figure 1 Measuring the Input Pulse Cycle**

## 2. Description of Functions

- This document describes how to measure the cycle of a pulse entered into the input capture input pin (FTIOA) using input capture timer W. Figure 2 shows the block diagram of input capture timer W. Read the following for details about the items in the block diagram.
  - Timer mode register W (TMRW)  
Starts or stops TCNT.
  - Timer control register W (TCRW)  
Selects an input clock signal for TCNT. In this document, the input clock signal is set to  $\phi / 8$ .
  - Timer interrupt enable register W (TIERW)  
Permits or prohibits interrupt requests. In this document, TIERW permits interrupt requests raised by the OVF and IMFA flags of TSRW and prohibits other interrupts.
  - Timer status register W (TSRW)  
Shows the status of timer W. In this document, when TCNT overflows from H'FFFF to H'0000, TSRW sets the OVF flag to 1. When GRA functions as an input capture register and the input capture signal transfers the value of TCNT to GRA, TSRW sets the IMFA flag to 1.
  - Timer I/O control register 0 (TIOR0)  
Controls GRA. In this document, when GRA is used as an input capture register and the FTIOA pin is set to 1, the value of TCNT is transferred to GRA.
  - Count register (TCNT)  
A 16-bit register that is incremented and can be read and written. The register is incremented by the internal or external clock signal entered. In this document, the input clock signal is set to  $\phi / 8$  and the register is incremented at the rising edge of a clock signal.
  - General register A (GRA)  
A 16-bit register that can be read and written. In this document, when GRA is used as an input capture register and the FTIOA pin is set to 1, the value of TCNT is transferred to GRA.
  - Input capture/output compare A pin (FTIOA)  
Set as the input capture input pin and transfers the value of TCNT to GRA when this pin is set to 1.
  - Input pulse cycle
    - = (Value of TCNT stored in prdhl)  $\times$  (TCNT input clock signal cycle)
    - = (Value of TCNT stored in prdhl)  $\times$  (1 / ( $\phi$  / PSS))
    - = (Value of TCNT stored in prdhl)  $\times$  (1 / (16 MHz / 8))
    - = (Value of TCNT stored in prdhl)  $\times$  0.5  $\mu$ s



**Figure 2 Block Diagram of Timer W**

- Table 1 shows the function of each item described in this document. Assign the function to each item as shown in Table 1 to measure the pulse cycle.

**Table 1 Assignment of Functions**

Item	Function
TMRW	Starts or stops TCNT.
TCRW	Sets the input clock signal for TCNT to $\phi / 8$ .
TIERW	Permits the interrupt requests enabled by OVF and IMFA flags of TSRW.
TSRW	Sets the applicable flag when GRA is used as an input capture register or when TCNT overflows.
TIOR0	Uses GRA as an input capture register and transfers the value of TCNT to GRA when the FTIOA pin is set to 1.
TCNT	A 16-bit register that counts up at a rising edge of $\phi / 8$
GRA	Receives the value of TCNT when the FTIOA pin is set to 1.

### 3. Description of Operation

- The details about the operation are described here. Figure 3 shows the operation when no overflow occurs between the leading edge of the first pulse and the leading edge of the second pulse. Figure 4 shows the operation when an overflow occurs. The pulse cycle is measured by the hardware processing and software processing described in Figure 3 and Figure 4.

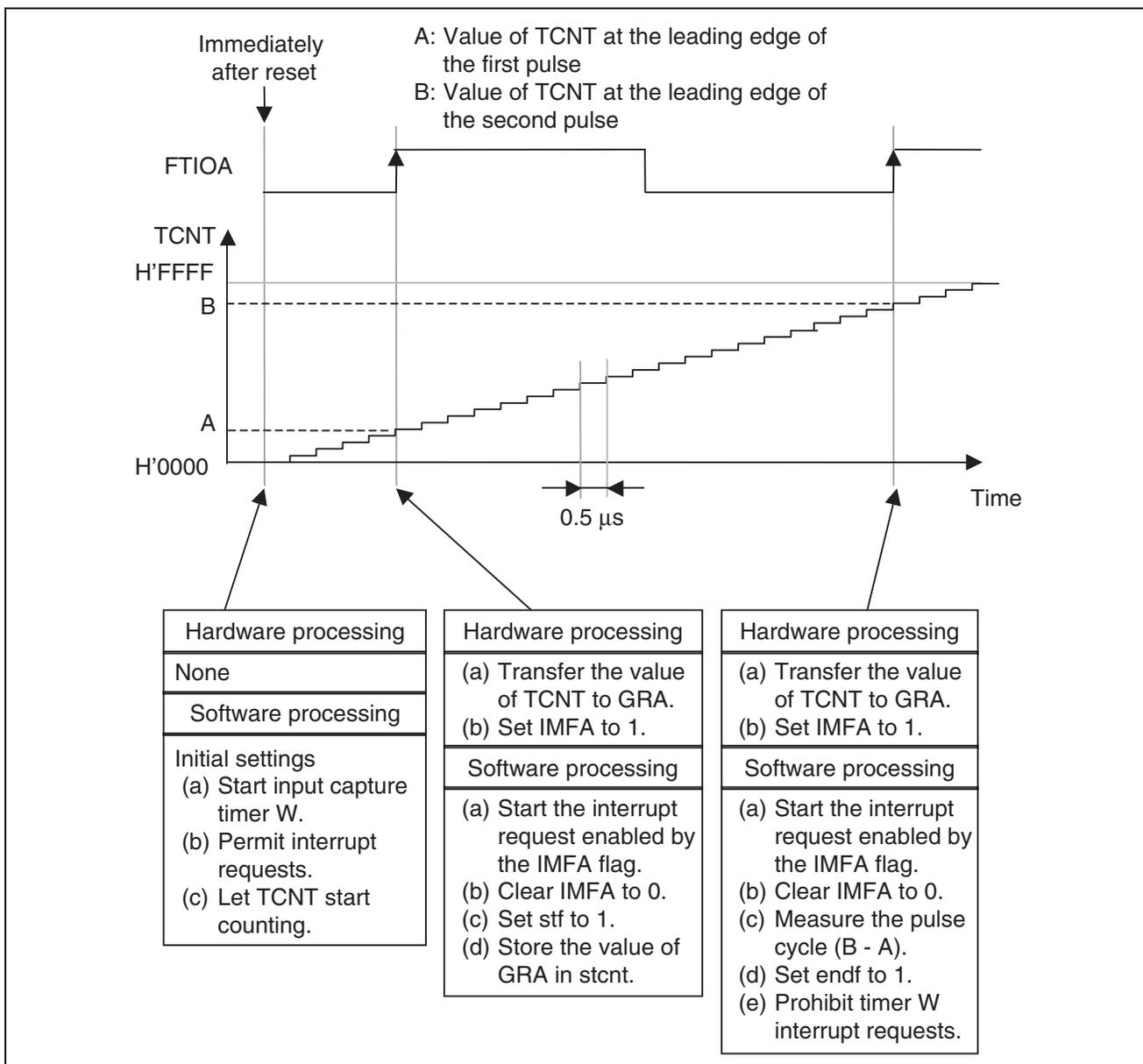


Figure 3 Operation 1

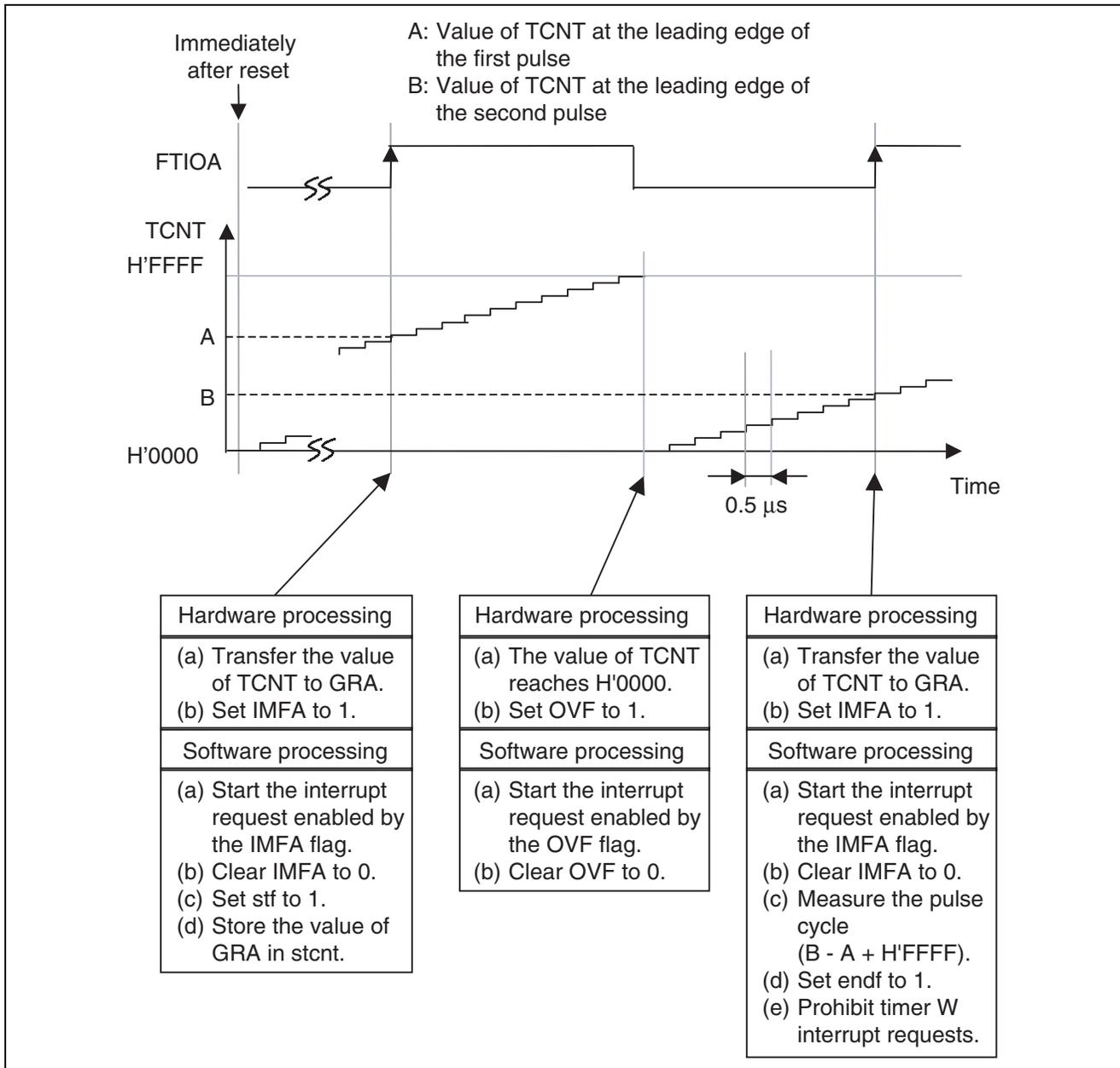


Figure 4 Operation 2

## 4. Description of Software

### 4.1 About the Modules

- Table 2 lists the modules used in this document.

**Table 2 Modules**

Module name	Label	Function
Main routine	main	Starts input capture timer W, lets TCNT start counting, and generates interrupts.
Timer W interrupt routine	tw0int	Controls the output of interrupt requests from timer W, stores the measured pulse cycle in RAM, and clears the OVF and IMFA flags.

### 4.2 About the Arguments

- No arguments are used in this document.

### 4.3 About the Internal Registers Used

- The following internal registers are used in this document.

— TMRW (timer mode register W) address: H'FF80

Bit	Bit name	Set value	R/W	Function
7	CTS	0	R/W	Determines whether to allow TCNT to start counting. CTS = 0: TCNT stops counting. CTS = 1: TCNT starts counting.

— TCRW (timer control register W) address: H'FF81

Bit	Bit name	Set value	R/W	Function
6	CKS2	0	R/W	Selects the input clock signal for TCNT.
5	CKS1	1	R/W	TCNT counts up when it receives internal clock signal $\phi / 8$ .
4	CKS0	1	R/W	

— TIERW (timer interrupt enable register W) address: H'FF82

Bit	Bit name	Set value	R/W	Function
7	OVIE	1	R/W	Permits or prohibits the output of interrupt requests when TCNT overflows. OVIE = 0: Prohibits interrupt requests using the OVF flag of TSRW. OVIE = 1: Permits interrupt requests using the OVF flag of TSRW.
0	IMIEA	1	R/W	Permits or prohibits the output of interrupt requests when GRA is used as an input capture register. IMIEA = 0: Prohibits interrupt requests using the IMFA flag of TSRW. IMIEA = 1: Permits interrupt requests using the IMFA flag of TSRW.

— TSRW (timer status register W) address: H'FF83

Bit	Bit name	Set value	R/W	Function
7	OVF	0	R/W	Flag for indicating whether an overflow has occurred OVF = 0: TCNT has not overflowed. OVF = 1: TCNT has overflowed.
0	IMFA	0	R/W	Indicates whether the value of TCNT is transferred to GRA using the input capture signal when GRA works as an input capture register. IMFA = 0: The value of TCNT is not transferred to GRA. IMFA = 1: The value of TCNT is transferred to GRA.

— TIOR0 (timer I/O control register 0) address: H'FF84

Bit	Bit name	Set value	R/W	Function
2	IOA2	1	R/W	Controls I/O. Sets the function of GRA. GRA = 0: GRA functions as an output compare register. GRA = 1: GRA functions as an input capture register.
1	IOA1	0	R/W	Controls I/O.
0	IOA0	0	R/W	When IOA2 = 1 00: The value of TCNT is transferred to GRA when the FTIOA pin is set to 1. 01: The value of TCNT is transferred to GRA when the FTIOA pin is set to 0. 1X: The value of TCNT is transferred to GRA when the FTIOA pin is set to 1 or 0.

X: Can be any.

- TCNT (count register) address: H'FF86  
 Function: A 16-bit register that counts up at a rising edge of  $\phi / 8$ .  
 Set value: H'0000
  
- GRA (general register A) address: H'FF88  
 Function: Receives the value of TCNT when the FTIOA pin is set to 1 when GRA functions as an input capture register.  
 Set value: -

#### 4.4 About RAM

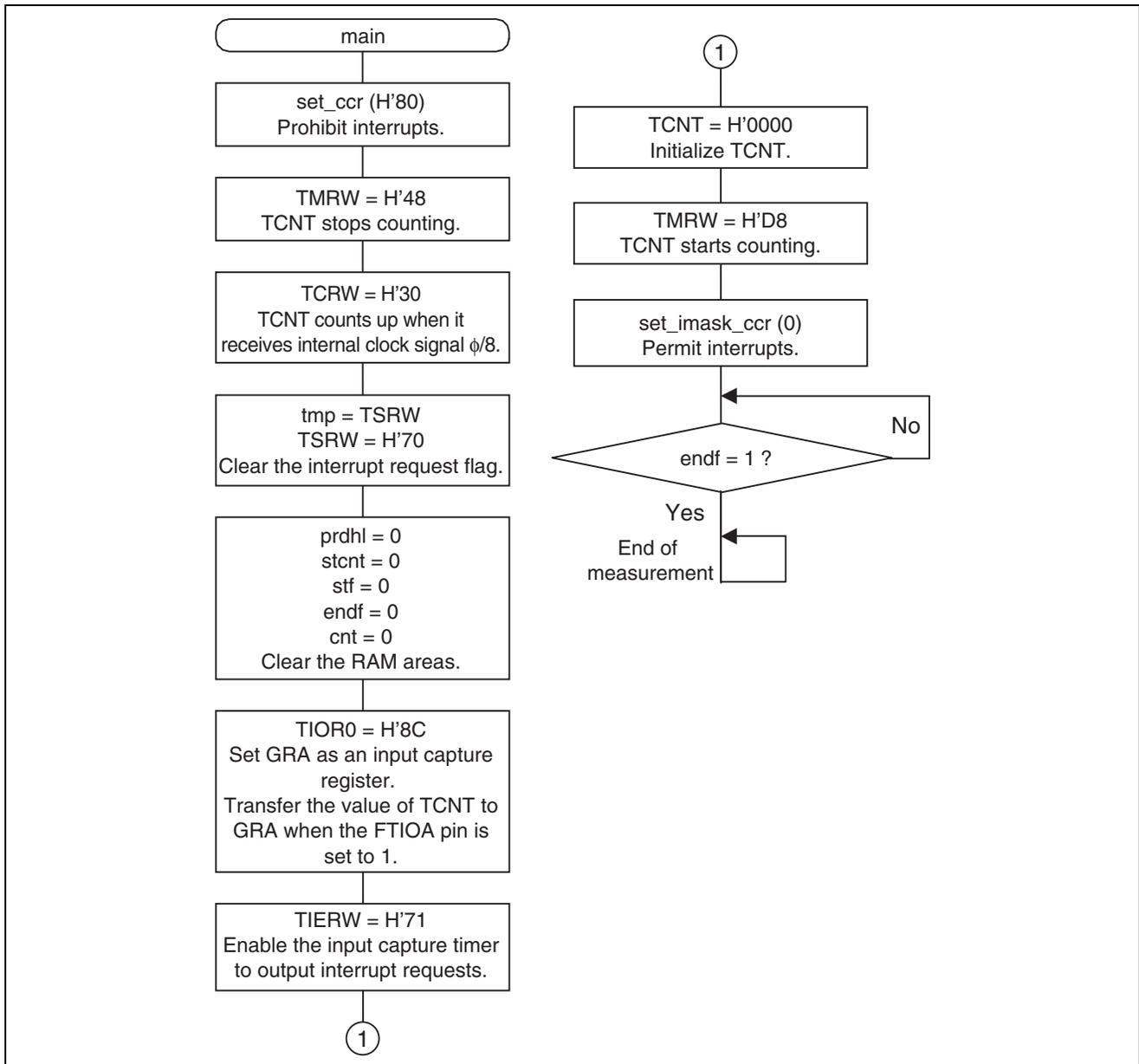
- Table 3 shows how RAM is used in this document.

**Table 3 RAM Areas to be Used**

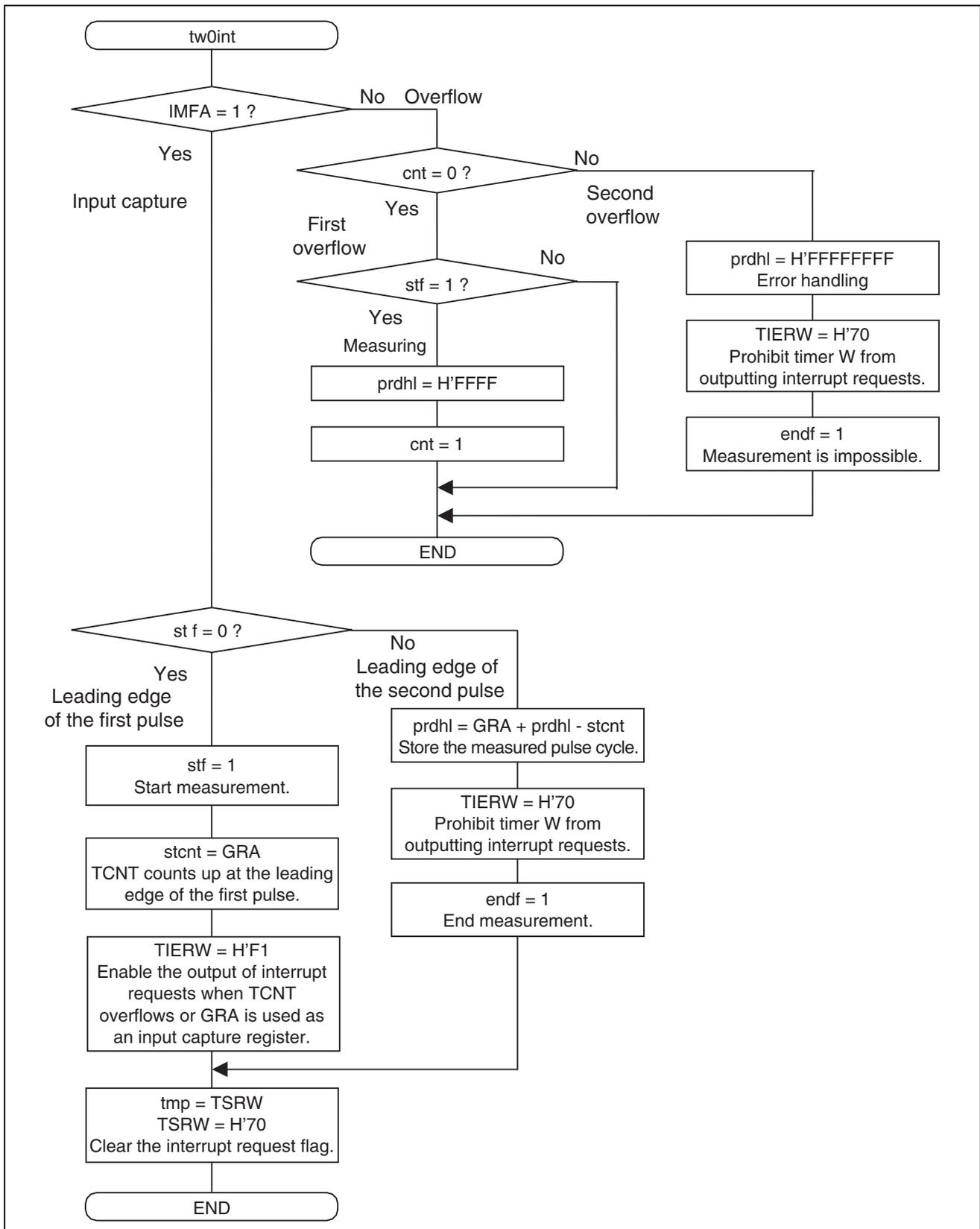
RAM area name	Description	Size of memory used	Used by:
prdhl	Stores the measured pulse cycle.	4 bytes	Main routine Timer W interrupt routine
stcnt	Stores the count of TCNT at the beginning of measurement.	2 bytes	Main routine Timer W interrupt routine
stf	stf = 0: The input capture timer has not output an interrupt request. stf = 1: The leading edge of the first pulse is detected. Measurement starts.	1 byte	Main routine Timer W interrupt routine
endf	endf = 0: The leading edge of the second pulse is not detected. endf = 1: The leading edge of the second pulse is detected or more than one overflows occurred when stf was 1. Measurement ends.	1 byte	Main routine Timer W interrupt routine
cnt	Set to 1 if an overflow occurs when stf = 1.	1 byte	Main routine Timer W interrupt routine

5. Flowchart

5.1 Main Routine



5.2 Timer W Interrupt Routine



- Link addresses

<b>Section name</b>	<b>Address</b>
CV1	H'0000
CV2	H'002A
P	H'0100
B	H'FB80

### Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Dec.20.03	—	First edition issued

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