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APPLICATION NOTE

H8/300H Tiny Series

Measuring Voltage

Introduction

An op-amp is connected to the analog input pin, and the voltage measurement result (units: volts) is displayed on 7-segment LEDs.

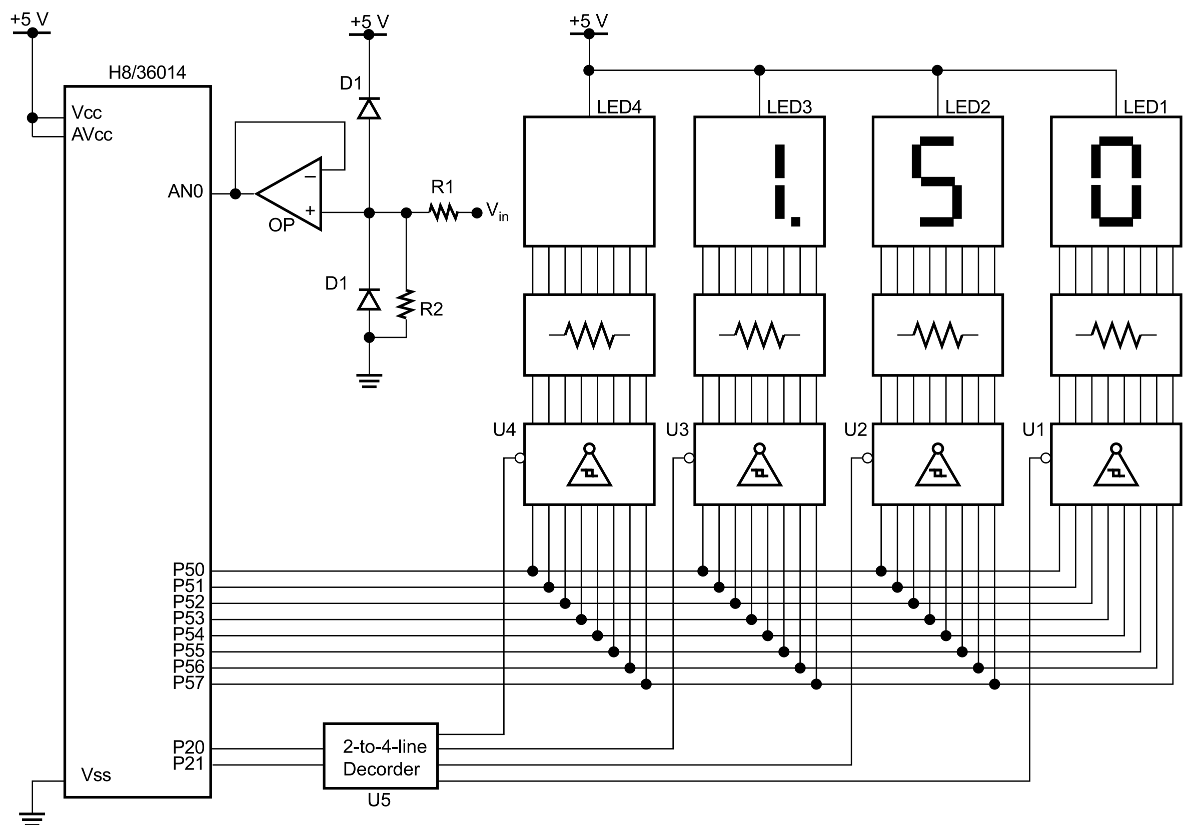
Target Device

H8/36014

Contents

1. Specifications

1. Figure 1.1 shows the hardware configuration of DC voltage measurement. As shown in the figure, the op-amp is connected to the analog input pin 0 (pin AN0).
2. A/D conversion of the AN0 pin input is performed, and the A/D conversion result is displayed on seven-segment LEDs connected to an I/O port.
3. The seven-segment LED displays show the 10-bit data of the A/D conversion result in decimal form.
4. The A/D conversion is performed every 0.49152 seconds.



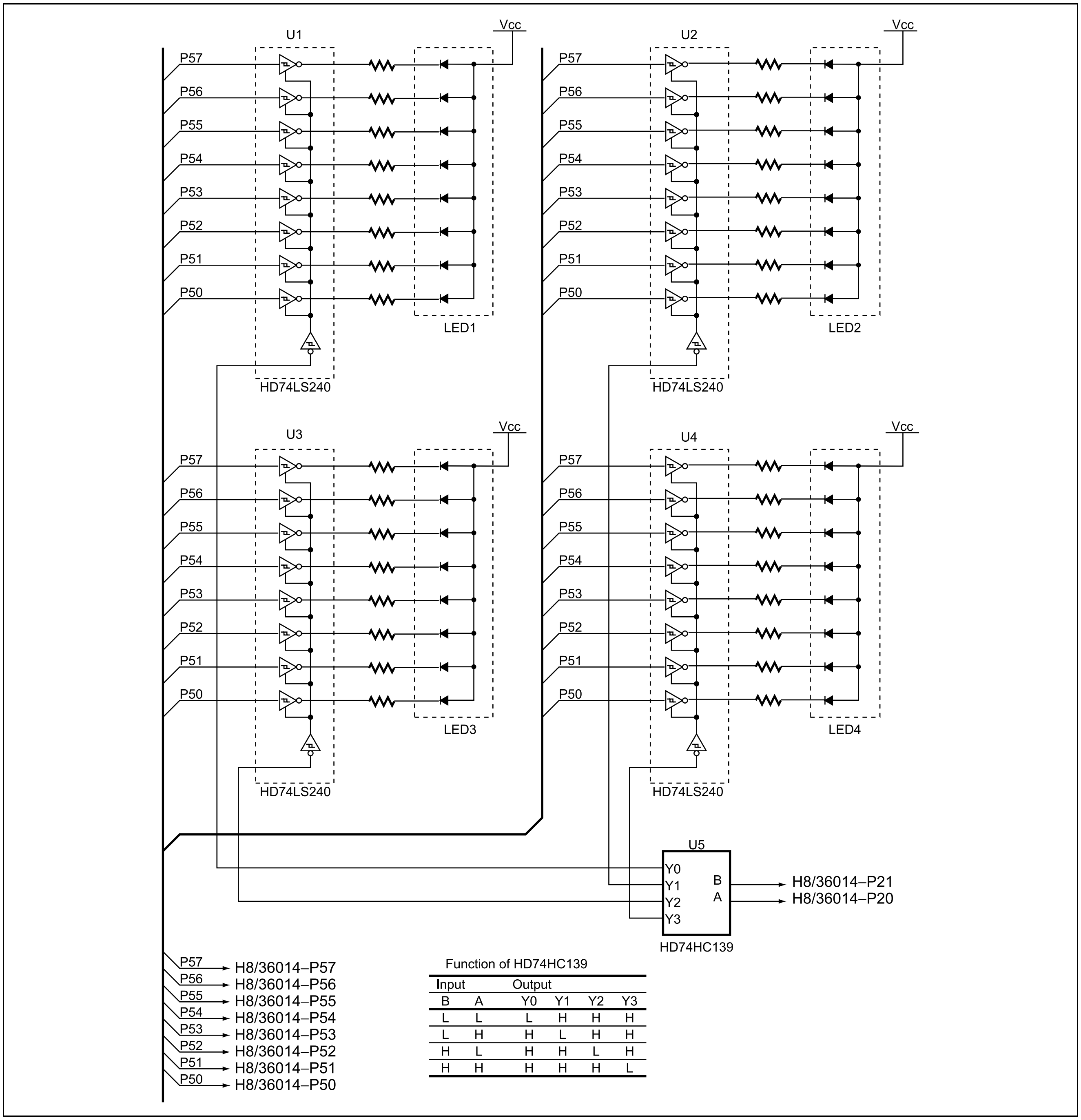
[Legend]

OP:	Op-amp (TLV2451CP, TI)
D1:	Switching diode (1SS133, ROHM)
R1 to R2:	Resistance R2 >> R1 (reference: R1 = 100 kΩ, R2 = 470 kΩ)
LED1 to LED4:	Common-anode seven-segment LEDs
U1 to U4:	3-state output inverter driver (HD74LS240)
U5:	2-to-4-line decoder (HD74HC139)

Figure 1.1 Hardware Configuration

5. In this sample task, the H8/36014 operating voltage (Vcc) and analog power supply voltage (AVcc) are 5.0 V, and the OSC clock frequency is 16 MHz.
6. The op-amp used in this task example is a C-MOS type rail-to-rail (also called full-swing, depending on the manufacturer) op-amp. In conventional op-amps, the output voltage range was narrowed by the voltage loss of the op-amp itself, but in a rail-to-rail op-amp, an output amplitude equal to the power supply voltage is obtained.
7. The operation of this task example is as follows.
   A. The voltage measurement range is 0 V to 5.0 V (Vcc). When measuring 1.5 V, the LED display is "1.50".
   B. By adding a circuit to divide the voltage being measured, voltages greater than the power supply voltage can also be measured.

8. In this sample task, in order to display results on seven-segment LEDs, the port output is input to three-state output inverter drivers (HD74LS240), and the driver outputs are connected to the cathodes of the seven-segment LEDs. The port used for display on four seven-segment LEDs is connected to all of the seven-segment LEDs; switching of the display on the seven-segment LEDs is controlled by the enable pin of the three-state inverter drivers. A 2-to-4-line decoder (HD74HC139) is used to generate signals for switching the seven-segment LED display, and is controlled by two port outputs. Figure 1.2 shows the method of control of the seven-segment LEDs.



Input		Output			
B	A	Y0	Y1	Y2	Y3
L	L	L	H	H	H
L	H	H	L	H	H
H	L	H	H	L	H
H	H	H	H	H	L

Figure 1.2 Method of Control of Seven-Segment LEDs

9. In this sample task, the A/D conversion result is displayed on the seven-segment LEDs in decimal form (unit: V). Figure 1.3 shows the method used to display the A/D conversion result on the LEDs.

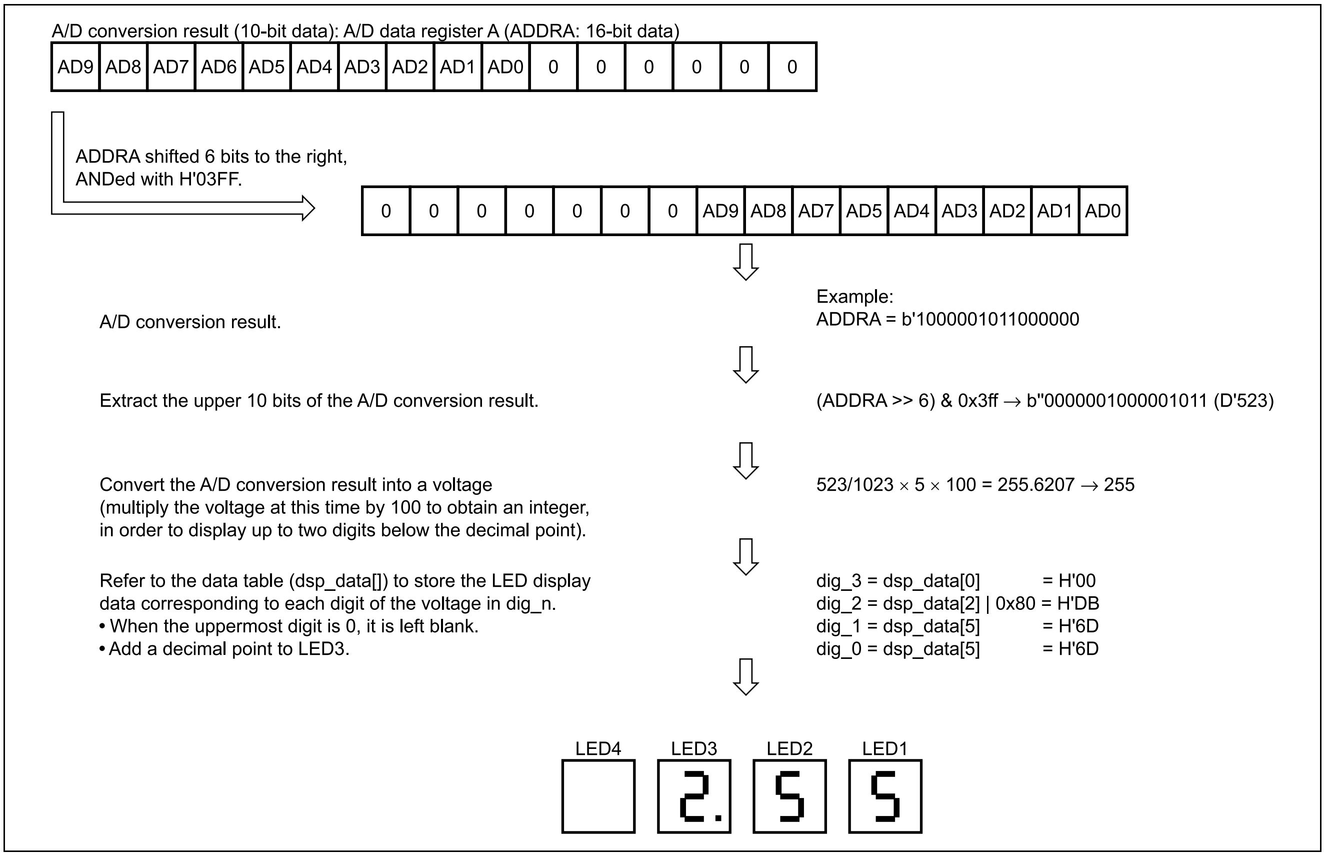


Figure 1.3 How A/D Conversion Results are Displayed on the LEDs

2. Description of Functions

1. Figure 2.1 is a block diagram of the H8/36014 functions used in this sample task; table 2.1 shows function allocations.

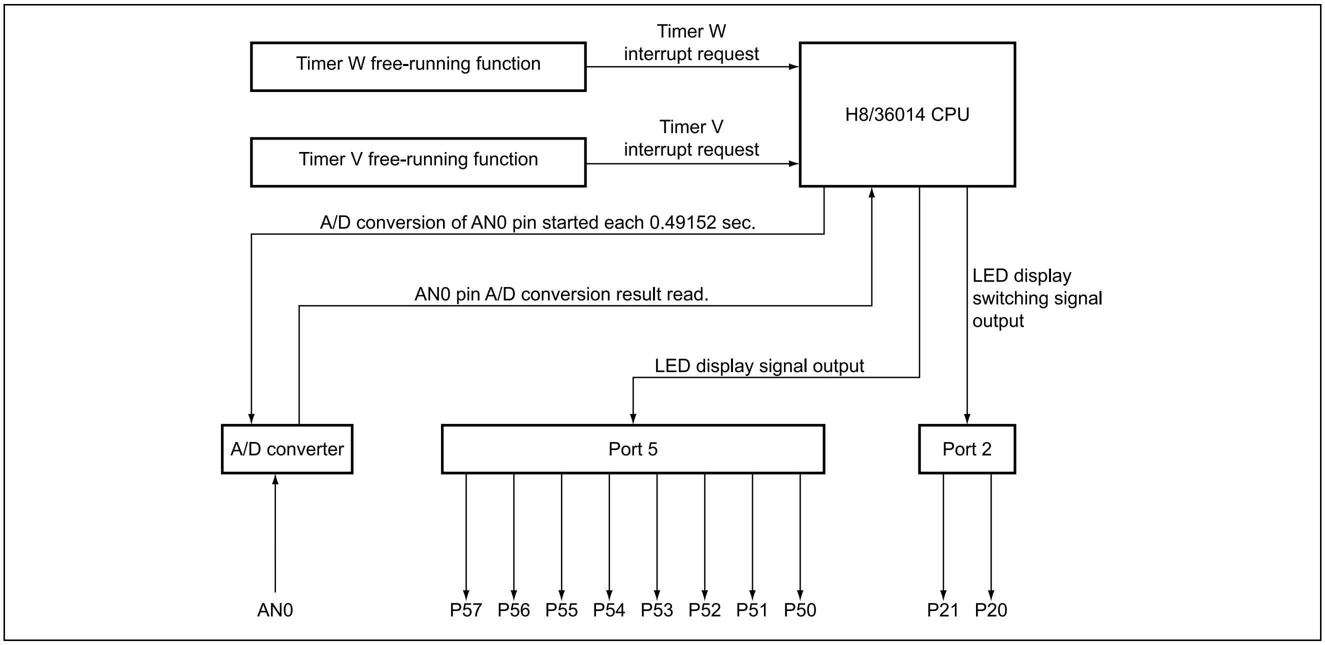


Figure 2.1 Block Diagram of Functions Used

Table 2.1 Function Allocation

Function Used	Function Allocation
Timer W	The timer W free running function is used to perform A/D conversion of the analog input pin 0 (AN0) signal. The A/D conversion period is measured by the timer W overflow period of 32.768 ms.
Timer V	The timer V free running function is used to control switching of the 7-segment LED display. Dynamic lighting is performed by light the four 7-segment LEDs in order at every 2.048 ms Timer V overflow period.
A/D converter	The output voltage from the op-amp connected to the A/D converter analog input pin 0 (AN0) for the voltage follower is A/D converted.
Port 2	Display on the four 7-segment LEDs is switched by the port 2 output pins P20 and P21. The P20 and P21 output pins are connected to I/O pins of a 2-to-4-line decoder.
Port 5	Results are displayed on the 7-segment LEDs by output from the port 5 output pins P50 to P57. The 10-bit data which is the A/D conversion result at pin AN0 is converted into a 4-digit decimal display data for output to the LEDs.

2. A diagram of the connection of the seven-segment LEDs used is shown in figure 2.2. As shown in the figure, by outputting "high" from port 2.2, the corresponding LED segments are lit. The relationship between the port 5 outputs and the LED display data is shown in table 2.2.

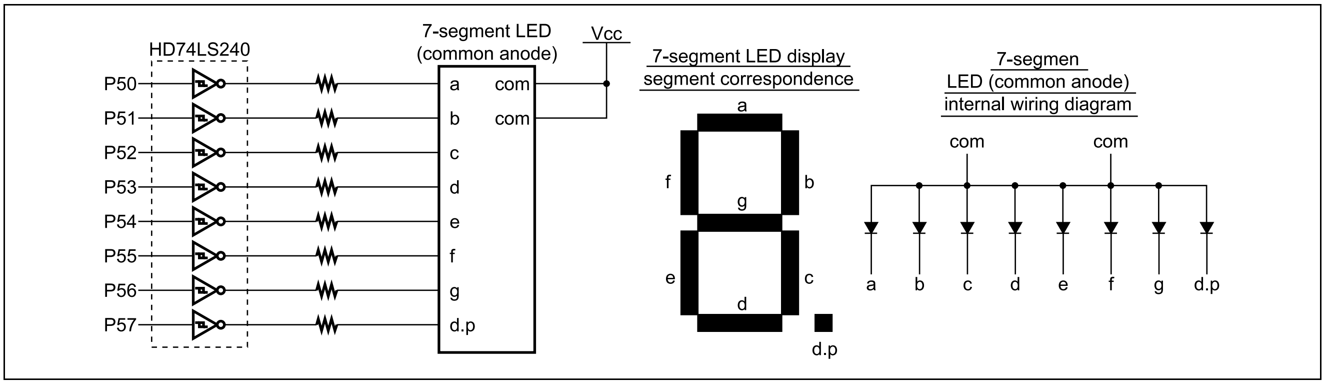
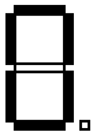
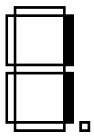
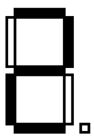
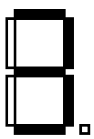
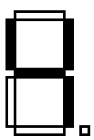
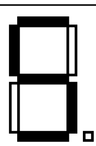
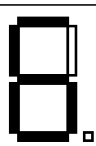
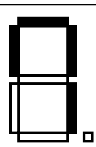
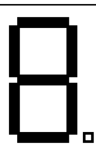
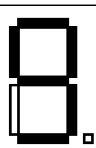
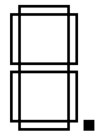


Figure 2.2 7-Segment LED Connection Diagram and Internal Wiring

Table 2.2 Relation between Port 5 Outputs and 7-Segment LED Display Data

LED Display	Port 5 Output Data							
	P57	P56	P55	P54	P53	P52	P51	P50
	0	0	1	1	1	1	1	1
	0	0	0	0	0	1	1	0
	0	1	0	1	1	0	1	1
	0	1	0	0	1	1	1	1
	0	1	1	0	0	1	1	0
	0	1	1	0	1	1	0	1
	0	1	1	1	1	1	0	1
	0	0	1	0	0	1	1	1
	0	1	1	1	1	1	1	1
	0	1	1	0	1	1	1	1

LED Display	Port 5 Output Data							
	P57	P56	P55	P54	P53	P52	P51	P50
	1	0	0	0	0	0	0	0

Note: The first integer digit is ANDed with a decimal point

3. Principles of Operation

1. Figure 3.1 shows the principle of operation when using the timer W to perform A/D conversion of the AN0 pin output. As shown in figure 3.1, in this sample task the A/D conversion period (0.49152 s) is measured using the timer W overflow flag in the tmrw routine, without using the A/D conversion interrupt, to judge the end of A/D conversion.

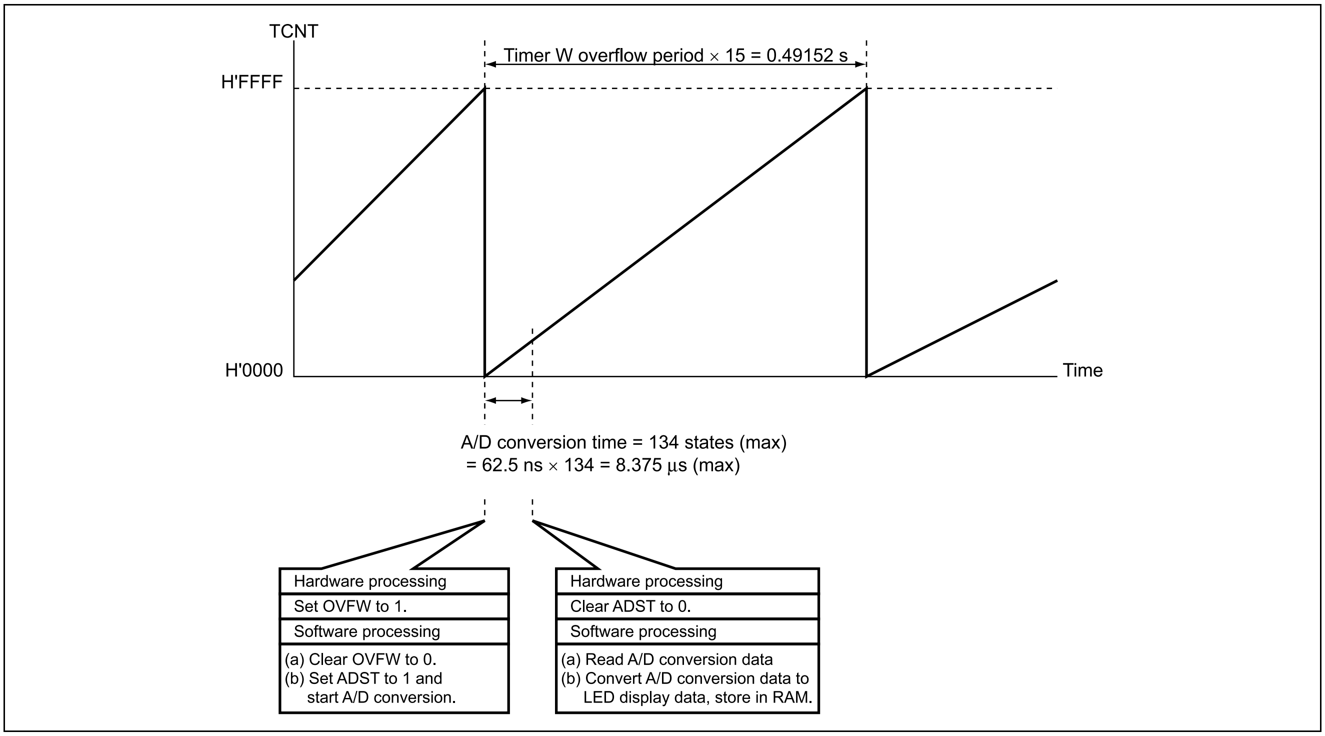


Figure 3.1 Principle of Operation of A/D Conversion of the AN0 Pin Output using Timer W

2. The principle of operation of the seven-segment LED display control is as follows. Figure 3.2 describes the operation for the case in which "2.55" is displayed on LED4 through LED1. As shown in figure 3.2, by displaying the data in order on LED1 through LED4 at each timer V overflow period, data is displayed dynamically on the seven-segment LEDs.

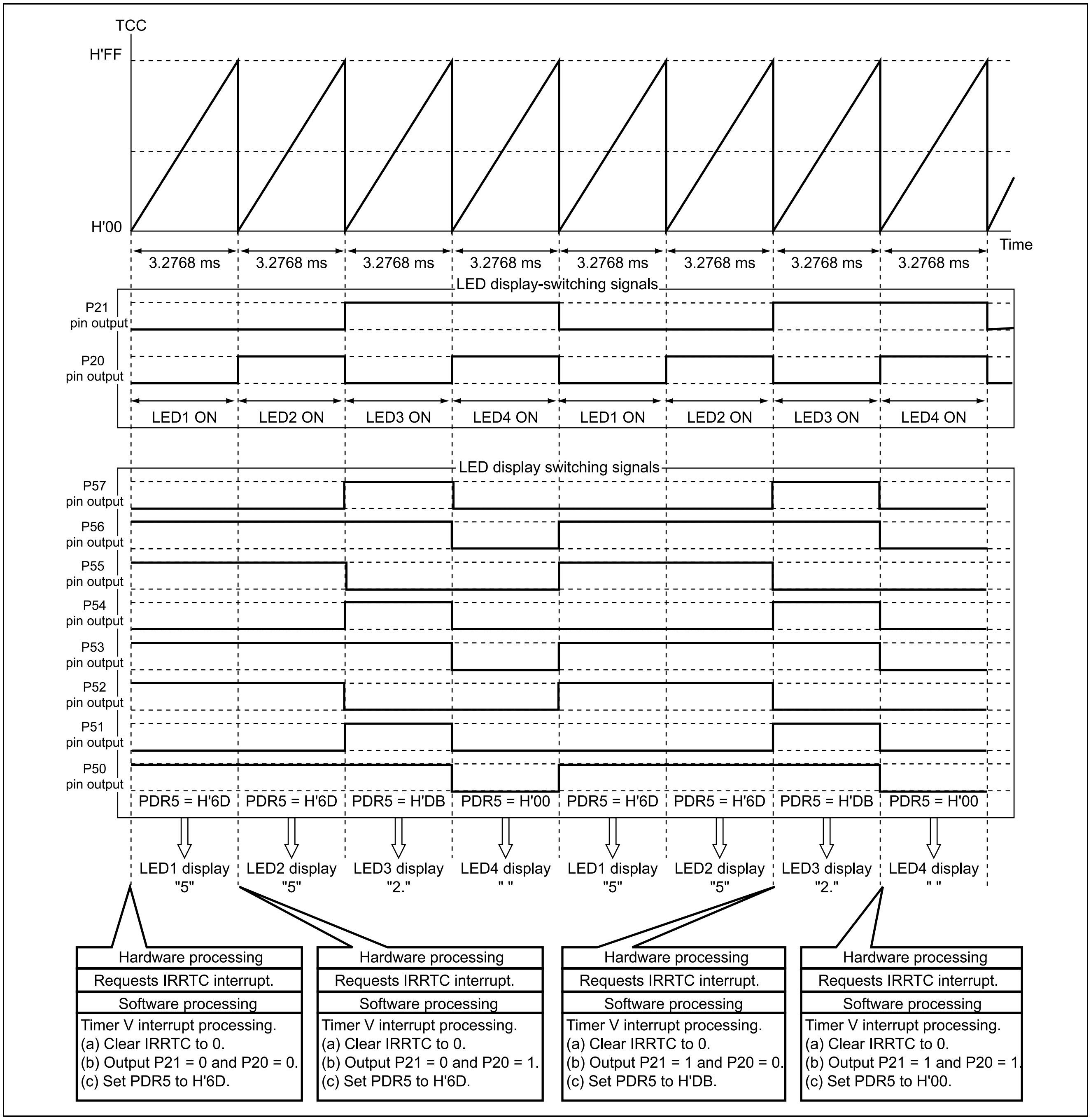


Figure 3.2 Principle of Operation of 7-Segment LED Display Control

4. Description of Software

4.1 Description of Modules

Table 4.1 describes the modules used in this sample task.

Table 4.1 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets initial values, enables interrupts
Timer W interrupt processing routine	tmrw	Clears interrupt flag, converts A/D conversion data into LED display data, and stores in RAM
Timer V interrupt processing routine	tmrv	Clears interrupt flag and controls LED display data output and LED display switching

4.2 Description of arguments

This sample task does not use arguments.

4.3 Description of Internal Registers

The internal registers used in this sample task are described in table 4.2.

Table 4.2 Description of Internal Registers

Register Name		Function	Address	Setting
TCRV0		Timer control register V0: Selects TCNTV input clock, sets TCNTV clear conditions, controls interrupt requests	H'FFA0	H'03 (initial setting)
	CMIEB	Compare-match interrupt enable B: when CMIEB = 0, disables interrupt requests by CMFB in TCSRV	Bit 7	0
	CMIEA	Compare-match interrupt enable A: when CMIEA = 0, disables interrupt requests by CMFA in TCSRV	Bit 6	0
	OVIE	Timer overflow interrupt enable: when OVIE = 0, disables interrupt requests by OVF in TCSRV, when OVIE = 1, enables interrupt requests by OVF in TCSRV	Bit 5	0/1
	CCLR1	Counter clear 1, 0: Sets conditions to clear TCNTV	Bit 4	0
	CCLR0	When CCLR1=0 and CCLR0=0, TCNTV clearing is disabled	Bit 3	0
	CKS2	Clock select 2 to 0: Combined with ICKS0 in TCRV1, selects clock for input to TCNTV and count conditions	Bit 2	0
	CKS1		Bit 1	1
	CKS0	When CKS2=0, CKS1=1, CKS0=1, and ICKS0=1, TCNTV counts on the falling edge of the internal clock ϕ/128	Bit 0	1

Register Name		Function	Address	Setting
TCSRV		Timer control/status register V: Displays status flag, controls output of compare-match	H'FFA1	H'10
	CMFB	Compare-match flag B: Set to 1 when the values of TCNTV and TCORB match	Bit 7	0
	CMFA	Compare-match flag A: Set to 1 when the values of TCNTV and TCORA match	Bit 6	0
	OVF	Timer overflow flag: When the TCNTV value overflows, OVF is set to 1 In the OVF=1 state, when 0 is written to OVF after reading OVF, OVF is cleared to 0	Bit 5	0
	OS3	Output select 3, 2: Sets the output level of the TMOV pin for the output of compare-match B When set to OS3 = 0 and OS2 = 0, no change occurs	Bit 3	0
	OS2		Bit 2	0
	OS1	Output select 1, 0: Sets the output level of the TMOV pin for the output of compare-match A When set to OS1 = 0 and OS0 = 0, no change occurs	Bit 1	0
	OS0		Bit 0	0
TCRV1		Timer control register V1: Selects TRGV pin edge select, TRGV input enable, TCNTV input clock	H'FFA5	H'E3
	TVEG1	TRGV input edge select 1, 0: Selects input edge of TRGV pin When set to TREG1=0, TREG0=0, disables trigger input from TRGV pin	Bit 4	0
	TVEG0		Bit 3	0
	TRGE	TRGV input enable: Enables/disables TCNTV count-up by edge input selected using TVEG1 and TVEG0 When set to TREG=0, disables start of TCNTV count-up due to input to TRGV pin and halt of TCNTV count-up when TCNTV is cleared due to a compare-match	Bit 2	0
	ICKS0	Internal clock select 0: Combined with CKS2 to CKS0 of TCRV0, selects clock for input to TCNTV and count conditions; when set to CKS2=0, CKS1=1, CKS0=1 and ICKS0=1, TCNTV counts on the falling edge of the internal clock ϕ/128	Bit 0	1
TMRW		Timer mode register W: Selects general register functions and timer output mode	H'FF80	H'80
	CTS	Counter start: When CTS=1, indicates TCNT has started counting When CTS=0, indicates TCNT has stopped counting	Bit 7	1
TCRW		Timer control register W: Selects counter clock Sets counter clear conditions and timer output level	H'FF81	H'30
	CKS2	Clock select: When CKS2 = 0, CKS1 = 1 and CKS0 = 1, sets TCNT input clock to system clock divided by 8	Bit 6	0
	CKS1		Bit 5	1
	CKS0		Bit 4	1
TIERW		Timer interrupt enable register W: controls timer W interrupt requests	H'FF82	H'00 (initial setting)
	OVIE	Timer overflow interrupt enable: when OVIE = 0, disables interrupt requests by OVF When OVIE = 1, enables interrupt requests by OVF	Bit 7	0/1

Register Name		Function	Address	Setting
TSRW		Indicates interrupt request status	H'FF83	H'00
	OVF	Timer overflow: When OVF=0, indicates TCNT has not overflowed When OVF=1, indicates that TCNT has overflowed	Bit 7	0
TCNT		Timer counter: 16-bit count-up counter which takes as input the system clock frequency-divided by 8	H'FF86	H'00
ADCSR		A/D control/status register: Consists of A/D converter control bits and conversion status bits	H'FFB8	H'00 (initial setting)
	ADF	A/D end flag: Set to 1 when A/D conversion ends in single mode After reading in the ADF=1 state, is cleared to 0 by writing 0	Bit 7	0
	ADIE	A/D interrupt enable: When 0, disables A/D conversion end interrupt requests by the ADF	Bit 6	0
	ADST	A/D start: Setting this to 1 starts A/D conversion Automatically cleared to 0 when A/D conversion ends in single mode	Bit 5	0/1
	SCAN	Scan mode: When 0, A/D conversion mode is single mode	Bit 4	0
	CKS	Clock select: When 0, A/D conversion time =134 states (max)	Bit 3	0
	CH2	Channel select: Selects the analog input channel; when CH2=0, CH1=0 and CH0=0 (SCAN=0), input channel is AN1	Bit 2	0
	CH1		Bit 1	0
	CH0		Bit 0	0
ADCR		A/D control register: Enables A/D conversion start by an external trigger	H'FFB9	H'7E
	TRGE	Trigger enable: When 0, disables the start of A/D conversion by edge input to the external trigger pin (ADTRG)	Bit 7	0
ADDRA		A/D data register A: Stores the AN0 A/D conversion result	H'FFB0	—
PCR2		Port control register 2: Selects, for each bit, pin I/O to use as the port 2 general I/O port When PCR2=H'03, pin P22 functions as a general input pin, and pins P21 and P20 function as general output pins	H'FFE5	H'03
PDR2		Port data register 2: General I/O port data register for port 2	H'FFD5	H'F8
PMR5		Port mode register 5: Sets the port 5 pin functions	H'FFE1	H'00
	POF7	P57 pin function switch: When 0, P57 functions as a general I/O port	Bit 7	0
	POF6	P56 pin function switch: When 0, P56 functions as a general I/O port	Bit 6	0
	WKP5	P55/$\overline{\text{WKP5}}$/$\overline{\text{ADTRG}}$ pin function switch: When 0, P55 functions as a general I/O port	Bit 5	0
	WKP4	P54/$\overline{\text{WKP4}}$ pin function switch: When 0, P54 functions as a general I/O port	Bit 4	0
	WKP3	P53/$\overline{\text{WKP3}}$ pin function switch: When 0, P53 functions as a general I/O port	Bit 3	0
	WKP2	P52/$\overline{\text{WKP2}}$ pin function switch: When 0, P52 functions as a general I/O port	Bit 2	0
	WKP1	P51/$\overline{\text{WKP1}}$ pin function switch: When 0, P51 functions as a general I/O port	Bit 1	0
	WKP0	P50/$\overline{\text{WKP0}}$ pin function switch: When 0, P50 functions as a general I/O port	Bit 0	0

Register Name	Function	Address	Setting
PUCR5	Port pull-up control register 5: Controls, for each bit, the pull-up MOS of each port 5 pin set to an input port	H'FFD1	H'00
	When PUCR5=H'00, pull-up MOS for pins P57 to P50 is turned off		
PDR5	Port data register 5: Port 5 general I/O port data register	H'FFD8	H'00
PCR5	Port control register 5: Selects, for each bit, the pin I/O used as a port 5 general I/O port	H'FFE8	H'FF
	When PCR5=H'FF, the pins P57 to P50 function as general output pins		

4.4 Description of RAM

Table 4.3 describes the RAM used in this sample task.

Table 4.3 Description of RAM

Label Name	Function	Address	Used in
dig_0	Store LED1 display data (1 byte)	H'FB88	main, tmrw
dig_1	Store LED2 display data (1 byte)	H'FB89	main, tmrw
dig_2	Store LED3 display data (1 byte)	H'FB8A	main, tmrw
dig_3	Store LED4 display data (1 byte)	H'FB8B	main, tmrw
cnt	8-bit counter to switch LED1 to LED4 display (1 byte)	H'FB8C	main, tmrv
counter_sub	8-bit counter to adjust A/D acquisition interval (1 byte)	H'FB8D	main, tmrw
convdat	Coefficient for voltage conversion $\times$ 100 (4 bytes)	H'FB80	main, tmrw
temp	Temporarily stack area for calculated results (2 bytes)	H'FB84	tmrw
ptr	Pointer to store dig_0 address (2 bytes)	H'FB86	tmrv

4.5 Description of data table

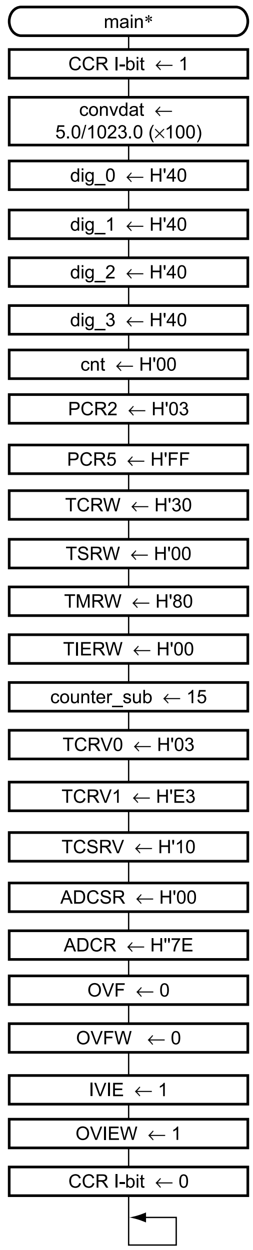
In this sample task, seven-segment LED display data is stored as a one-dimensional data table in ROM. Table 4.4 describes the seven-segment LED display data table (dsp_data).

Table 4.4 Description of 7-Segment LED Display Data Table (dsp_data[])

Array Name	Data	Data Description	Data Size	Address
dsp_data[0]	H'3F	Data output from port 5 to display "0" on an LED	1 byte	H'04CA
dsp_data[1]	H'06	Data output from port 5 to display "1" on an LED	1 byte	H'04CB
dsp_data[2]	H'5B	Data output from port 5 to display "2" on an LED	1 byte	H'04CC
dsp_data[3]	H'4F	Data output from port 5 to display "3" on an LED	1 byte	H'04CD
dsp_data[4]	H'66	Data output from port 5 to display "4" on an LED	1 byte	H'04CE
dsp_data[5]	H'6D	Data output from port 5 to display "5" on an LED	1 byte	H'04CF
dsp_data[6]	H'7D	Data output from port 5 to display "6" on an LED	1 byte	H'04D0
dsp_data[7]	H'27	Data output from port 5 to display "7" on an LED	1 byte	H'04D1
dsp_data[8]	H'7F	Data output from port 5 to display "8" on an LED	1 byte	H'04D2
dsp_data[9]	H'6F	Data output from port 5 to display "9" on an LED	1 byte	H'04D3

5. Flowchart

1. Main routine (main)



Mask interrupt requests by setting the CCR interrupt mask bit (I) to 1.

Store the coefficient for voltage conversion (×100) in convdat.

Initial settings for RAM area
dig_0 = H'40: LED1 initial display data "-"
dig_1 = H'40: LED2 initial display data "-"
dig_2 = H'40: LED3 initial display data "-"
dig_3 = H'40: LED4 initial display data "-"
cnt = H'00: Initial value of LED enable counter = 0

Port 2 initial settings
P20/SCK3: P20 output pin (output data = 0)
P21/RXD: P21 output pin (output data = 0)
P22/TXD: P22 input pin

Port 5 initial settings

P50/$\overline{WKP0}$:	P50 output pin (output data = 0)
P51/$\overline{WKP1}$:	P51 output pin (output data = 0)
P52/$\overline{WKP2}$:	P52 output pin (output data = 0)
P53/$\overline{WKP3}$:	P53 output pin (output data = 0)
P54/$\overline{WKP4}$:	P54 output pin (output data = 0)
P55/$\overline{WKP5}$/$\overline{ADTRG}$:	P55 output pin (output data = 0)
P56:	P56 output pin (output data = 0)
P57:	P57 output pin (output data = 0)

Timer W initial settings
TCNT input clock: Internal clock φ divided by 8
Clear timer overflow (OVF) to "0".
Start timer counter counting operation.
Interrupt requests cannot occur due to the TSRW OVF flag.
8-bit counter_sub initialized to 15.

Timer V initial settings
Operation mode: Free-running operation
TCNTV input clock: Internal clock φ/128
Count condition: Falling edge

A/D converter initial settings
Scan mode: Single mode
Analog input channel: AN0
A/D conversion time: 134 states (max)

Clear the timer overflow flag (OVF) to 0.

Clear the timer overflow flag (OVF) to 0.

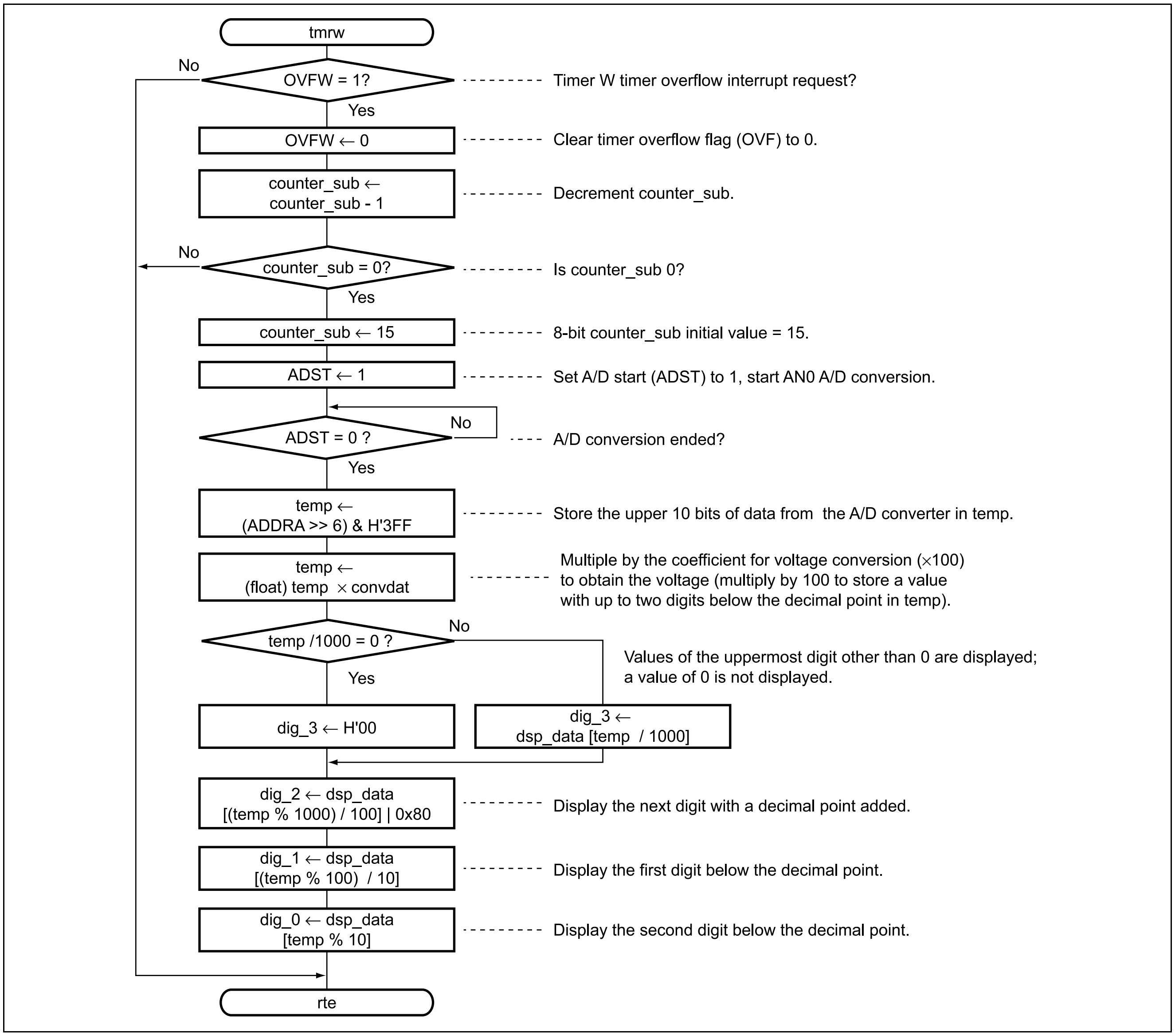
Enable timer V timer overflow interrupt requests.

Enable timer W timer overflow interrupt requests.

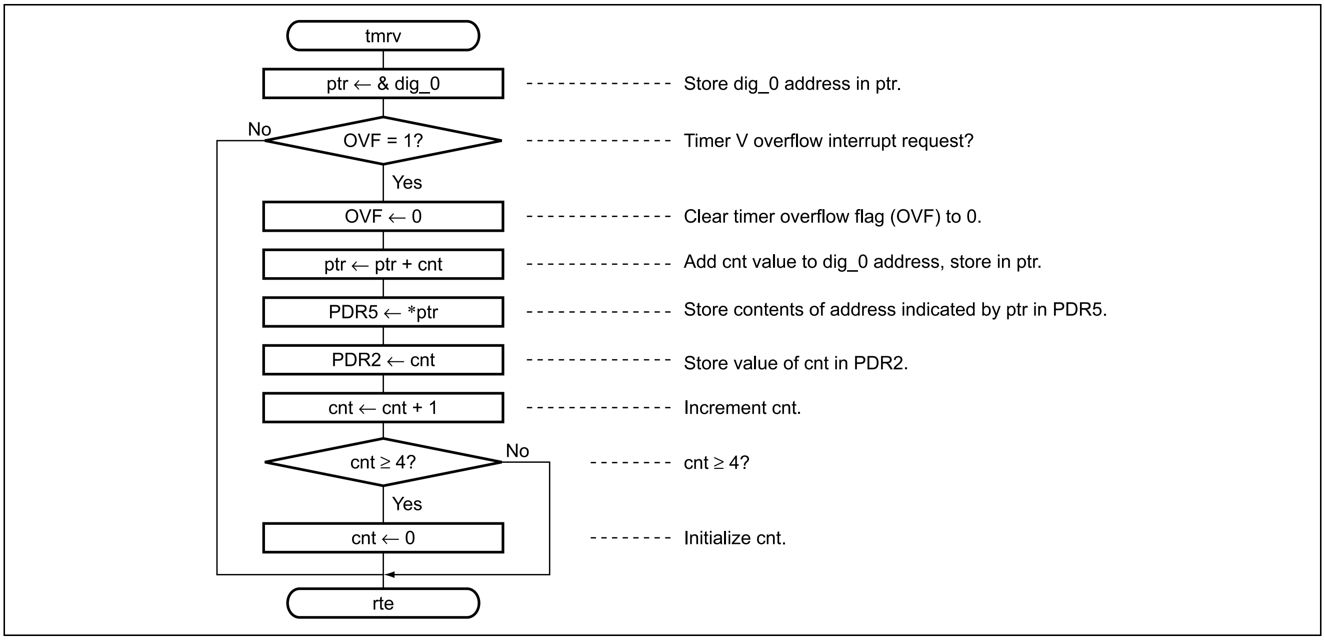
Clear the interrupt mask bit (I) in CCR to 0.

Note: * In this sample task, the stack pointer is specified by INIT.SRC (assembly language).

2. Timer W interrupt processing routine (tmrw)



3. Timer V interrupt processing routine (tmrv)



6. Program Listing

INIT.SRC (program list)

```
     .export   _INIT
     .import   _main
;
     .section  P,CODE
_INIT:
     mov.w     #h'ff80,r7
     ldc.b     #b'10000000,ccr
     jmp  @_main
;
     .end
```

```
/*   H8/300H tiny Series -H8/36014- Application note                                                              */
/*   Application example                                                                                          */
/*   Voltage measurement                                                                                          */

#include <machine.h>

/*   Symbol defnition                                                                                             */
struct BIT {
     unsigned char b7:1;      /* bit 7 */
     unsigned char b6:1;      /* bit 6 */
     unsigned char b5:1;      /* bit 5 */
     unsigned char b4:1;      /* bit 4 */
     unsigned char b3:1;      /* bit 3 */
     unsigned char b2:1;      /* bit 2 */
     unsigned char b1:1;      /* bit 1 */
     unsigned char b0:1;      /* bit 0 */
};

#define PDR2        *(volatile unsigned char *)0xFFD5                /* Port data register 2                  */
#define PCR2        *(volatile unsigned char *)0xFFE5                /* Port control register 2               */

#define PDR5        *(volatile unsigned char *)0xFFD8                /* Port data register 5                  */
#define PCR5        *(volatile unsigned char *)0xFFE8                /* Port control register 5               */

#define TMRW        *(volatile unsigned char *)0xFF80                /* Timer mode register W                 */
#define TCRW        *(volatile unsigned char *)0xFF81                /* Timer control register W              */
#define TCRW_BIT    (*(struct BIT *)0xFF81)                          /* Timer Control Register W              */
#define TIERW       *(volatile unsigned char *)0xFF82                /* Timer interrupt enable register W     */
#define TIERW_BIT   (*(struct BIT *)0xFF82)                          /* Timer Interrupt Enable Register       */
#define OVIEW       TIERW_BIT.b7                                     /* Timer Overflow Interrupt Enable W     */
#define TSRW        *(volatile unsigned char *)0xFF83                /* Timer status register W               */
#define TSRW_BIT    (*(struct BIT *)0xFF83)                          /* Timer Status Register W               */
#define OVFW        TSRW_BIT.b7                                      /* Timer Over flow W                     */

#define TCRV0       *(volatile unsigned char *)0xFFA0                /* Timer control register V0             */
#define TCRV0_BIT   (*(struct BIT *)0xFFA0)
#define OVIE        TCRV0_BIT.b5                                     /* Timer overflow interrupt enable       */
#define TCSRV       *(volatile unsigned char *)0xFFA1                /* Timer control/status register V       */
#define TCSRV_BIT   (*(struct BIT *)0xFFA1)
#define OVF         TCSRV_BIT.b5                                     /* Timer overflow flag                   */
#define TCRV1       *(volatile unsigned char *)0xFFA5                /* Timer control register V1             */
```

```
#define ADCSR       *(volatile unsigned char *)0xFFB8          /* A/D control/status register    */
#define ADCSR_BIT   (*(struct BIT *)0xFFB8)
#define ADST        ADCSR_BIT.b5                               /* A/D start                      */
#define ADCR        *(volatile unsigned char *)0xFFB9          /* A/D control register           */
#define ADDRA       *(volatile unsigned int *)0xFFB0           /* A/D data register A            */
#define ADDRB       *(volatile unsigned int *)0xFFB2           /* A/D data register A            */
#define ADDRC       *(volatile unsigned int *)0xFFB4           /* A/D data register A            */
#define ADDRD       *(volatile unsigned int *)0xFFB6           /* A/D data register A            */

#pragma interrupt (tmrw)
#pragma interrupt (tmrv)

/*   Function definition                                                                         */
extern void INIT(void);                                        /* Stack pointer set              */
void main(void);                                               /* main routine                   */
void tmrw(void);                                               /* Timer W interrupt routine      */
void tmrv(void);                                               /* Timer V interrupt routine      */

/*   Data table                                                                                  */
const unsigned char dsp_data[10] =
{
0x3f,                                                          /* LED display data = "0"         */
     0x06,                                                     /* LED display data = "1"         */
     0x5b,                                                     /* LED display data = "2"         */
     0x4f,                                                     /* LED display data = "3"         */
     0x66,                                                     /* LED display data = "4"         */
     0x6d,                                                     /* LED display data = "5"         */
     0x7d,                                                     /* LED display data = "6"         */
     0x27,                                                     /* LED display data = "7"         */
     0x7f,                                                     /* LED display data = "8"         */
     0x6f,                                                     /* LED display data = "9"         */
};

/*   RAM define                                                                                  */
unsigned char dig_0;                                           /* Dig-0 LED display data store   */
unsigned char dig_1;                                           /* Dig-1 LED display data store   */
unsigned char dig_2;                                           /* Dig-2 LED display data store   */
unsigned char dig_3;                                           /* Dig-3 LED display data store   */
unsigned char cnt;                                             /* LED enable counter             */
unsigned char counter_sub;
float convdat;                                                 /* Convert data (VOLT)            */
unsigned int temp;
unsigned char *ptr;                                            /* Pointer set                    */

/*   Vector address                                                                              */
#pragma section V1                                             /* Vector section set             */
void (*const VEC_TBL1[])(void) = {
     INIT                                                      /* H'0000 Reset vector            */
};
#pragma section V2                                             /* Vector section set             */
void (*const VEC_TBL2[])(void) = {
     tmrw                                                      /* H'002a Timer W interrupt vector */
};
#pragma section V3                                             /* Vector section set             */
void (*const VEC_TBL3[])(void) = {
     tmrv                                                      /* H'002c Timer V interrupt vector */
};
#pragma section                                                /* P                              */
```

```
/******************************************************************************************************************************/
/*   Main program                                                                                                             */
/******************************************************************************************************************************/
void main(void)
{
set_imask_ccr(1);                                                            /* CCR I-bit = 1                         */

convdat = 5.0 / 1023.0 * 100.0;                                              /* Set convert constant                  */

     dig_0 = 0x40;                                                           /* Used RAM area initialize              */
      dig_1 = 0x40;                                                          /* Used RAM area initialize              */
     dig_2 = 0x40;                                                           /* Used RAM area initialize              */
     dig_3 = 0x40;                                                           /* Used RAM area initialize              */
     cnt   = 0x00;                                                           /* Used RAM area initialize              */

     PCR2  = 0x03;                                                           /* Port 2 initialize                     */

     PCR5  = 0xff;                                                           /* Port 5 initialize                     */

                                                                             /* Timer W initialize                    */
TCRW = 0x30;                                                                 /* Clock Select                          */
TSRW = 0x00;                                                                 /* Clear OVF                             */
TMRW = 0x80;                                                                 /* Timer Counter Count Start             */
TIERW = 0x00;                                                                /* OVF Interrupt Disable                 */
counter_sub = 15;                                                            /* Initialize 8bit Counter_sub           */

     TCRV0 = 0x03;                                                           /* Timer V initialize                    */
     TCRV1 = 0xe3;                                                           /* Internal clock select                 */
     TCSRV = 0x10;                                                           /* Clear OVF to 0                        */

     ADCSR = 0x00;                                                           /* A/D converter initialize              */
     ADCR  = 0x7e;

     OVF     = 0;                                                            /* Clear OVF to 0                        */
     OVFW    = 0;                                                            /* Clear OVF to 0                        */
     OVIE    = 1;                                                            /* Timer V OVF interrupt enable          */
     OVIEW   = 1;                                                            /* Timer W OVF interrupt enable          */


set_imask_ccr(0);                                                            /* CCR I-bit = 0                         */

     while(1);
}
```

```
/*****************************************************************************************************************************/
/*   Timer W Interrupt                                                                                                       */
/*****************************************************************************************************************************/
void tmrw(void)
{
if ( OVFW == 1 ) {
OVFW = 0;                                                                    /* Clear OVF                                    */
counter_sub--;                                                               /* Decrement 8bit Counter                       */
if ( counter_sub == 0x00 ){                                                  /* 8bit Counter != H'00                         */
counter_sub = 15;                                                            /* Initialize 8bit Counter_sub                  */
          ADST  = 1;                                                         /* A/D converter start                          */
          while(ADST == 1);                                                  /* A/D converter end ?                          */
temp = (ADDRA >> 6) & 0x3ff;                                                 /* Pick up 10bit data                           */
temp = (float)temp * convdat;                                                /* Convert A/D to volt                          */
                                                                             /* Display Decimal                              */
if (temp/1000 == 0) {
dig_3 = 0x00;                                                                /* Dig-3 LED display data set                   */
} else {
dig_3 = dsp_data[temp / 1000];                                               /* Dig-3 LED display data set                   */
}
dig_2 = dsp_data[(temp % 1000) / 100] | 0x80;                                /* Dig-2 LED display data set                   */
dig_1 = dsp_data[(temp % 100) / 10];                                         /* Dig-1 LED display data set                   */
dig_0 = dsp_data[temp % 10];                                                 /* Dig-0 LED display data set                   */
}
}
}

/*****************************************************************************************************************************/
/*   Timer V Interrupt                                                                                                       */
/*****************************************************************************************************************************/
void tmrv(void)
{
     ptr = &dig_0;                                                           /* LED display data store address set           */

     while(OVF == 1){                                                        /* OVF = 1 ?                                    */
          OVF  = 0;                                                          /* Clear OVF to 0                               */
          ptr += cnt;                                                        /* LED display data read                        */
          PDR5 = *ptr;                                                       /* LED display data output                      */
          PDR2 = cnt;                                                        /* LED enable data output                       */
          cnt++;                                                             /* "cnt" increment                              */
          if (cnt >= 4){                                                     /* 4 times end ?                                */
               cnt = 0;                                                      /* "cnt" initialize                             */
          }
     }
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.29.03	—	First edition issued