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Renesas Electronics Corporation

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M16C/80 Group

Operation of A-D Converter (in one-shot mode, an external trigger)

1.0 Abstract

In one-shot mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

Table 1. Chosed functions

Item	Set-up	Item	Set-up
Operation clock ϕ_{AD}	<input type="radio"/> Divided-by-4 f_{AD} / divided-by-2 f_{AD} / f_{AD}	Expanded analog input pin	<input type="radio"/> Not used
Resolution	<input type="radio"/> 8-bit / 10-bit		<input type="radio"/> Either ANEX0 pin or ANEX1 pin
Analog input pin	<input type="radio"/> One of AN0 pin to AN7 pin		<input type="radio"/> External operation amplifier connection mode
Trigger for starting A-D conversion	<input type="radio"/> Software trigger	Sample & Hold	<input type="radio"/> Not activated
	<input type="radio"/> Trigger by ADTRG		<input type="radio"/> Activated

2.0 Introduction

- Operation (1) If the level of the $\overline{AD_{TRG}}$ changes from "H" to "L" with the A-D conversion start flag set to "1", the A-D converter begins operating.
- (2) After A-D conversion is completed, the content of the successive comparison register (conversion result) is transmitted to A-D register i. At this time, the A-D conversion interrupt request bit goes to "1". Also the A-D converter stops operating.
- (3) If the level of the $\overline{AD_{TRG}}$ pin changes from "H" to "L", the A-D converter carries out conversion from step (1) again. If the level of the $\overline{AD_{TRG}}$ pin changes from "H" to "L" while conversion is in progress, the A-D converter stops the A-D conversion in process, and carries out conversion from step (1) again.

Figure 1 shows the operation timing

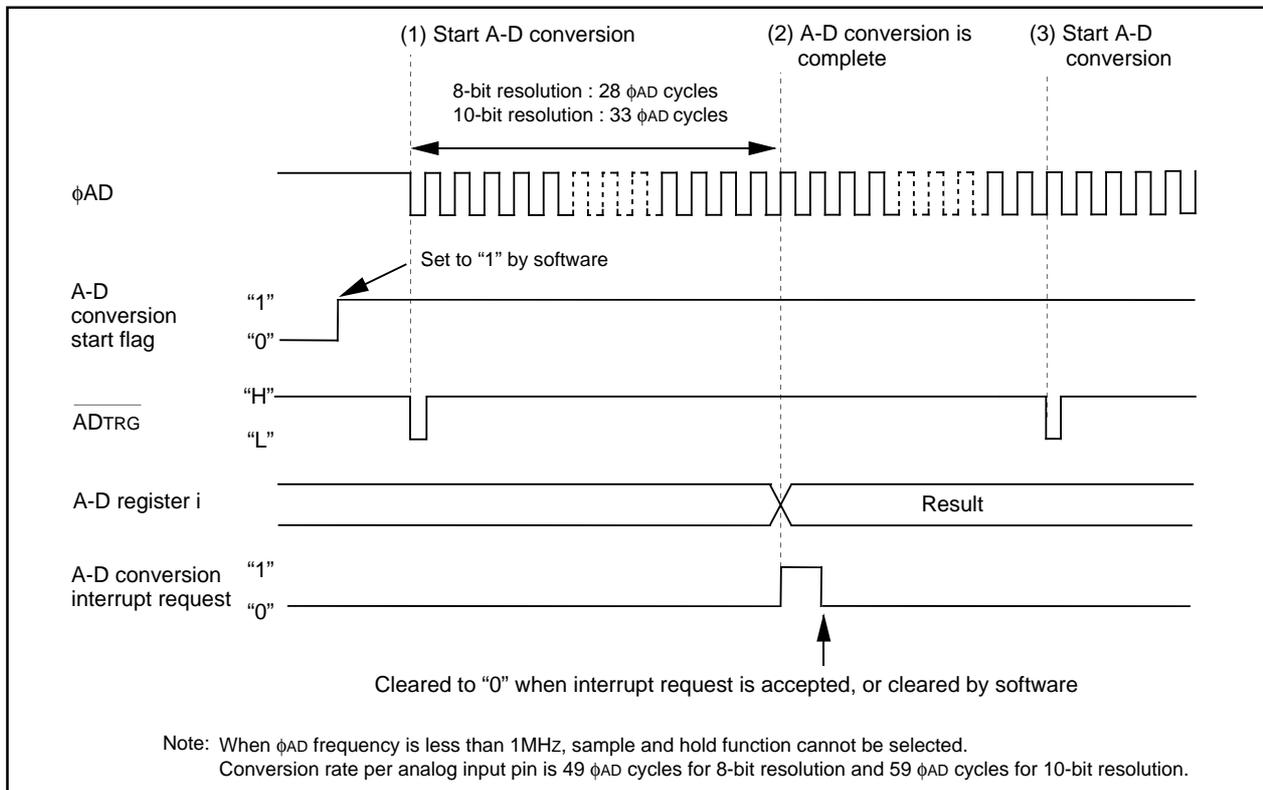
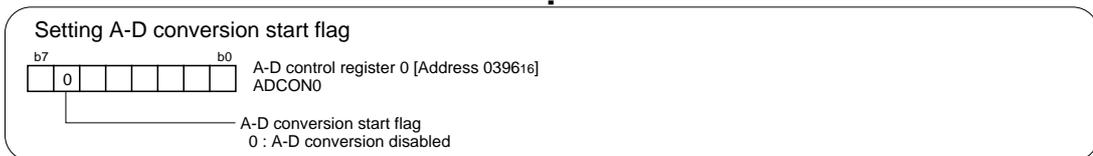
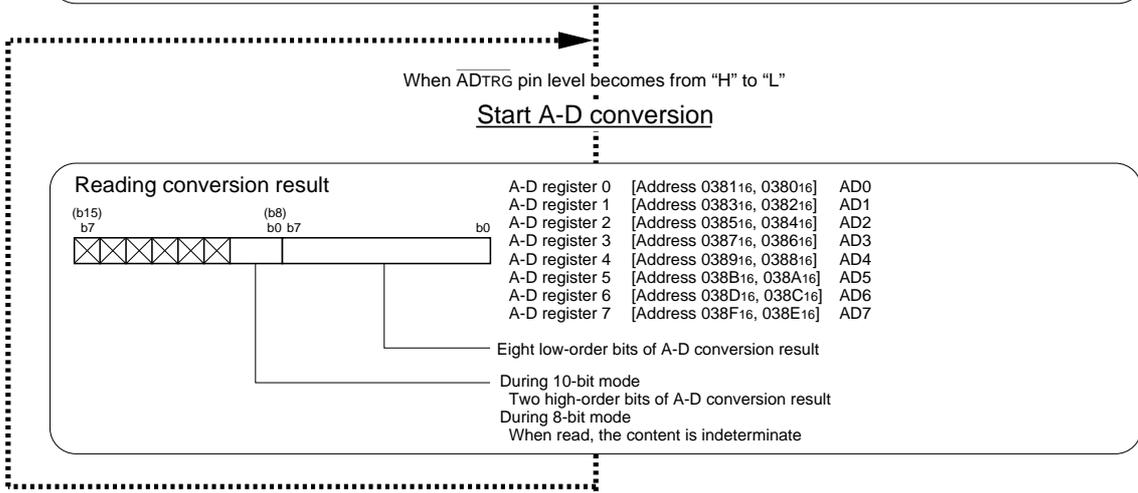
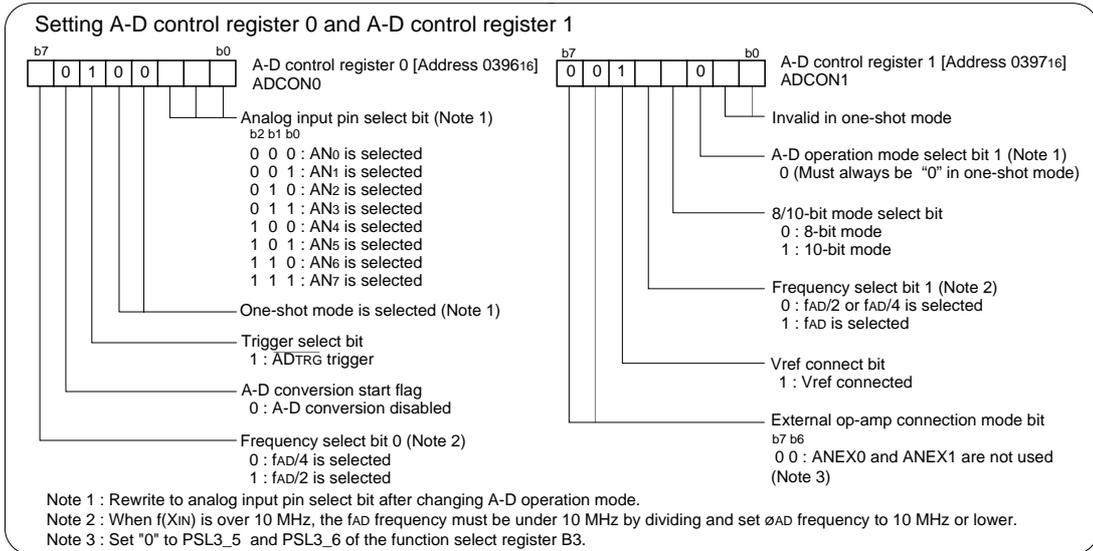


Figure 1. Operation timing of one-shot mode, with an external trigger selected

3.0 Set-up procedure



Stop A-D conversion

Operation of A-D Converter (in one-shot mode, an external trigger)

```

;=====
;      A-D Converter (in one-shot mode, an external trigger selected)
;=====
; Disabled A-D conversion interrupt and clear interrupt request bit to "0"
MOV.B   #00h, adic
; Selecting Sample and hold
MOV.B   #00000001B, adcon2
;
;           +-----;A-D conversion method select bit
;           (1:With sample and hold)
; Setting A-D control register 0 and A-D control register 1
MOV.B   #10100000B, adcon0
;
;           |||+++-----;Analog input pin select bit (000:AN0 is selected)
;           |||+++-----;One-shot mode is selected
;           ||+-----;Trigger select bit (1:ADTRG trigger)
;           |+-----;A-D conversion start flag (0:A-D conversion disabled)
;           +-----;Frequency select bit 0 (1:fAD/2 is selected)
MOV.B   #00101000B, adcon1
;
;           |||+++-----;Invalid in one-shot mode
;           |||+++-----;A-D operation mode select bit1
;           |||+++-----;      (Must always be "0" in one-shot mode)
;           |||+++-----;8/10-bit mode select bit (1:10-bit mode)
;           ||+-----;Frequency select bit 1 (0:fAD/2 or fAD/4 is selected)
;           |+-----;Vref connect bit (1:Vref connected) (Note)
;           +-----;External op-amp connection mode bit
;           (00:ANEX0 and ANEX1 are not used) (Note)
; Setting the direction register of the relevant port to input
BCLR    pd10_0      ;AN0(P100):Analog input pin
; Setting the direction register of the external trigger input pin
MOV.B   #00000100B, prcr ;Clearing the protect (set to write-enabled state)
;
;           +-----;Enables writing to port P9 direction register
BCLR    pd9_7      ;ADTRG(P97):A-D external trigger input pin
MOV.B   #00000100B, prcr
BCLR    ps3_7      ;ADTRG(P97) is I/O port
; (Note) Setting function select register B3 (ANEX0 & ANEX1 are not used)
BCLR    ps13_5     ;P95:Input peripheral function enabled
BCLR    ps13_6     ;P96:Input peripheral function enabled
;
;-----
;      Start A-D conversion
;-----
; (Note) When the Vref connection bit is changed from 0 to 1,
; start A-D conversion after an elapsing of 1 us or longer.
MOV.W   #10, R0    ; 10 * 2cy = 20cy = 1 us or longer (@20MHz)
PRE_START:
NOP
NOP
ADJNZ.W #-1, R0, PRE_START
;
; Setting A-D conversion start flag
BSET    adst
START_AD:
;
; When ADTRG pin level becomes from "H" to "L", Start A-D conversion
;
WAIT_AD_CNV:
BTST    ir_adic    ; Waiting A-D conversion completing
JNC     WAIT_AD_CNV
BCLR    ir_adic    ; Clear to "0" A-D conversion interrupt request
;
COMPLETE_CNV:
; Reading conversion result
MOV.W   ad0, v_AD_result ; Read conversion result
AND.W   #03FFH, v_AD_result ; Mask 10 bits result
;
JMP     START_AD
;

```

Operation of A-D Converter (in one-shot mode, an external trigger)

```

;-----
;      Stop A-D conversion
;-----
STOP_AD:
      BCLR      adst          ; A-D conversion stop
;
STOPPED_AD:
      JMP      STOPPED_AD
;
;=====
;      Dummy interrupt processing program
;=====
dummy:
      REIT
;
;*****
;      Setting of fixed vector
;*****
      .SECTION  F_VECT, ROMDATA
      .ORG     FIXED_VECT_TOP
;
      .LWORD   dummy      ;Undefined instruction
      .LWORD   dummy      ;Overflow
      .LWORD   dummy      ;BRK instruction execution
      .LWORD   dummy      ;Address match
      .LWORD   dummy      ;
      .LWORD   dummy      ;Watchdog timer
      .LWORD   dummy      ;
      .LWORD   dummy      ;NMI
      .LWORD   RESET      ;Reset
;
      .END

```

5.0 Reference**Renesas Technology Corporation Semiconductor Home page**<http://www.renesas.com/>**Technical Support**E-mail: support_apl@renesas.com**Data Sheet**

M16C/80 group Rev. E3

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