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Renesas Electronics Corporation

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Application Note

Power MOS FET

Application Note

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Rev.2.00 2004.08

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Power MOS FET

Application Note

1. Electrical Characteristics Definition and Usage Explanation

1.1 Absolute Maximum Ratings and Electrical Characteristics

1.1.1 Absolute Maximum Ratings

Figure 1.1 shows the meaning of power MOSFET absolute maximum ratings.

Example of 2SK3418 (Ta = 25°C)

Item	Symbol	Rating	Unit
Drain to source voltage	V_{DSS}	60	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	85	A
Drain peak current	I_D(pulse) *1	340	A
Body-drain diode reverse drain current	I_{DR}	85	A
Avalanche current	I_{AP} *2	60	A
Avalanche energy	E_{AR} *2	308	mJ
Channel dissipation	Pch *3	110	W
Channel temperature	Tch	150	°C
Thermal resistance	θch-c	1.14	°C/W

V_{DSS} has correlation to on-resistance

Lower for low-voltage drive component

Theoretical equation for drain current I_D:

$$I_D = \sqrt{\frac{Tchmax - Tc}{R_{DS(on)}max \times \alpha \times \theta ch - c}}$$

I_D(pulse) uses transient thermal resistance

$$\left(\alpha = \frac{150°C\ R_{DS(on)}}{25°C\ R_{DS(on)}}\right)$$

Rated current of source to drain diode

$$E_{AR} = \frac{1}{2} L \bullet I_{AP}^2 \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DSS}}$$

Pch temperature derating:

$$Pch(Tx) = Pch(25°C) \times \frac{Tchmax - Tc}{Tchmax - 25}$$

$$\theta ch\text{-}c = \frac{Tchmax - Tc}{Pch}$$

(Determined by package and chip size)

Notes: 1. Allowable value at PW ≤ 10μs, duty ≤ 1%
2. Allowable value at Tch = 25°C, Rg ≥ 50Ω
3. Allowable value at Tc = 25°C

Figure 1 Power MOS FET Absolute Maximum Ratings

1.1.2 Electrical Characteristics

Table 1.1 shows the meaning of power MOSFET electrical characteristics.

Table 1.1 Power MOS FET Electrical Characteristics

(Ta = 25°C)

Item	Symbol	Ratings			Test Conditions	Unit	Temperature Dependence	Design Notes
		Min	Typ	Max				
Drain to source breakdown voltage	$V_{(BR)DSS}$	60	—	—	I_D = 10mA, V_{GS} = 0	V	●	Correlation to on-resistance
Zero gate voltage drain current	I_{DSS}	—	—	10	V_{DS} = 60V, V_{GS} = 0	μA	●	Thermal dependence is high, but low in terms of loss
Gate to source leakage current	I_{GSS}	—	—	±0.1	V_{GS} = ±20V, V_{DS} = 0	μA	—	For products with on-chip protective diode, several tens of nA to several μA, guaranteed value of ±10 μA
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V_{DS} = 10V, I_D = 1mA	V	○	Affects switching operation noise and switching time tr, tf
Forward transfer admittance	|Yfs|	55	90	—	I_D = 45A, V_{DS} = 10V	s	○	
Static drain to source on state resistance 1	$R_{DS(on)1}$	—	4.3	5.5	I_D = 45A, V_{GS} = 10V	mΩ	●	Most important parameters in determining on-loss. Note that these rise together with temperature.
Static drain to source on state resistance 2	$R_{DS(on)2}$	—	6.0	9.0	I_D = 45A, V_{GS} = 4V	mΩ	●	
Input capacitance	Ciss	—	9770	—	V_{DS} = 10V, V_{GS} = 0, f = 1MHz	pF	—	V_{DS} dependent. Drive loss indicator in analog operation
Output capacitance	Coss	—	1340	—		pF	—	V_{DS} dependent. Affects fall time tf under light load.
Reverse transfer capacitance	Crss	—	470	—		pF	—	V_{DS} dependent. Influences switching time tr, tf.
Total gate charge	Qg	—	180	—	V_{DD} = 50V, V_{GS} = 10V, I_D = 85A	nC	—	Characteristic that determines drive loss. Greatly dependent on gate drive voltage.
Gate to source charge	Qgs	—	32	—		nC	—	
Gate to drain charge	Qgd	—	36	—		nC	—	Characteristic that determines switching time tr, tf. Dependent on power supply voltage V_{DD} (increases when V_{DD} rises).
Turn-on delay time	td(on)	—	53	—	V_{GS} = 10V, I_D = 45A, R_L = 0.67Ω, Rg = 50Ω	ns	—	Determined by Rg, Qgd, and gate drive voltage. Influence diode on-loss in inverter use.
Rise time	tr	—	320	—		ns	—	
Turn-off delay time	td(off)	—	700	—		ns	—	Determined by Rg, Qgd, and Vth. Influence surge voltage (noise) when switching off.
Fall time	tf	—	380	—		ns	—	
Body-drain diode forward voltage	V_{DF}	—	1.0	—	I_F = 85A, V_{GS} = 0	V	○	Becomes same characteristic as on-resistance when positive bias is applied to V_{GS}.
Body-drain diode reverse recovery time	trr	—	70	—	I_F = 85A, V_{GS} = 0, di/dt = 50μA/μs	ns	●	Short-circuit current: lowers di/dt to suppress noise.

Note: ●: Has positive temperature coefficient, ○: Has negative temperature coefficient

1.2 Relationship between On-Resistance $R_{DS(on)}$ and Withstand Voltage V_{DSS}

Figure 1.2 shows the relationship between a withstand voltage V_{DSS} = 20 to 100 V rated component and on-resistance $R_{DS(on)}$. When selecting the withstand voltage of an component, a margin should be left in the settings with respect to circuit operation conditions power supply voltage V_{DD} and surge voltage $V_{DS(peak)}$ generated when switching off. As V_{DSS} has a positive temperature characteristic with respect to temperature, the minimum temperature environment conditions for use of the component must be taken into consideration.

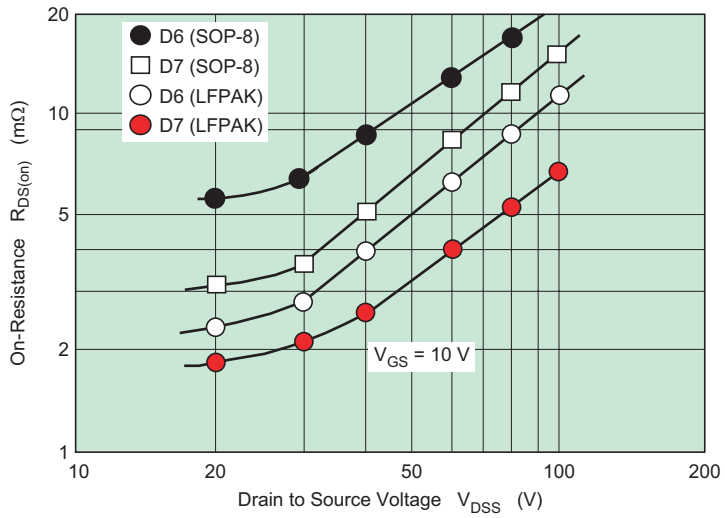


Figure 1.2 $R_{DS(on)}$ – V_{DSS} Relationship

Figure 1.3 shows the $V_{(BR)DSS}$ temperature characteristic (taking the example of the 2SK3418). In this case, making the withstand voltage margin larger than necessary is inadvisable as it will result in higher on-resistance and greater steady-state loss. Recently, components have appeared that can handle guaranteed avalanche resistance in order to reduce this margin as much as possible and provide the benefit of lower loss.

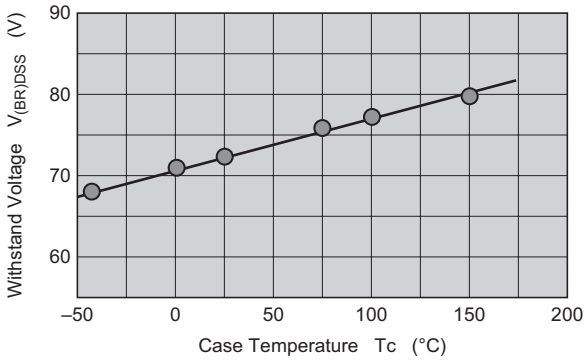


Figure 1.3 $V_{(BR)DSS}$ – Tc Characteristics (2SK3418)

1.3 Saturation Voltage $V_{DS(on)}$(= Id × $R_{DS(on)}$) Gate Drive Voltage Dependence

This characteristic is a characteristic curve for designing at what gate drive voltage the $V_{DS(on)}$ area (on-resistance area) is effected in the case of a predetermined operating current Id.

In the case of power MOS FETs, 10 V drive components, 4 V drive components, 4 V drive (or lower) components are produced according to the gate drive operating current. The means of achieving low-voltage drive is generally to use a thin gate oxide film (whereby the gate-source withstand voltage V_{GSS} rating is reduced) to attain a lower $V_{GS(off)}$ value.

$V_{GS(off)}$ has an approximately –5 mV/°C negative temperature coefficient (characteristic that falls approximately 0.5 V with a 100°C rise).

When selecting the type of component in terms of drive voltage, it is necessary to consider the application (for example, selection of a 10 V drive component with a high $V_{GS(off)}$ value to cope with noise in switching power supply or motor drive applications) and the specifications of the gate drive IC or LSI to be used (such as a low-level voltage that keeps the MOS FET off).

Recently, therefore, a distinction may be made between the use of 4 V drive components and 10 V drive components according to the conditions of use and application even in automotive electrical equipment.

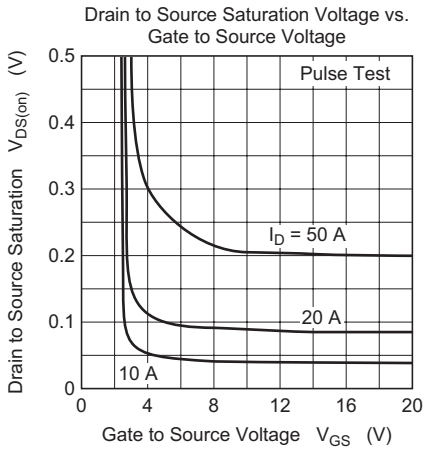


Figure 1.4 $V_{DS(on)}$ – V_{GS} Characteristics (2SK3418)

1.3.1 On-Resistance $R_{DS(on)}$ Temperature Dependence

Figure 1.5 shows temperature dependence of on-resistance $R_{DS(on)}$. Power MOS FET on-resistance $R_{DS(on)}$ has a positive temperature characteristic.

If the ratio between channel temperature rating Tch(max.) of 150°C and room temperature of 25°C (150°CRon/25°CRon) is designated α, the value is approximately 1.7 to 1.8 times for an component with a withstand voltage of 100 V or less, and approximately 2.4 to 2.5 times for an component with a withstand voltage of 500 V. It should also be noted that, as shown in the figure, $R_{DS(on)}$ does not rise linearly with a rise in temperature, but increases in a curvilinear shape.

What this means is that, when ambient temperature Ta = 100°C, for example, if the channel temperature calculation result is that Tch = 130°C, and Ta is made 120°C (a 20°C rise), Tch does not simply rise by 20°C to become 150°C, but rises above that temperature.

Therefore, when an component is used in a high-temperature environment such as automotive electrical equipment, this temperature characteristic must be carefully considered in heat radiation design. For details, refer to the power MOS FET heat radiation design example.

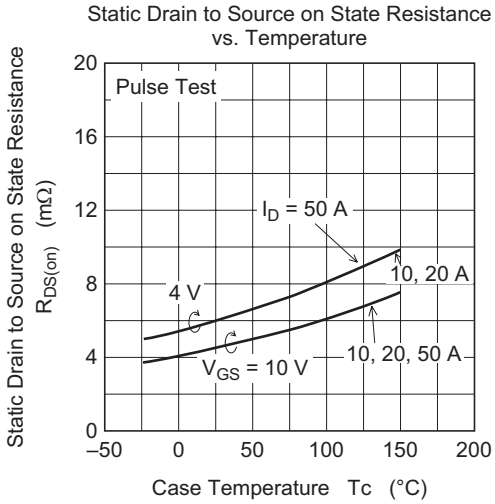


Figure 1.5 $R_{DS(on)}$ – Tc Characteristics (2SK3418)

1.4 Gate Charge Amounts Qg, Qgs, Qgd

In figure 1.6(a), the point up to prescribed drive voltage V_{GS} (=XV) is total charge amount Qg. This is the characteristic parameter that determines gate peak current ig(peak) for driving the gate and drive loss P(drive loss).

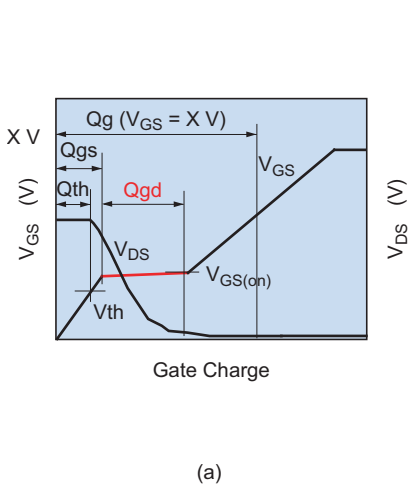
$$Ig(peak) = Qg/t \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(1)$$

$$P(drive\ loss) = f \cdot Qg \cdot V_{GS} \quad \ldots\ldots\ldots\ldots\ldots\ldots(2)$$

Qgd corresponds to mirror capacitance Crss, and depends on power supply voltage V_{DS}. It is also a parameter that influences switching characteristics.

$$tf \cong \frac{(Rs + rg) \cdot Qgd}{Vgs(on) - Vth} \log \frac{Vgs(on)}{Vth} \quad \ldots\ldots\ldots(3)$$

Fall time tf that controls L load switching loss is expressed by equation (3). Qg and Qgd are important items in designing high-frequency operation loss. In high-frequency (f = 100 kHz or above) applications, it can be said that the smaller the Ron·Qg or Ron·Qgd product, the higher is the performance of the component.



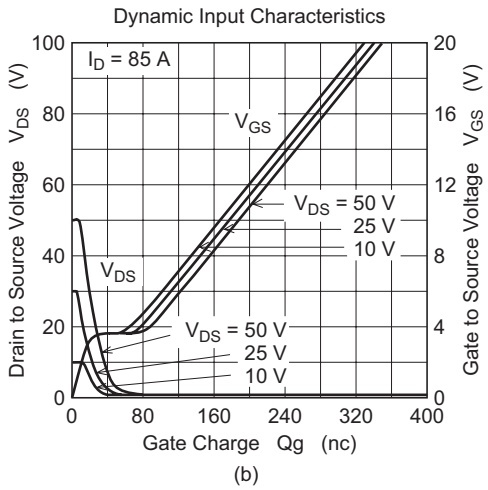


Figure 1.6 Input Dynamic Characteristics (2SK3418)

1.4.1 Characteristics of Internal Diode between Source and Drain

In a power MOSFET, a parasitic diode is provided between the source and drain. Rated current I_{DR} of this diode is the same value as forward drain current rating I_D.

The characteristics of this diode show the same forward voltage characteristics as an ordinary diode in the case of zero bias of the gate drive voltage (V_{GS} = 0). If the gate drive voltage is given positive bias (in the Nch case), as shown in Figure 1.7 there is a voltage drop determined by on-resistance $R_{DS(on)}$ (V_{SD} = Id × $R_{DS(on)}$) that is the same as in the forward direction, and a much lower forward voltage can be obtained even than with an SBD (Schottky barrier diode).

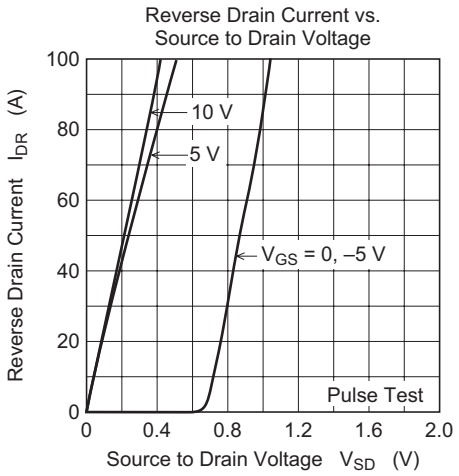


Figure 1.7 I_{DR} – V_{SD} Characteristics (2SK3418)

The benefits of such reverse-direction characteristics are actively applied in the following kinds of uses.

- Load switches for preventing battery reverse connection
- Switching power supply (n+1) redundant-type hot swap circuits
- Motor drive circuit external diode replacement
- Switching power supply secondary-side drive rectification circuits, etc.

1.5 Internal Diode Reverse Recovery Time trr Current I_{DR} Characteristic

In motor drive (power steering, starter generators, etc. in the case of electrical equipment) and switching power supply synchronous rectification applications that make positive use of a power MOSFET internal diode, there is a requirement for this reverse recovery time trr to be fast. In these applications, operationally upper arm/lower arm shorting and excess turn-on loss occur in this trr period. Generally, therefore, in the control circuitry, a dead time (longer than trr) is provided that turns off the gate signal at the time of upper/lower component switching.

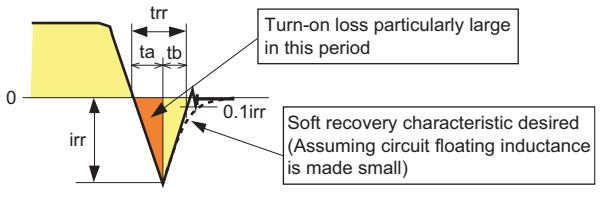


Figure 1.8 Reverse Recovery Time trr Waveform

This reverse recovery time trr shows a tendency to increase as the temperature rises. Also, the steeper di/dt at the time of recovery (area tb in figure 1.9), the more likely is the occurrence of noise, and therefore a soft recovery characteristic is desirable. Reverse recovery time trr differs greatly according to the withstand voltage of the component. In the case of a withstand voltage of 60 V or less, it is comparatively fast at a value of 40 to 60 ns. It is around 100 ns in the 100 V class, and around 300 to 600 ns in the 250 to 500 V high-withstand-voltage class. Therefore, in the high-withstand-voltage class of 250 V and above, products have been developed that have been speeded up to around 100 ns by means of lifetime control technology.

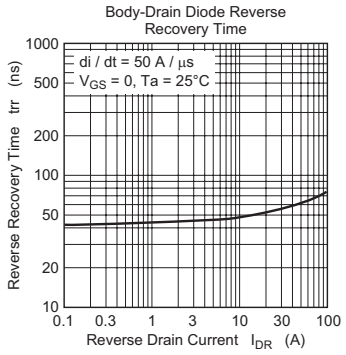


Figure 1.9 trr – I_{DR} Characteristics (2SK3418)

1.6 Transient Thermal Resistance Characteristic θch-c(t) – Pulse Width PW Characteristic

Figure 1.10 shows the θch-c(t)—pulse width PW characteristic. This is a characteristic for calculating channel temperature Tch in the component operating state. Pulse width PW on the horizontal axis is the operating time, and 1 Shot Single Pulse repeat operation conditions are shown.

For example, PW = 1 ms, D = 0.2 (duty cycle = 20%) means that the repetition frequency is 200 Hz (repetition cycle T = 5 ms).

Generally, when channel temperature rise ΔTch is calculated with duty cycle = 20% (D = 0,2), PW = 10 ms, and current dissipation Pd = 60 W, the following equation may be used, but since error arises as shown below, the transient thermal resistance characteristic should be used.

$$Tch = (0.2 \times Pd) \times \theta ch\text{-}c = (0.2 \times 60) \times 1.14 = 13.7°C$$

When the transient thermal resistance characteristic is used, 16.5ºC error arises as shown below.

$$Tch = Pd \times \theta ch\text{-}c(t) = 60 \times 0.44 \times 1.14 = 30.2°C$$

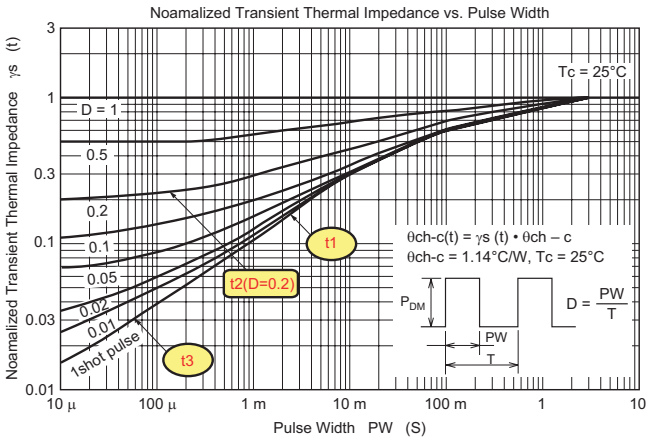
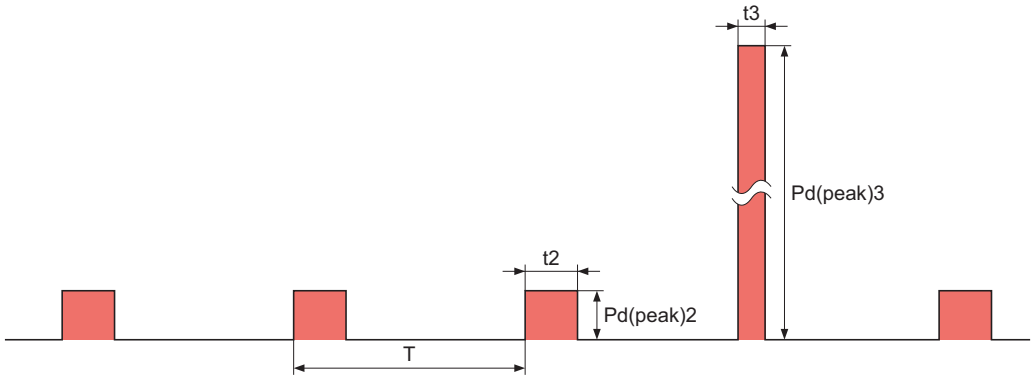


Figure 1.10 θch-c(t) – Pulse Width PW Characteristics (2SK3418)

Examples of channel temperature Tch calculation (2SK3418) using transient thermal resistance are shown below.

- Example 1
  To calculate channel temperature Tch under the following conditions: when case temperature Tc = 85°C, peak power Pd(peak)1 = 50 W, application time ts = 10 ms, 1 shot single pulse
  $Tch1 = Tc + (Pd(peak)1) \times \theta ch\text{-}c(t1) = 85 + (50 \times 0.3 \times 1.14) = 102.1°C$
- Example 2
  To calculate channel temperature Tch under the following conditions: when case temperature Tc = 85°C, operating frequency f = 2 kHz, repeat operation with duty cycle = 20%, applied power Pd(peak)2 = 50 W
  From the above operation, application time t2 = 100 μs, repetition cycle T = 500 μs, and D = t2/T = 0.2. Therefore:
  $Tch2 = Tc + (Pd(peak)2) \times \theta ch\text{-}c(t2/T) = 85 + (50 \times 0.22 \times 1.14) = 97.54°C$
- Example 3
  To calculate peak channel temperature Tch(peak) when peak power Pd(peak)3 = 500 W is further applied for a period of t3 = 60 μs by another circuit control system during the operation in Example 2
  $Tch2 = Tc + (Pd(peak)2) \times \theta ch\text{-}c(t2/T) + \{(Pd(peak)3 – Pd(peak)2 \times t2/T)\} \times \theta ch\text{-}c(t3)$
  $= 85 + (50 \times 0.22 \times 1.14) + (500 – 50 \times 0.2) \times 0.031 \times 1.14)$
  $= 85 + 12.54 + 17.32$
  $= 114.86°C$



1.7 Area of Safe Operation (ASO)

1.7.1 Area of Safe Operation (ASO) Diagram

Figure 1.11 shows an area of safe operation (ASO) diagram for the 2SK3418.

The ASO limited area is divided into the following 5 areas.

Area (1) is an area limited by maximum rated currents I_{DC}, $I_{D(pulse)}$max.

Area (2) is an area limited by on-resistance $R_{DS(on)}$max [$I_D = V_{DS}/R_{DS(on)}$]. Generally, this area is divided separately from the ASO area.

Area (3) is an area limited by channel loss.

Area (4) is the same kind of secondary breakdown area as in a bipolar transistor that appears under conditions of continuous operation or opened with a comparatively long pulse width (several ms or more). This is because, when the operating voltage increases in the same applied power line, the operating current naturally decreases, but in this small current area the output transfer characteristic (Vgs-Id characteristic) is a negative temperature characteristic. When the area becomes a large current area that entails a change to a positive temperature characteristic, this phenomenon disappears. The current value at which the temperature characteristic changes from negative to positive differs from product to product, and with products of several amperes or less this phenomenon is unlikely to occur, and this can be guaranteed with a so-called constant power line with no secondary breakdown.

Area (5) is an area limited by withstand voltage V_{DSS}max.

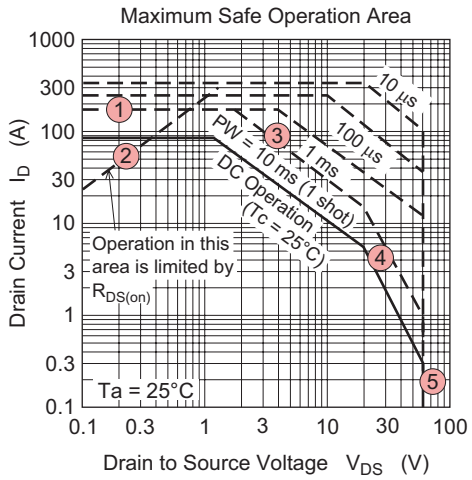


Figure 1.11 ASO Diagram (2SK3418)

1.7.2 Notes on ASO in Circuit Control System

As power MOS FETs are generally used in switching applications, in normal operation they are usually used in limited area (2). A point requiring attention in circuit design is the control system sequence.

Figure 1.12 shows an example of the power supply voltage and gate drive voltage sequence for a terminal electronic device when the system's source power supply is cut. As shown by the solid lines in the figure, if the fall time until power supply voltage V_{DD} is turned off is longer than that for gate drive voltage V_{GS}, V_{GS} is in an underdrive state in period t1 in the figure, and enters ASO limited area (4) or (5), making it necessary to confirm whether it is in an area of safe operation. An effective means of avoiding such an operation area is to perform sequence control so that the fall time of gate drive voltage V_{GS} is delayed beyond supply voltage V_{DD} as shown by the dotted lines.

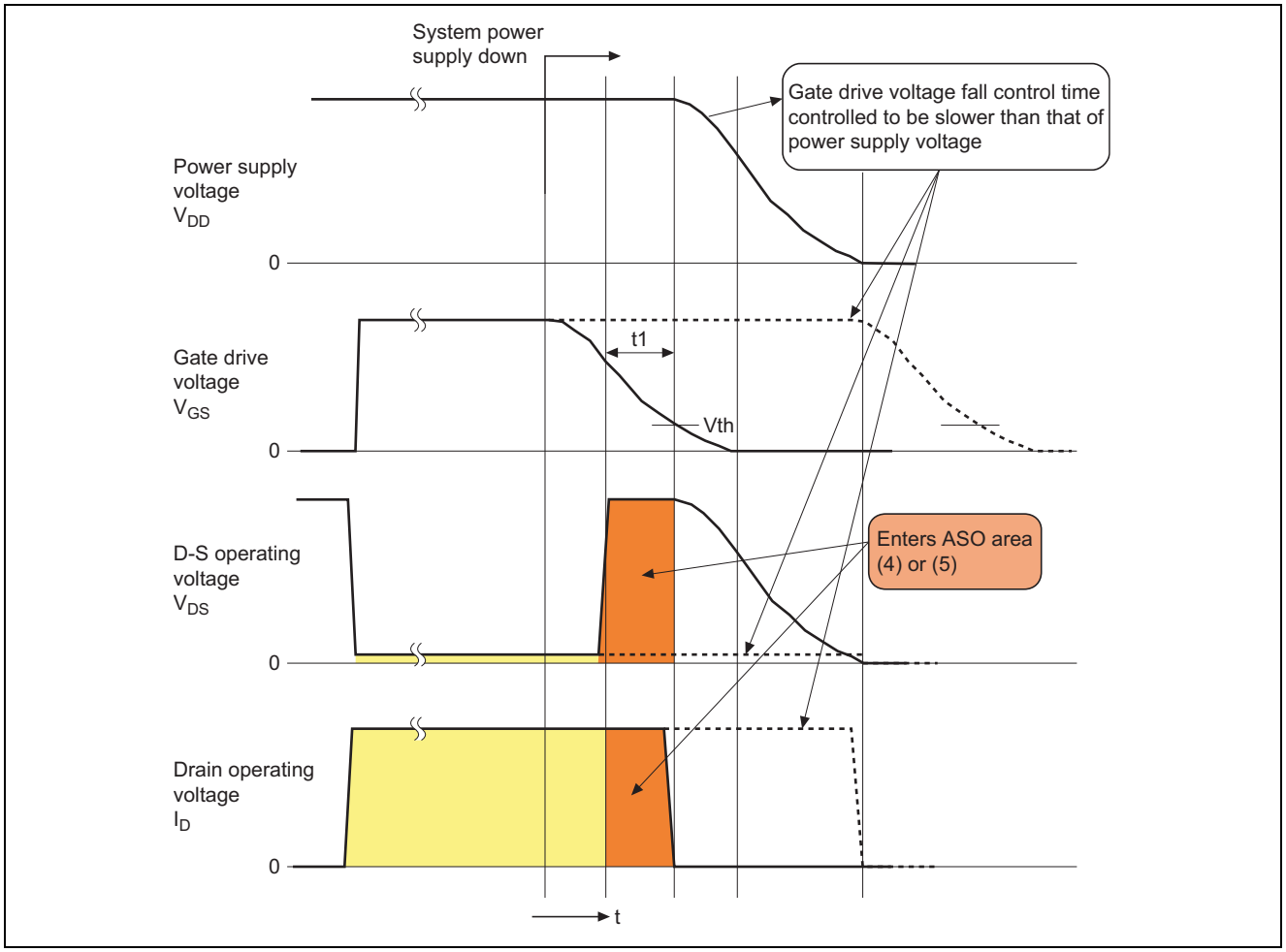


Figure 12 Example of Terminal Electronic Device System Power Supply Voltage and Gate Drive Voltage Sequence

2. Power MOS FET Destruction Mechanisms and Countermeasures

Introduction

As power MOS FETs are often used in the final output circuitry of electronic device application circuits, and are used under a wide range of conditions, circuit designers frequently have to confront the problem of unexpected component destruction.

The purpose of this section is to carry out electronic circuit design with a good understanding of the mechanisms behind such destruction, and produce as far as possible problems involving heat radiation, destruction, and so forth, in mass production and in the market after design is completed, in order to use power MOS FETs effectively.

2.1 Relationship between Power MOS FET Application Areas and Destruction Modes

2.1.1 Relationship between Main Power MOS FET Application Areas and Destruction Modes

Table 2.1 shows the relationship between main power MOSFET application areas and destruction modes. Power MOS FET destruction modes can be broadly be divided into the five modes shown below.

Table 2.1 Relationship between Power MOSFET Application Areas and Destruction Modes

Application Field / Application / Destruction Mode				Switching Power Supply								Automobile (electronic components)		Motor Drive		
				AC/DC(OA, Server)								Motor	Valve, solenoid	Low voltage	High voltage	
				Forward converter	Resonance method	Bridge circuit	Large-power parallel connection	DC-DC converter	Synchronous rectification	UPS (DC-AC)	Machine tool (electrostatic discharge)	EPS start-up generator	ABS direct gas injection	OA (PPC, HDD)	FA (servo)	Audio amp.
1	Avalanche destruction			◎	◎	◎	◎	◎	○	○	◎	○	◎	○	◎	—
2	ASO destruction	Forward-bias ASO		—	—	—	—	—	—	—	—	—	—	—	—	◎
		Loss ↓ Heat	ASO with short-circuit of load (Short-circuit between upper and lower sides)	—	○	○	—	—	○	◎	—	○	—	○	◎	—
			$R_{DS(on)}$	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	◎	—
			Switching	◎	◎	○	○	◎	◎	◎	◎	○	○	◎	○	—
			Built-in Di trr	—	◎	○	—	—	◎	◎	—	○	—	○	◎	—
3	Built-in diode destruction			—	○	○	—	—	○	◎	—	○	—	○	◎	—
4	Destruction by parasitic oscillation when operating with MOS FETs connected in parallel			—	—	○	◎	—	—	○	◎	—	—	—	—	◎
5	Gate surge or electrostatic destruction			Guard against static electricity during handling (including electrostatic charges on the mounting equipment), and against external surges that reach to the circuit.												

(1) Avalanche destruction mode

A phenomenon whereby destruction occurs if a surge voltage exceeding the rated V_{DSS} of the component is applied between the drain and source, destruction voltage $V_{(BR)DSS}$ (whose value differs according to the destruction current) is reached, and a certain energy level or higher is attained. This destruction energy differs according to the individual product and operating conditions.

(2) ASO (Area of Safe Operation) destruction

Mostly caused by heat caused by exceeding the so-called Area of Safe Operation, in which component maximum rating drain current Id, drain-source voltage V_{DSS}, or allowable channel dissipation Pth(W) is exceeded. Main causes of heat radiation are classified as a continuous or transient factors.

1. Continuous factors : Heat radiation due to DCASO (loss caused by DC power application)
   : On-resistance $R_{DS(on)}$ loss ($R_{DS(on)}$ increases at high temperatures)
   : Loss due to leakage current I_{DSS} (extremely small compared with other loss)
2. Transient factors : Pulse ASO (1 shot pulse application)
   : Load shorting ASO
   : Switching loss (turn-on, turn-off)*
   : Internal diode trr loss (Upper/lower arm shorting loss)*

All are temperature-dependent. Asterisked items also depend on operating frequency f.

(3) Internal diode destruction

This is a mode in which, when a parasitic diode configured between the source and drain operates, a power MOSFET parasitic bipolar transistor operates and breaks down in reverse recovery of that diode. (For details, see section 2.4, Internal Diode Destruction.)

(4) Destruction due to parasitic oscillation

This destruction mode is prone to occur in the case of parallel connection. (For details, see section 2.5, Destruction Due to Parasitic Oscillation, and section 2.6, Notes on Parallel Connection.)

(5) Gate surge, electrostatic destruction

Main types are gate overvoltage destruction caused by surge application between the gate and source from external circuitry, and gate destruction ESD (electrostatic discharge) caused by static electricity due to handling (including a charge from mounting or measuring equipment).

Table 2.1 shows the importance of the above five modes in various devices and applications, and taking these points into account when designing circuits and selecting components is an effective means of preventing various problems.

From this standpoint, the following considerations are important.

2.1.2 Power MOS FET Applications and Operating Range

Figure 2.1 shows the kind of operating conditions in which power MOS FET applications are used, with load inductance and operating frequency as parameters.

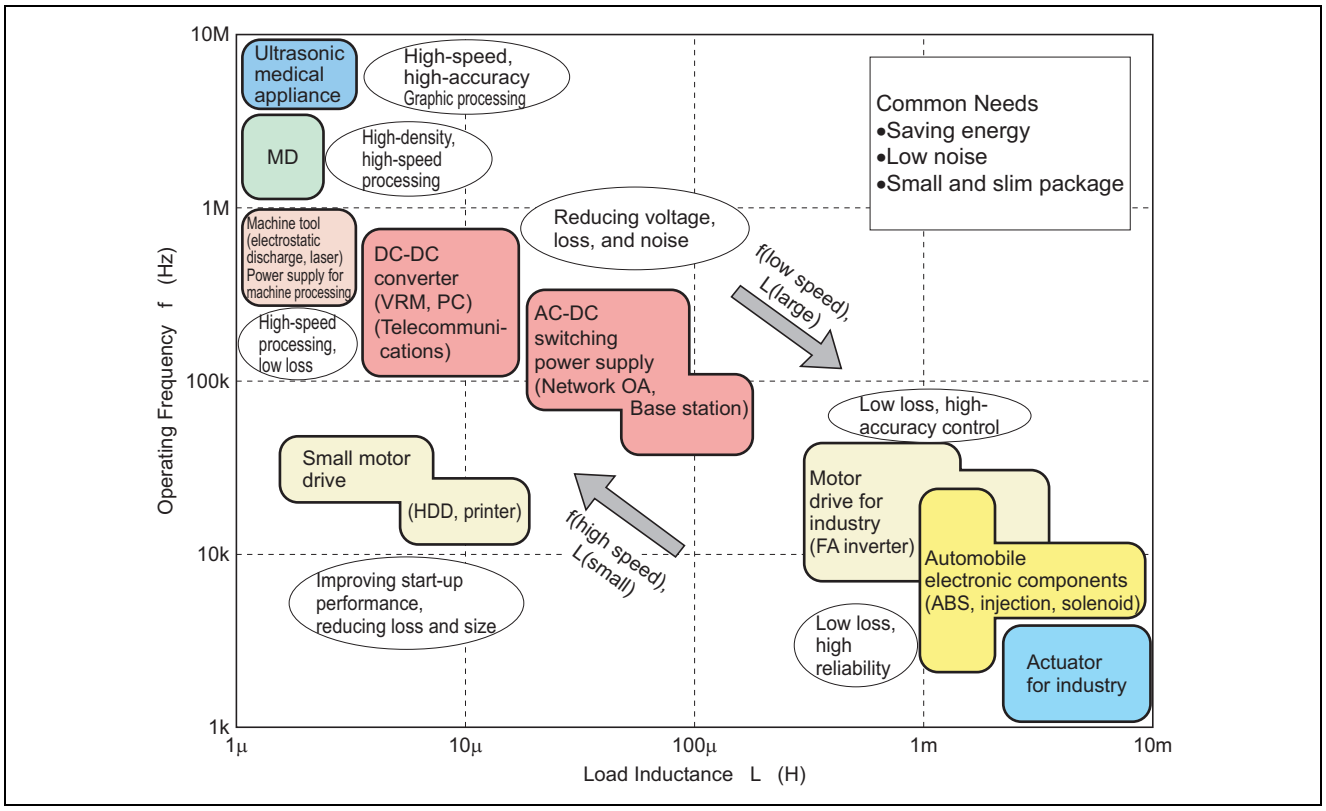


Figure 2.1 Power MOS FET Applications

Market requirements are (1) improved energy saving, (2) lower noise (environmental considerations), (3) smaller, thinner design.

With regard to the characteristics demanded of power MOS FETs, the most important characteristics and specifications naturally differ according to the field and application concerned.

Consequently, a demand has recently arisen for products specific to particular applications.

2.1.3 Power MOS FET Structure

Figure 2.2 shows an N-channel power MOS FET chip and its internal structure.

As shown in the figure, the internal structure of an N-channel power MOS FET chip comprises a large number of cells connected in parallel. As shown in the enlarged cell diagram, current flows in the source → drain direction (the reverse is true in a P-channel type).

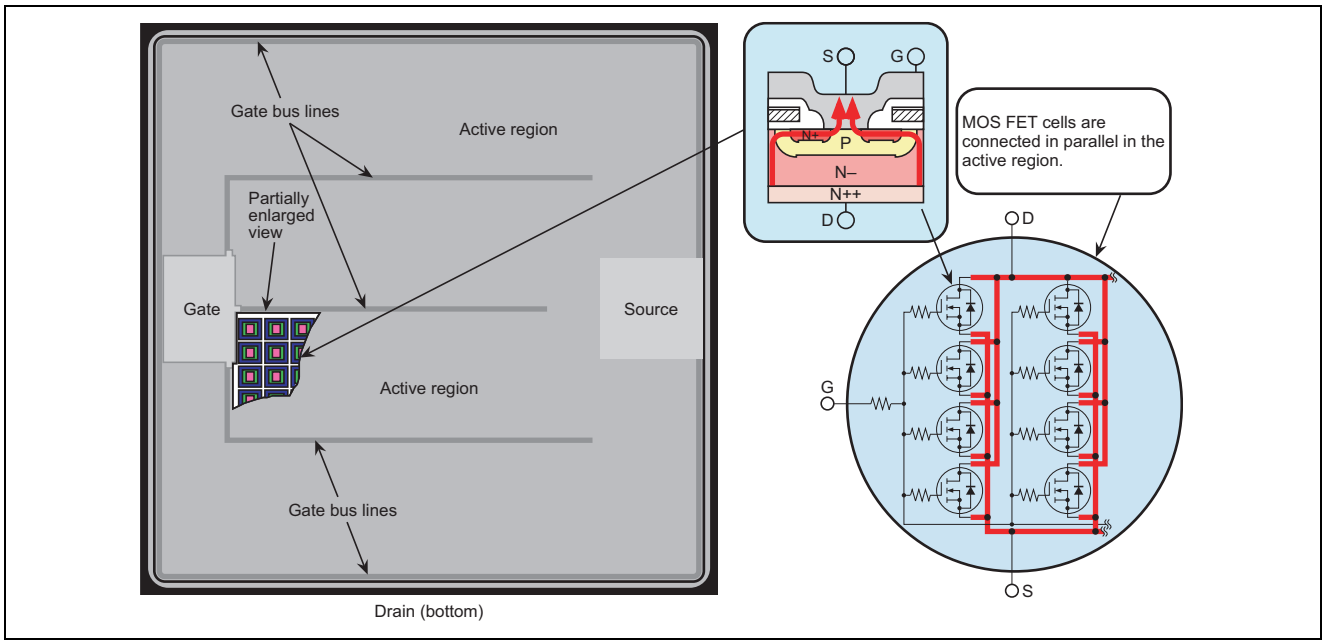


Figure 2.2 N-Channel Power MOS FET Chip and Internal Structure

Figure 2.3 shows the cross-sectional structure of an N-channel power MOS FET (with gate protection diodes).

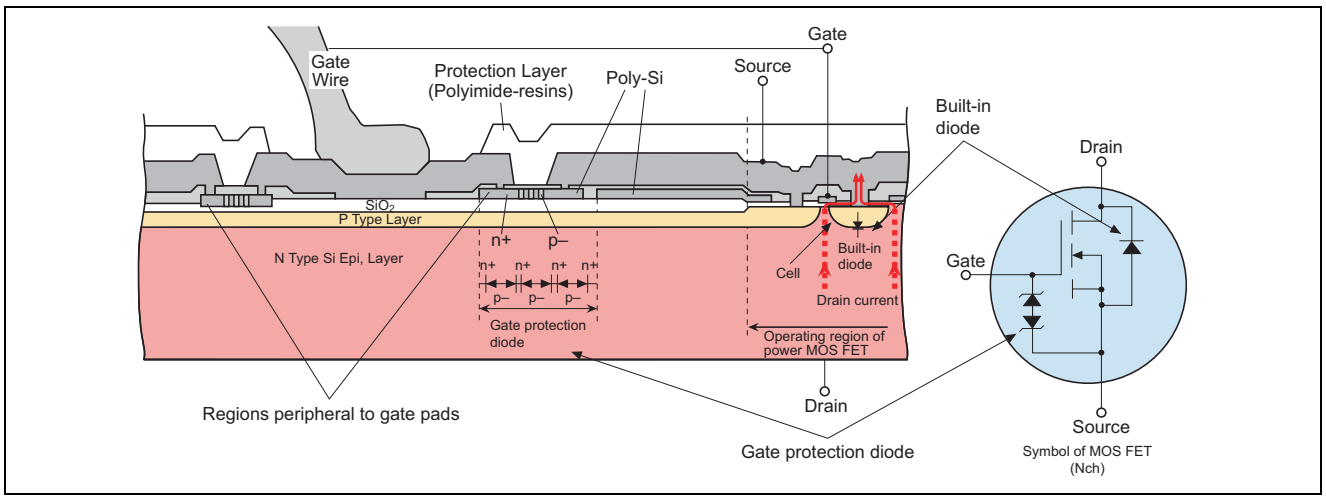


Figure 2.3 Cross-Sectional Structure of N-Channel Power MOS FET (with Gate Protection Diodes)

Figure 2.4 shows the output static characteristics and diode characteristics of a high-withstand-voltage power MOS FET (2SK1522). When a power MOS FET is used in a monitor drive, UPS (uninterruptible power supply), or similar application, the internal diode characteristics can be used effectively. The cell cross-sectional structure of a general power MOS FET plate structure is shown, together with an equivalent circuit diagram. A power MOS FET has a structure in which bipolar transistors are connected in parallel between drain and source. These transistors operate at the time of transitions, and are designed so that Rb is made small, for example, so as not to affect the MOS FET destruction tolerance.

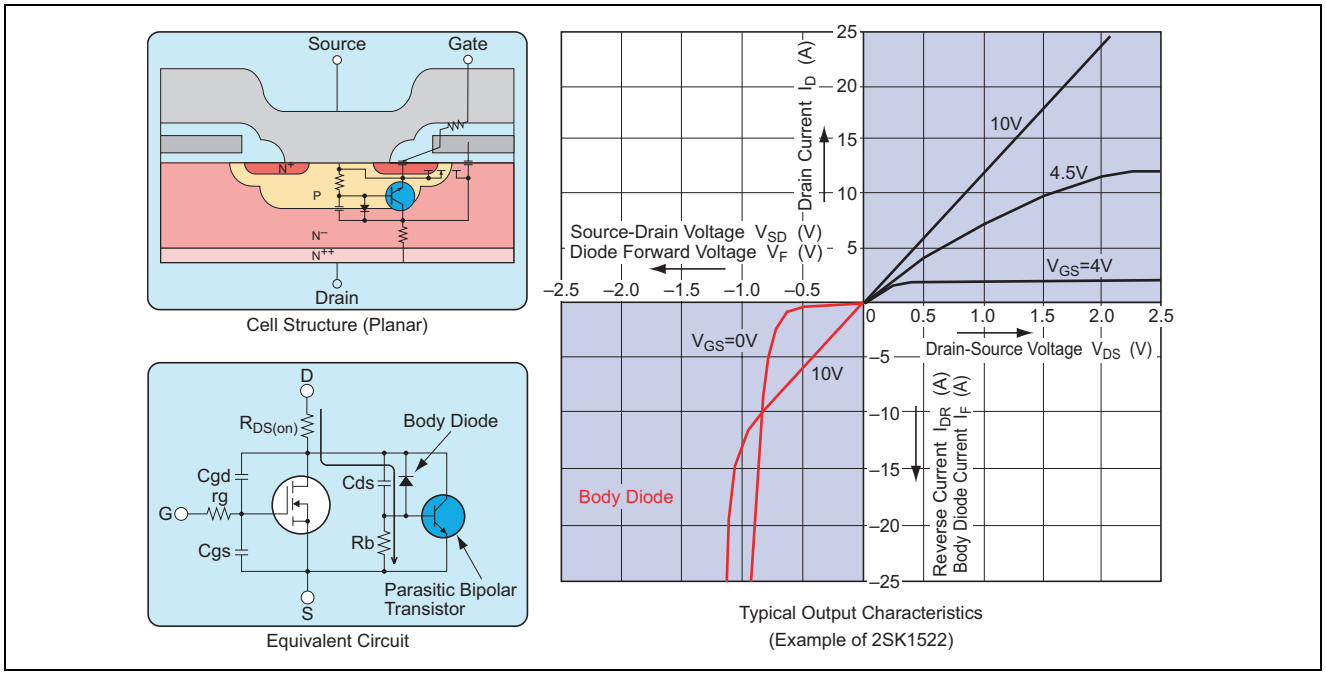


Figure 2.4 Output Static Characteristics and Diode Characteristics (High Withstand Voltage)

Figure 2.5 shows the output static characteristics and diode characteristics of a low-withstand-voltage power MOS FET (HAT2064R) in the same way as in the previous section. Low-withstand-voltage power MOS FETs attain an ultra-low on-resistance characteristic on the order of several mΩ or less, and are therefore much smaller than a rectification Schottky barrier diode (SBD) low-V_F component (V_F = 0.4 to 0.5 V), and are widely used as MOS synchronous rectification components for the purpose of achieving higher efficiency of low-voltage power supplies (Vout = 3.3 V or less).

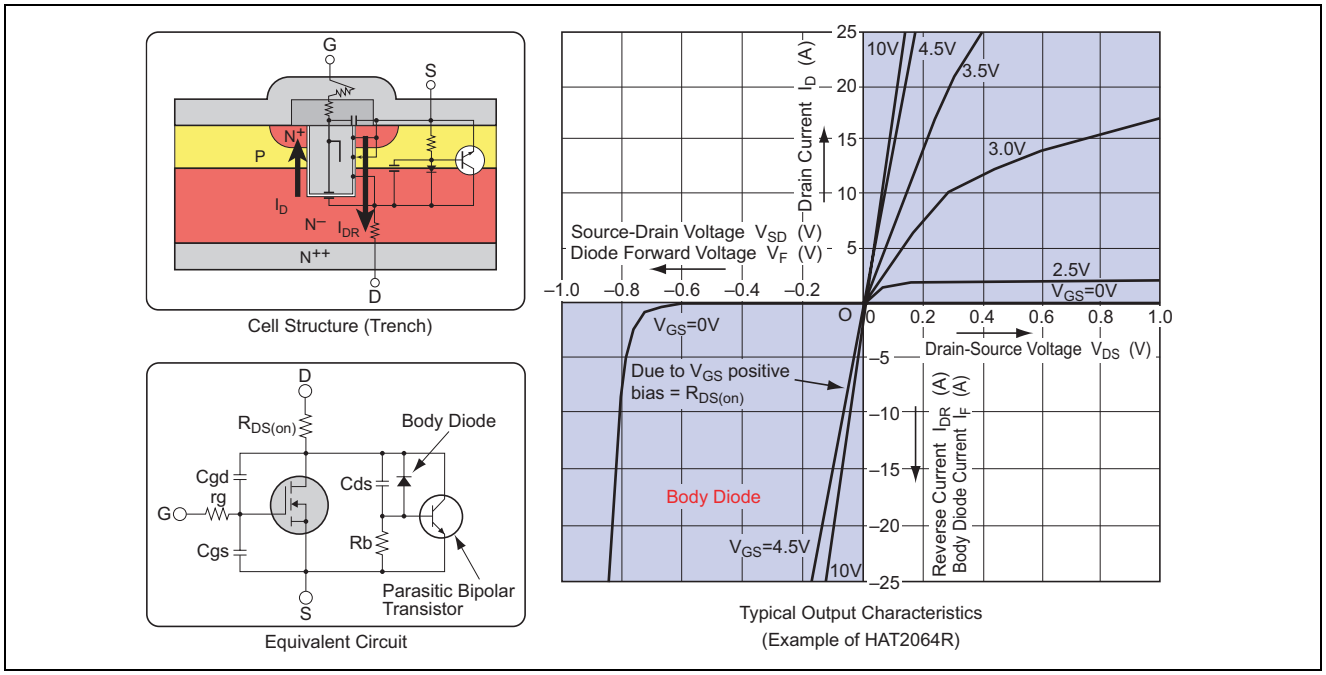


Figure 2.5 Output Static Characteristics and Diode Characteristics (Low Withstand Voltage)

2.2 Avalanche Destruction

2.2.1 Explanation of Avalanche Destruction

Avalanche destruction is a mode in which a flyback voltage generated when dielectric load switching operation is turned off, or a spike voltage due to leakage inductance, exceeds the power MOS FET drain rated withstand voltage, entered in a destruction area, and destruction occurs.

2.2.2 Avalanche Destruction Resistance Test Circuit and Waveform

Figure 2.6 shows an avalanche destruction resistance standard test circuit (a) and its operational waveform (b).

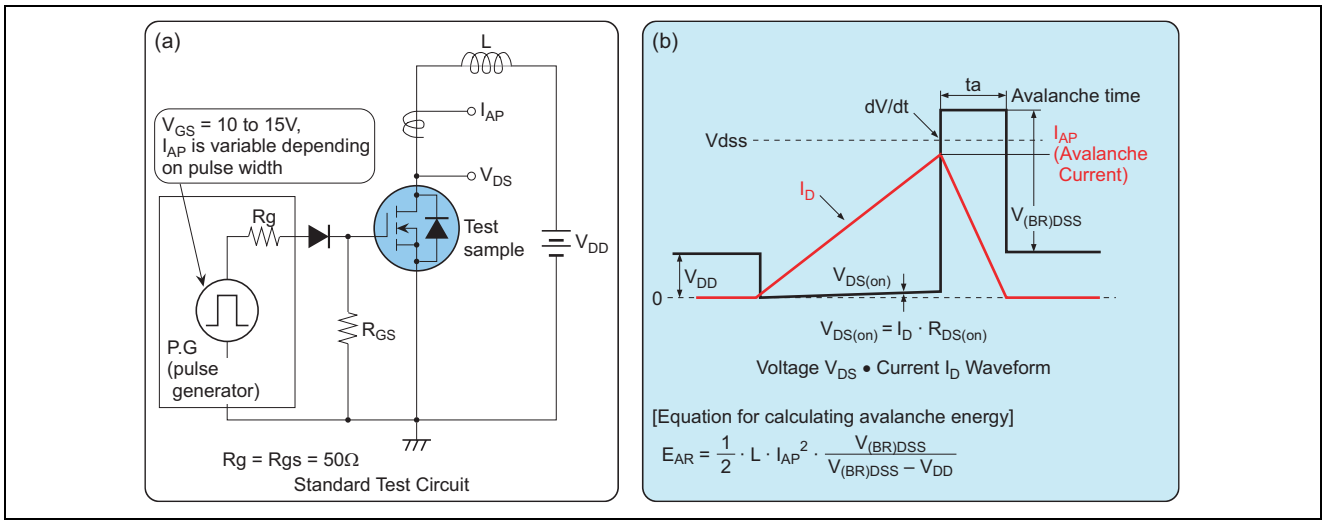


Figure 2.6 Avalanche Destruction Resistance Test Circuit and Waveform

Period ta in the waveform in (b) is defined as the avalanche time. The range in which drain-source peak voltage Vds(p) satisfies the condition Vdss ≤ Vds(p) < $V_{(BR)DSS}$ is an area in which the so-called rated voltage is exceeded but avalanche destruction has not been reached. In this kind of operation area, the avalanche area may or may not actually be entered depending on actual withstand voltage $V_{(BR)DSS}$ of the component, but it is advisable to select a product with guaranteed avalanche resistance. Avalanche resistance guaranteed products are all subjected to final screening by the standard circuit shown in (a). For avalanche resistance guaranteed products, avalanche current rated value I_{AP}(A) and avalanche energy value E_{AR}(J) are stipulated. E_{AR} is expressed by equation (1).

$$E_{AR} = Pd \cdot t = \frac{1}{2} V_{(BR)DSS} \cdot I_{AP} \cdot ta = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}} \quad (J) \quad \cdots\cdots\cdots(1)$$

Also, with regard to peak channel temperature Tch(peak) in the avalanche operation state, use within rating channel temperature Tch ≤ 150°C is necessary. An example of calculation of this channel temperature is given in another section.

2.2.3 Avalanche Energy Calculation Method

Figure 2.7 shows an avalanche test equivalent circuit.

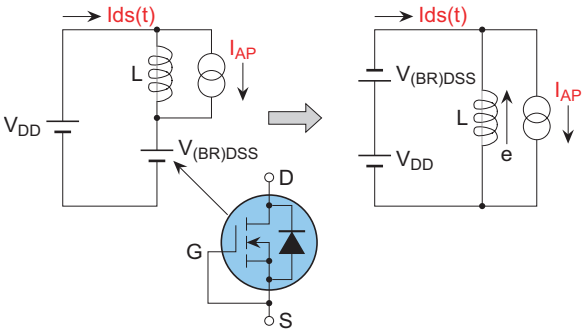


Figure 2.7 Avalanche Test Equivalent Circuit

Avalanche energy value E_{AR} in the equivalent circuit is expressed by equation (1).

$$E_{AR} = \int_0^{ta} Vds(t) \cdot Id(t)\, dt \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(1)$$

Vds(t) and Id(t) are as follows:

$$Vds(t) = V_{(BR)DSS} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(2)$$

$$Id(t) = I_{AP} - \frac{I_{AP}}{ta} t \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(3)$$

$$ta = \frac{L \cdot I_{AP}}{V_{(BR)DSS} - V_{DD}} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(4)$$

Substituting (2) and (3) in equation (1):

$$E_{AR} = \int_0^{ta} V_{(BR)DSS}\left(I_{AP} - \frac{I_{AP}}{ta} t\right)dt = \int_0^{ta}\left(V_{(BR)DSS} \cdot I_{AP} - \frac{V_{(BR)DSS} \cdot I_{AP} \cdot t}{ta}\right)dt$$

$$= \left[V_{(BR)DSS} \cdot I_{AP} \cdot t - \frac{V_{(BR)DSS} \cdot I_{AP} \cdot t^2}{2ta}\right]_0^{ta} = \frac{1}{2} \cdot V_{(BR)DSS} \cdot I_{AP} \cdot ta$$

Substituting ta of equation (4) in the above equation:

$$\therefore E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

2.2.4 Classification of Avalanche Destruction Factors

The following three factors, illustrated in figure 2.8, affect the avalanche destruction resistance value.

(1) Limitation due to drain current Id rating
(2) Limitation due to excessive channel temperature in avalanche
(3) Decline of destruction resistance due to dV/dt (figure 2.6(b))

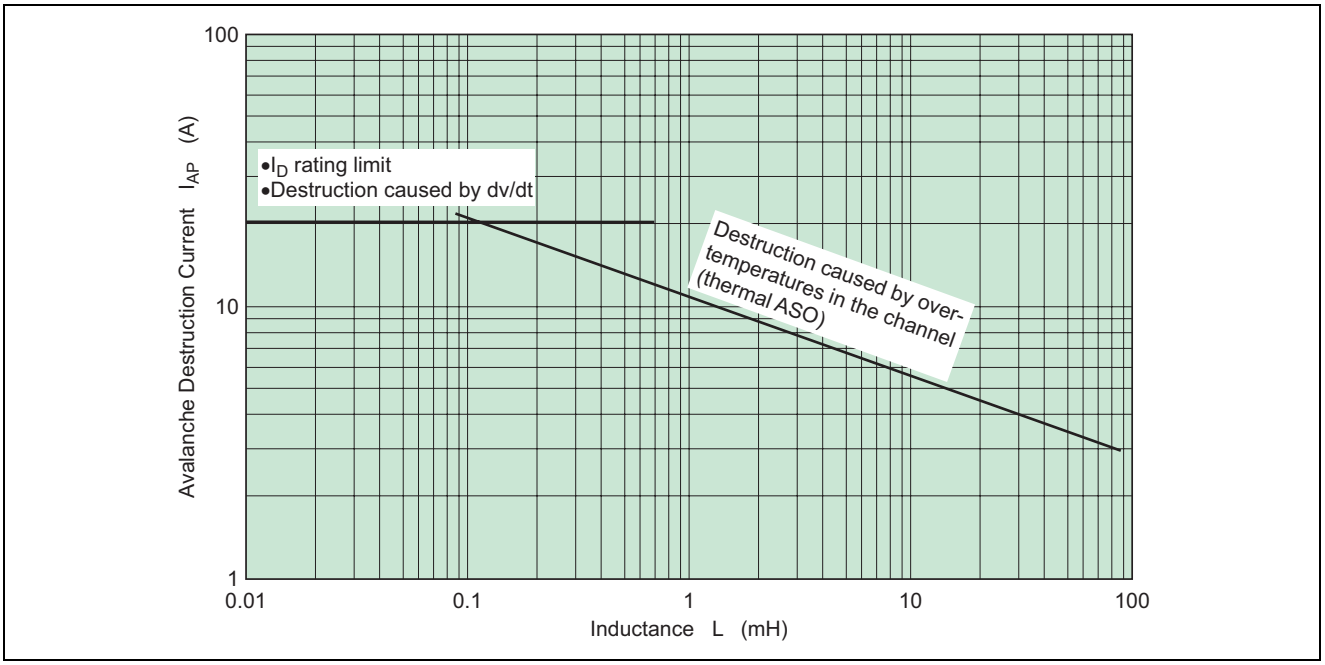


Figure 2.8 Classification of Avalanche Destruction Factors

2.2.5 Avalanche Destruction Current and Energy Value

Figures 2.9 and 2.10 show actual data show how avalanche destruction current I_{AP} and avalanche destruction energy E_{AR} vary with the inductance L value for a high-withstand-voltage 500 V class component and low-withstand-voltage 60 V class component, respectively. The graphs show that as the inductance L value increases, destruction current I_{AP} tends to fall, but the destruction energy E_{AR} value tends to increase. Therefore, to see the variations in avalanche resistance, it is necessary to consider both destruction current I_{AP} and energy value E_{AR}. In general, it can probably be stated that an component with a small inductance value L and large destruction energy value E_{AR} has good avalanche resistance.

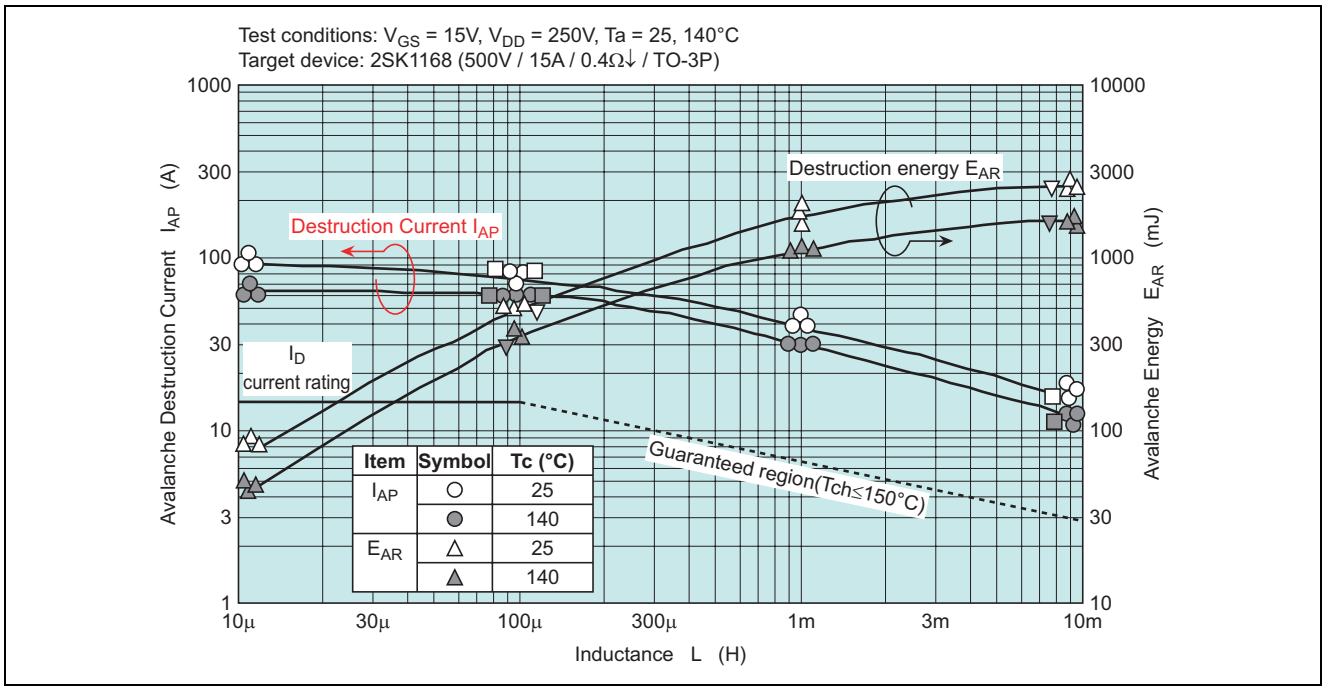


Figure 2.9 Avalanche Destruction Current and Energy Value (High Withstand Voltage)

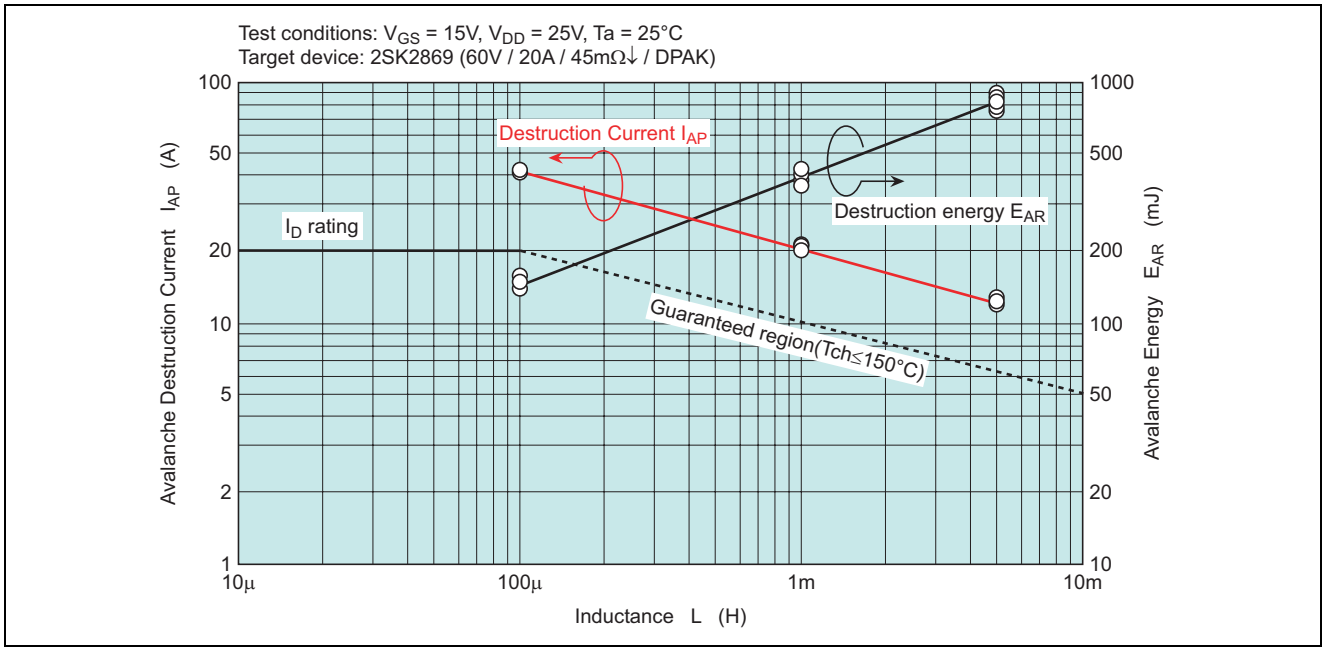


Figure 2.10 Avalanche Destruction Current and Energy Value (Low Withstand Voltage)

2.2.6 Avalanche Destruction Current and dV/dt Resistance

The third factor, the relationship between avalanche destruction resistance and dV/dt, will now be considered. Figure 2.11 shows measured values for avalanche destruction current I_{AP} dependence on dV/dt resistance. In a power MOS FET, as explained before, a parasitic bipolar transistor is formed between the drain and source in the structure shown in figure 2.4. As dV/dt is made steeper, a transient current flows through capacitance Cds, and this transistor is turned on, leading to a drop in destruction resistance. In the example in figure 2.11, the area in which dV/dt ≤ 10 V/µs can be called a safe area. This value differs according to the particular component.

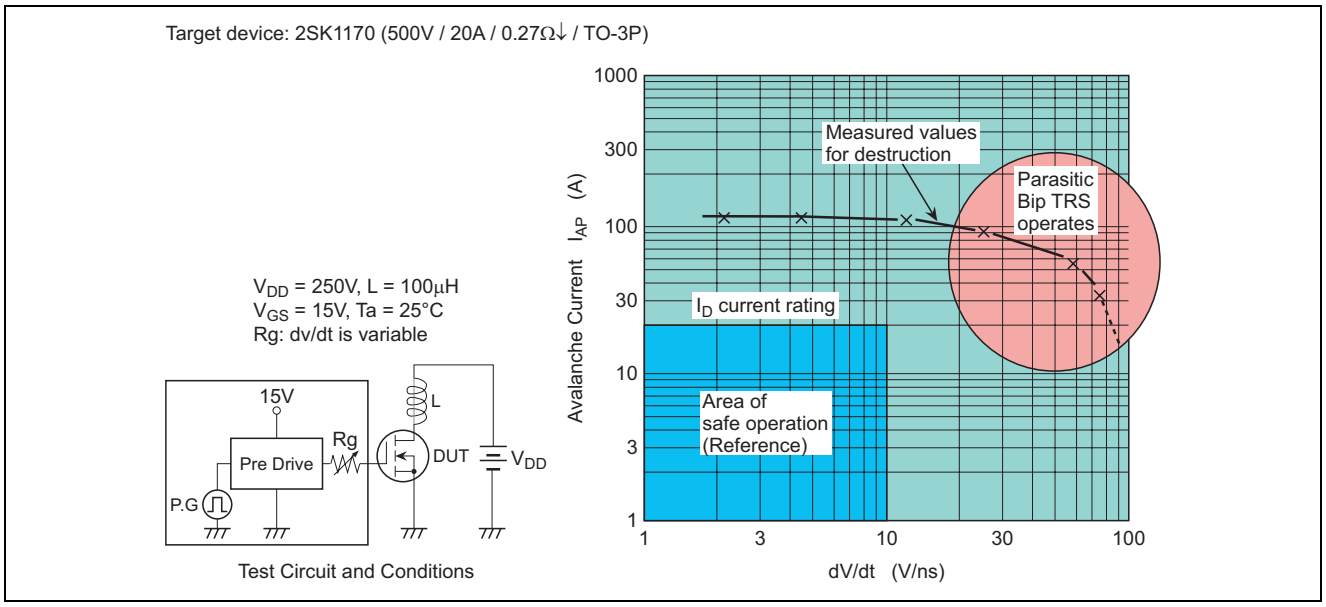
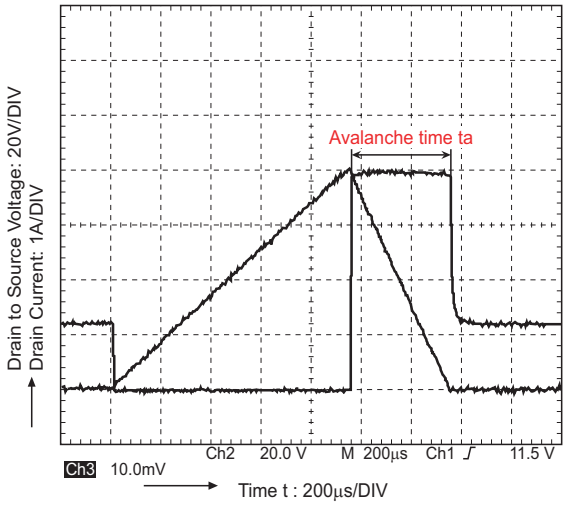


Figure 2.11 Avalanche Destruction Current and dV/dt Resistance

2.2.7 Simple Determination Method for Avalanche Resistance Guaranteed Products

A simple determination method for avalanche resistance guaranteed products is described here. The description is based on the avalanche operation waveform (1 shot period) in figure 2.12, taking the example of a 2SK2869 (60 V/20 A, 45 mΩ↓ , DPAK package) avalanche guaranteed product as the tested device.



Target device: 2SK2869
(60V / 20A / 45mΩ↓ / DPAK)
Test conditions
V_{GS} = 15V, V_{DD} = 25V, L = 5mH, Tc = 25°C, 1 shot
•Channel temperature during avalanche: Tch
Tch = T(S)ch + Pch × θch-c(t)
= 60 + 160 × 0.3336
= 113.4°C

T(S)ch: Initial channel temperature (assumed to be 60°C)
$Pch = \frac{1}{2} \times I_{AP} \times V_{(BR)DSS}$
$= \frac{1}{2} \times 4 \times 80 = 160W$
θch-c(t): ta = 400ms, 2SK2869
From the transient thermal resistance characteristics, 0.3336°C/W is obtained.

Note: 1. $I_D \leq$ Rated I_{AP} max
2. Tch ≤ Rated 150°C

Figure 2.12 Avalanche Time and Drain-Source Voltage (Drain Current)

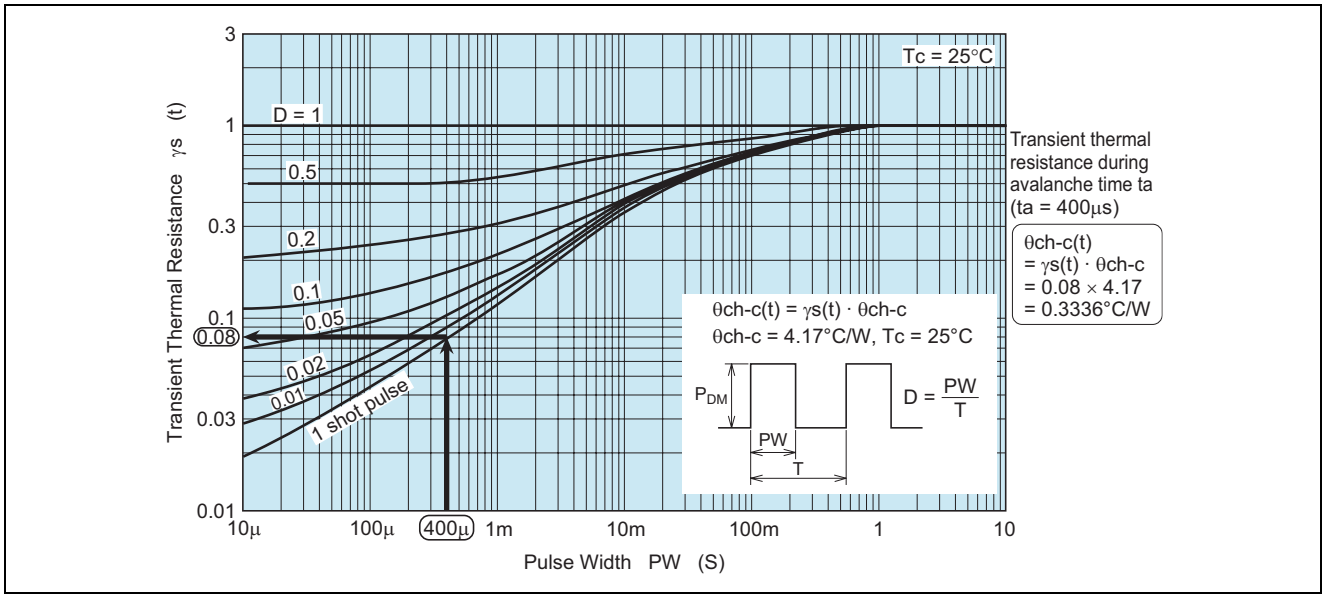


Figure 2.13 2SK2869 Transient Thermal Resistance Characteristics (Data Sheet)

Trial calculations have been carried out assuming that start channel temperature T(s)ch = 60°C before avalanche operation (due to the channel temperature rise caused by on-resistance $R_{DS(on)}$ and switching loss). For dV/dt, a range of safe operation was assumed. Therefore, the following two checkpoints should be confirmed.

(1) Whether avalanche current I_{AP} is within avalanche guarantee value current rating I_{AP}max
(For 2SK2869 avalanche guaranteed current I_{AP}, when L = 5 mH, I_{AP}max = 6.2 A (figure 2.10))
(2) Whether channel temperature Tch in avalanche operation is within the range Tchmax ≤ 150°C
First, as avalanche current I_{AP} in (1) is 4 A from the waveform, it can be confirmed that it is within avalanche rated current + I_{AP}max ≤ 6.2 A.
Next, channel temperature Tch in avalanche operation in (2) is expressed by equation (1).

$$Tch = T(s)ch + Pch \times \theta ch - c(t)$$

$$= T(s)ch + \left(\frac{1}{2} \times I_{AP} \times V_{(BR)DSS}\right) \times \theta ch - c(t) \quad \ldots\ldots\ldots\ldots (1)$$

Here, θch-c(t) is transient thermal resistance, and is calculated from the 2SK2869 data sheet transient thermal resistance characteristics in figure 2.13. θch-c(t = 400 μs) when avalanche opened time ta = 400 μs can be calculated from the graph as shown below.

$$\theta ch - c(t = 400\mu s) = \gamma(t) \times \theta ch - c$$
$$= 0.08 \times 4.17$$
$$= 0.3336°C/W$$

Therefore, substituting numeric values in equation (1) gives:

$$Tch = T(s)ch + \left(\frac{1}{2} \times I_{AP} \times V_{(BR)DSS}\right) \times \theta ch - c(t)$$

$$= 60 + \left(\frac{1}{2} \times 4 \times 80\right) \times 0.3336$$

$$= 113.4°C$$

and it can be confirmed that Tch is within the Tchmax ≤ 150°C rating.
Thus, it is determined that the value is within the avalanche guarantee range.
When more complex conditions or components are involved, individual measures should be taken.

2.2.8 Avalanche Destruction Countermeasures

Figure 2.14 shows avalanche destruction countermeasures (methods of suppressing surge voltages).

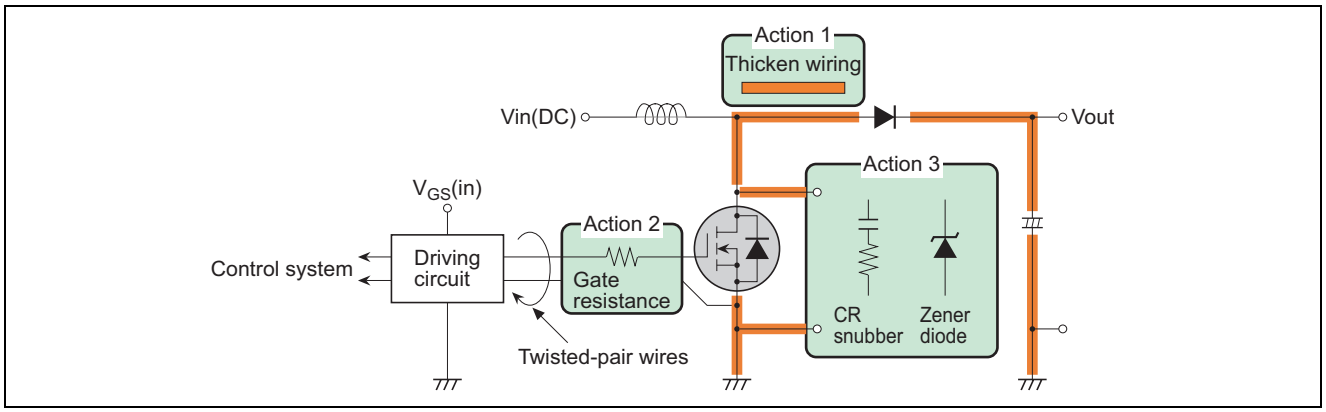


Figure 2.14 Avalanche Destruction Countermeasures

In avalanche destruction, destruction is caused by a counter voltage due to floating inductance (inductance load). As a characteristic after destruction, electrodes are shorted.
There are three countermeasures for avalanche destruction, as follows.

(1) Make large-current path wiring as short and thick as possible to reduce floating inductance.
(2) Insert a gate series resistance Rg, and suppress dV/dt. As a surge voltage occurs when switching off, surge voltages are suppressed by making the value of turn-off constant Rg large, but if the value is made too large, switching loss will increase. This should be considered when deciding on the circuit constant.
(3) Insertion of CR snubber and Zener diode
When a surge absorption snubber, etc., is inserted, the wiring should be made short and thick, and connection should be made directly to the power MOS FET drain and source terminals.

2.3 ASO Destruction (Heat Radiation Design)

2.3.1 Explanation of ASO Destruction

ASO destruction refers to a mode in which heat radiation is caused instantaneously and locally, and destruction occurs, when an overcurrent and the used voltage are applied simultaneously due to load shorting, etc., that does not occur in normal operation. It also refers to a mode in which the channel temperature rises excessively due to continuous heat radiation, thermal runaway occurs, and destruction results, when chip heat radiation is not performed properly due to thermal mismatching or a high repetition frequency.

2.3.2 ASO Destruction Countermeasures

Figure 2.15 illustrates ASO destruction and countermeasures.

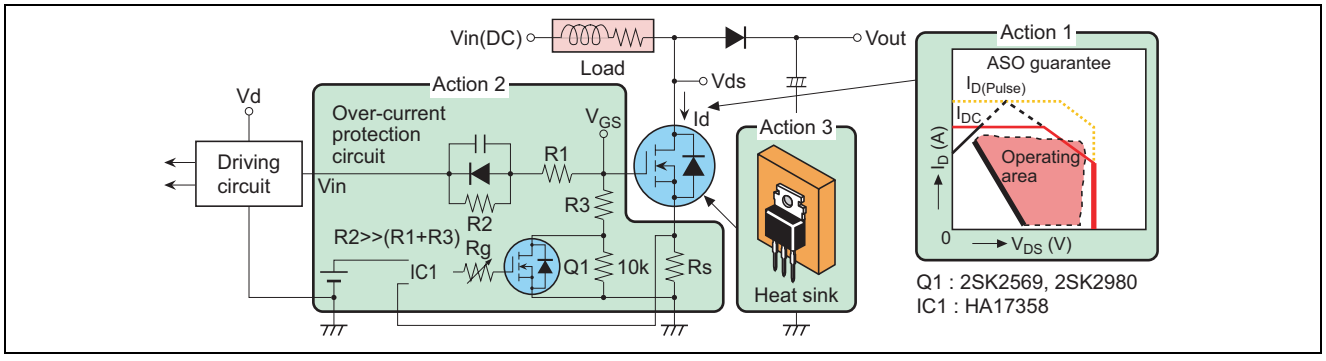


Figure 2.15 ASO Destruction (Heat Radiation Design) and Countermeasures

There are three countermeasures, as follows.

(1) Check inclusion within the forward bias ASO (Area of Safe Operation) guarantee, and that the temperature derating is adequate.

(2) If load shorting is predicted, insert an overcurrent protection circuit.
If the designed drain load current is exceeded, the voltage arose on Rs is detected, MOS FET Q1 is turned on, shorting occurs between G-S of the main power MOS FET via R3, and it is turned off. In this case the value of R3 is made larger than R1 determined as a normal switching off time constant, and is made a constant that prevents the occurrence of surge at the time of overcurrent (cutoff) protection. Alternatively, it is possible to perform cutoff control of speed at the time of cutoff in a list by means of Q1 gate resistance Rg. MOS FET gate-source drive voltage V_{GS} in normal operation is expressed by equation (1).

$$V_{GS} = Vin \times \frac{R3 + 10k\Omega}{(R3 + 10k\Omega) + (R1 + R2)} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(1)$$

V_{GS} is set to a value (V_{GS} = approx. 10 V) at which a power MOS FET operates fully in the on-resistance region. Gate retention voltage V_{GS}(cut) at the time of overcurrent cutoff is expressed by equation (2).

$$V_{GS(cut)} = Vin \times \frac{R3}{R1 + R2 + R3} \quad \cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots\cdots(2)$$

V_{GS}(cut) must be set to a value smaller than power MOS FET gate-source cutoff voltage $V_{GS(off)}$. The $V_{GS(off)}$ temperature characteristic (α = –5 mV to –7 mV/°C) is also taken into consideration.

(3) Carry out radiation design allowing a sufficient margin.
This is covered in the practical example of radiation design.

2.3.3 Forward Bias ASO (Area of Safe Operation)

Figure 2.16 shows a forward bias ASO graph (2SK3082) and the corresponding temperature derating method. (For information on an Area of Safe Operation (ASO), refer to the description of the use of power MOS FET characteristics described earlier.)

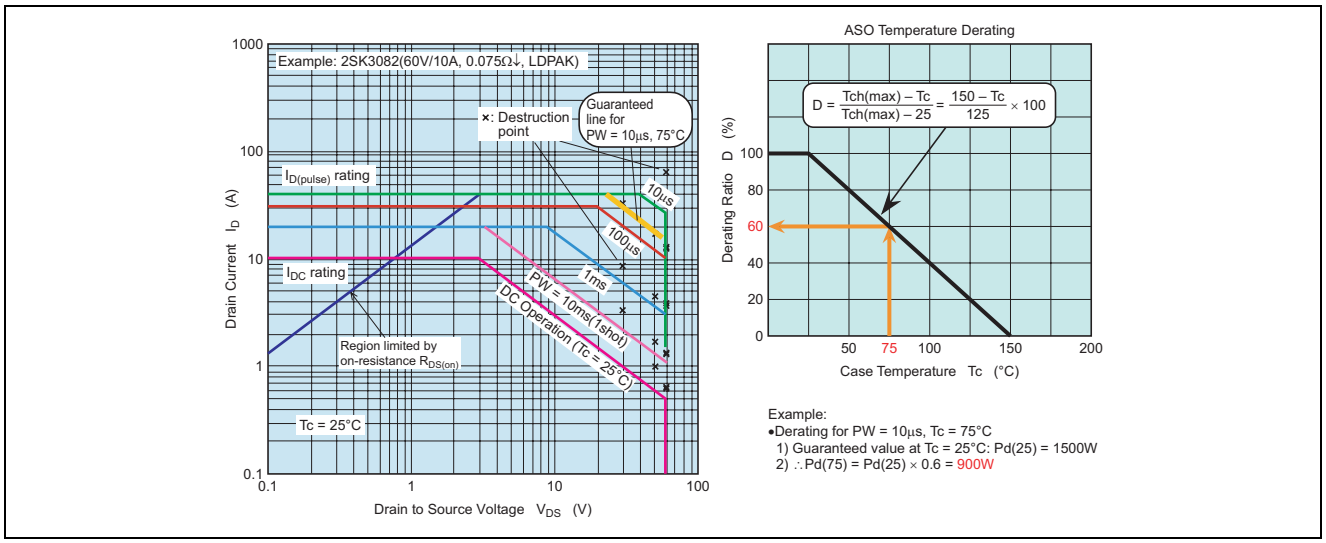


Figure 2.16 Forward Bias ASO Diagram (Area of Safe Operation)

With regard to the ASO temperature derating method, PW = 10 μs, Tc = 75°C derating will be described as an example.

First, regarding PW = 10 μs and Tc = 25°C guarantee values, this ASO diagram gives a Pd(25) = 1500 W (= Vds × I_D = 50 V × 30 A) power line. Then, as Tc = 75°C derating ratio D = 60%,

$$Pd(75) = Pd(25) \times 0.6$$
$$= 1500 \times 0.6$$
$$= 900W$$

In the ASO diagram, this is the area indicated by the PW = 10 μs, Tc = 75°C line in figure 2.16.

2.3.4 Load Shorting Resistance and Countermeasures

Figure 2.17 shows power MOS FET load shorting resistance (examples of the 2SK1518 and 2SK1522).
When a power MOS FET is used in a motor drive application, if the load should short, it is necessary to be able to withstand the conditions without breaking down until the overcurrent protection circuit operates.

1. As shown in figure 2.17, this load shorting resistance is dependent on the power supply voltage V_{DD} ($\approx V_{DS}$) used, with destruction occurring in a shorter time the greater the value of V_{DS} (as the power applied due to load shorting increases). This destruction time differs from product to product, but the overcurrent protection detection time in the event of load shorting should be set to between 1/2 and 1/3 or less of the destruction time. In the case of a power MOS FET, a setting of between 10 µs and 15 µs or less can be said to be safe.
2. Next, when load shorting occurs, as the short-circuit current an overcurrent of around 5 to 10 times the normal operation current flows, and this is cut off.
   A point to be noted here is the surge voltage that is generated when this overcurrent is cut off. This is showed as the waveform in figure 2.17. As a current considerably larger than the steady state current flows, it is necessary to set a cutoff turn-on time slower than the steady state on/off speed, and suppress the cutoff surge voltage to the component's rated voltage V_{DSS} or less.

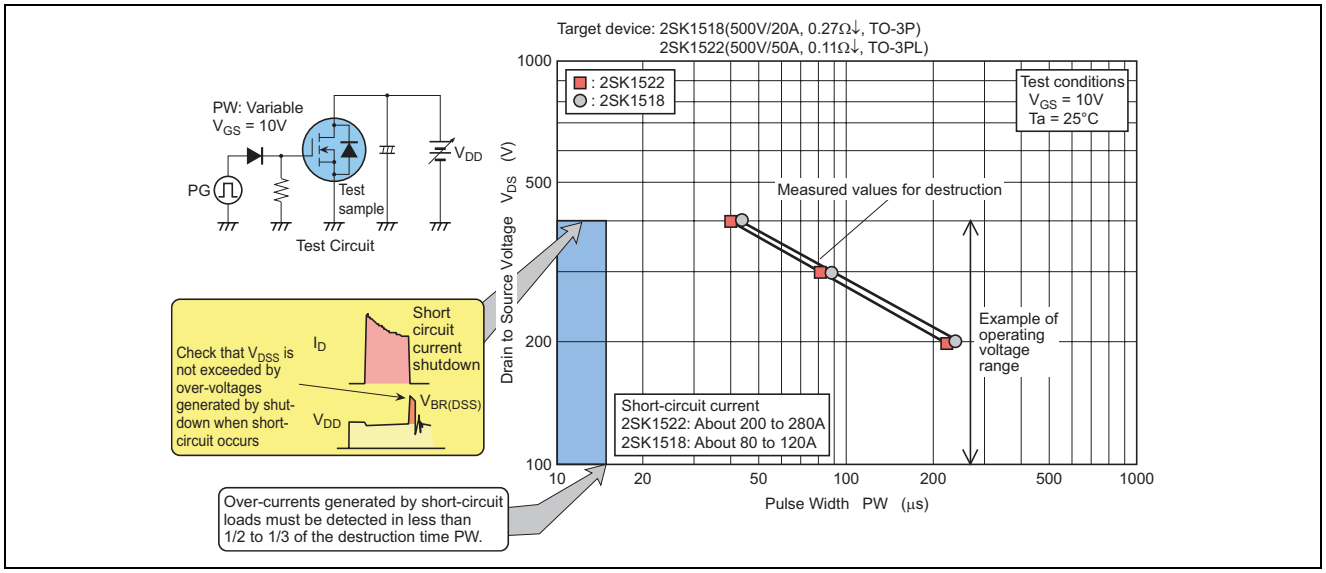


Figure 2.17 Power MOS FET Load Shorting Resistance and Countermeasures

2.3.5 Heat Radiation Design

When carrying out mounting design for power devices, it goes without saying that cooling technology — that is, how heat is to be radiated efficiently under various environmental conditions — is an important consideration, but how to perform theoretical heat calculations efficiently is also important. Examples are given here of practical heat radiation design in which the operating channel temperature of a power MOS FET can be calculated theoretically.

1. Preconditions when using a 2SK1170 (500 V/20 A, 0.27 Ω, TO-3P) are shown below.

(1) Operating conditions

— Ambient temperature Ta = 50°C
— Operating current Id = 8A, 10A (2 conditions)
— PW = 10 µs, duty = 50% max (f = 50 kHz operation)
— Switching loss P(tf) = 500 W, tf period = 0.2 µs (ton loss is omitted here)

Design target: Tch ≤ 120°C

(2) Heat sink thermal resistance θf-a: 3 kinds: (I). 0.5°C/W, (II). 1.0°C/W, (III). 1.5°C/W

(3) Mounting method: Insulating mica used, silicon grease used

$(\theta(i) + \theta(c)) = 0.8°C/W$

where θ(i): Insulating mica thermal resistance

θ(c): Contact thermal resistance

Table 2.2 Thermal Resistance of Various Transistor Packages

Thermal Resistance			Package						
			DPAK	TO-220AB	LDPAK	TO-220FM	TO-3P	TO-3PFM	TO-3PL
Rth(ch-c) (°C/W)			Rth(ch-c) = $\frac{Tj\ max - Tc}{Pch}$ (See individual catalog for Pch(W))						
Rth(c-a) *1 (°C/W)			178	80	83.3	62.5	55	42	45
(Rth(i) + Rth(c)) (°C/W)	No insulation plate	With silicon grease	0.3 to 0.6	0.3 to 0.5	0.3 to 0.5	0.4 to 0.6	0.1 to 0.2	0.3 to 0.5	0.1 to 0.2
		No silicon grease	2.0 to 2.5	1.5 to 2.0	1.5 to 2.0	1.5 to 2.0	0.5 to 0.9	1.0 to 1.5	0.4 to 0.5
	Mica insertion (t = 50 to 100μm)	With silicon grease	—	2.0 to 2.5	—	—	0.5 to 0.8	—	0.5 to 0.7
		No silicon grease	—	4.0 to 6.0	—	—	2.0 to 3.0	—	1.2 to 1.5

Note: 1. Reference value

Based on these preconditions, a design target channel temperature of Tch ≤ 120°C is set.

2. In this method, allowable power dissipation characteristics under various heat radiation conditions (1) and the power dissipation P_D characteristic according to a rise in the power MOS FET channel temperature (2) are calculated, and the point of intersection at which functions (1) and (2) overlap is taken as the channel temperature in the saturation state to be found. Results calculated on the basis of the above operating and environmental usage conditions are shown in figure 2.18.

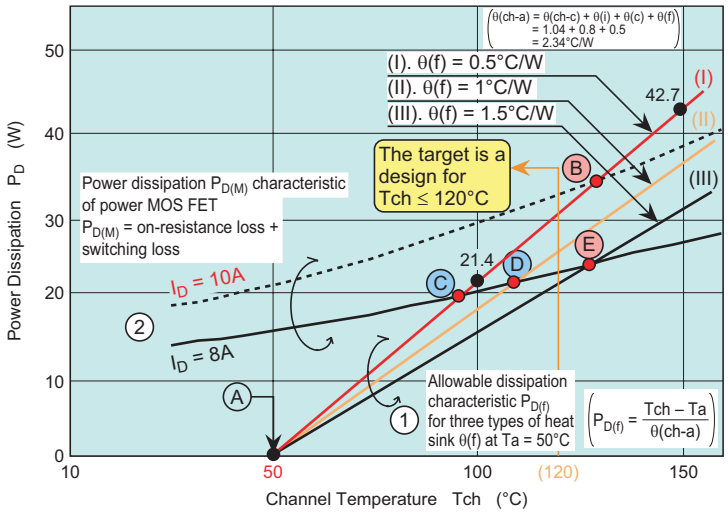


Figure 2.18 Channel Temperature Tch and Power Dissipation P_D

The procedure to reach figure 2.18 is described below.

3. With reference to the contents of the box below, allowable power dissipation characteristics under the aforementioned various heat radiation conditions (1) and the power MOS FET power dissipation characteristic (2) are calculated. In the calculation of power MOS FET power dissipation P_D, power MOS FET on-resistance temperature coefficient α (coefficient when Tch = 25°C is taken as 1.0) can be read beforehand from the Ron-Tc characteristic of the individual data sheet, and that value entered on the horizontal axis as in table 2.3. Table 2.3 shows the calculation results.

- Calculate and plot allowable power dissipation straight line $P_{D(f)}$ under each heat radiation condition ((1) in figure)
  First, find total thermal resistance θ(ch-a) under each heat radiation condition.
  $$\theta(ch\text{-}a) = \theta(ch\text{-}c) + (\theta(i) + \theta(c)) + \theta(f) \quad \ldots\ldots\ldots\ldots\ldots\ldots(1)$$
  From equation (1), θ(ch-a) when using (I) heat sink is as follows:
  θ(ch-a) = 1.04 + 0.8 + 0.5 = 2.34°C/W (Similarly for (II) = 2.84°C/W, (III) = 3.34°C/W)
  Allowable power dissipation $P_{D(f)}$ is expressed by equation (2). Three points can be used for the allowable loss curve.
  $$P_{D(f)} = \frac{Tch - Ta}{\theta(ch\text{-}a)} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots(2)$$
  Under condition (I), assuming Tch = 50, 100, 150°C gives 0W, 21.4 W, 42.7 W respectively (≈ (150 – 50)/2.34)
  Calculation can be performed for the 2 conditions (II) and (III) in the same way, and 3 straight lines plotted.
- Calculate and plot power MOS FET power dissipation curve $P_{D(M)}$ ((2) in figure)
  Power MOS FET on-resistance $R_{DS(on)}$ has a positive temperature characteristic.
  That is to say, there is a curvilinear rise (as shown in individual catalogs) as Tch rises.
  When power MOS FET total power dissipation $P_{D(M)}$ accompanying the temperature rise when I_D = 8A, 10A is found, taking this point into consideration, 2 curves can be drawn.

Table 2.3 Calculation of Power MOS FET Power Dissipation $P_{D(M)}$ (Example of 2SK1170)

Item \ Tch(°C)			25	40	60	80	100	120	140	150	Notes
$R_{DS(on)}$ temperature coefficient α for Tch = 25°C			1.0	1.09	1.27	1.5	1.73	2.0	2.27	2.41	See Ron-Tc characteristic in individual data sheet
MOS power dissipation	On-resistance loss $P_{ON} = I_D^2 \cdot R_{DS(on)max} \times \alpha \cdot \frac{t_{ON}}{T}$	I_D = 8A	8.64	9.4	11.0	13.0	14.9	17.3	19.6	20.8	Note $R_{DS(on)}$ temperature dependence
		I_D = 10A	13.5	14.7	17.1	20.3	23.4	27	30.6	32.5	
	Switching loss *1 $P_S = \frac{tf}{T} P(tf)$		5	5	5	5	5	5	5	5	Note operating frequency dependence
Total power dissipation $P_{D(M)}$ $P_{D(M)} = P_{ON} + P_S$		I_D = 8A	13.6	14.4	16.0	18.0	19.9	22.3	24.6	25.8	See separate section for detailed calculation of R, L load Ron loss, SW loss
		I_D = 10A	18.5	19.7	22.1	25.5	28.4	32.0	35.6	37.5	

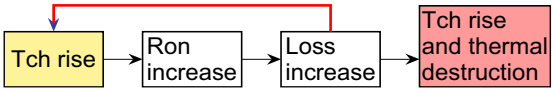
Note: 1. For the sake of simplicity, the same P_S value is used for both I_D = 8 A and 10 A.

4. In this way, the graph of channel temperature Tch vs power dissipation P_D in figure 2.18 is created.
   First, plot allowable loss characteristic (1) under each heat radiation condition.
   As ambient temperature Ta = 50°C has been assumed, taking Tch = 50°C as the zero point (as Tch = 50°C is 0 W), and individual allowable loss characteristics can be drawn for the use of 3 kinds of heat sinks. Next, power MOS FET power dissipation (at Id = 8 A, 10 A) calculated in table 4 is drawn, completing the process.

5. The way of interpreting figure 2.18 (considering the calculation results) and appropriate measures are described below.

- Considering Tch-P_D graph results
  (a) Points of intersection (B), (C), (D), and (E) represent channel temperature Tch in a state of thermal equilibrium under the respective conditions.
  That is to say, the only conditions that satisfy target design Tch ≤ 120°C are I_D = 8 A heat radiation conditions (I) and (II). (Points (C) and (D))
  (b) When point-of-intersection channel temperature Tch is 150°C or above, the maximum rating is exceeded.
  (c) Also, when both loss characteristic points of intersection are absent, as with the heat sink (III) condition, this means that thermal runaway*[1] occurs and destruction results.

Note: 1.



- Provision for design value Tch ≤ 120°C
  (a) Operating current I_D is made 8 A max and heat radiation condition (I) or (II) is applied. (Design target Tch is satisfied by (C) and (D).)
  (b) In case of use up to operating current I_D = 10 A max, the following points (combinations), etc., should be considered and a review conducted.
    1) Use a heat sink with smaller thermal resistance than (I). (Improve heat radiation conditions and lower θ(ch-a).)
    2) Lower θ(ch-c) by changing the component package. Example: TO-3P/2SK1170 → TO-3PL/2SK1629
    3) Change MOS FET to a one class higher low-on-resistance component. However, with high-speed operation (f = 100 kHz or higher), switching loss P(tf) must also be considered (as there is generally a trade-off between on-resistance Ron and switching time tf).

6. Figure 2.19 gives further information on the method of use and points for attention concerning figure 2.18. Tables 2.4 and 2.5 show power MOS FET loss calculation equations and calculation methods. Figure 2.20 show the calculation method for peak channel temperature Tch(peak) and thermal resistance θch-c(PW/T) in repeat operation.

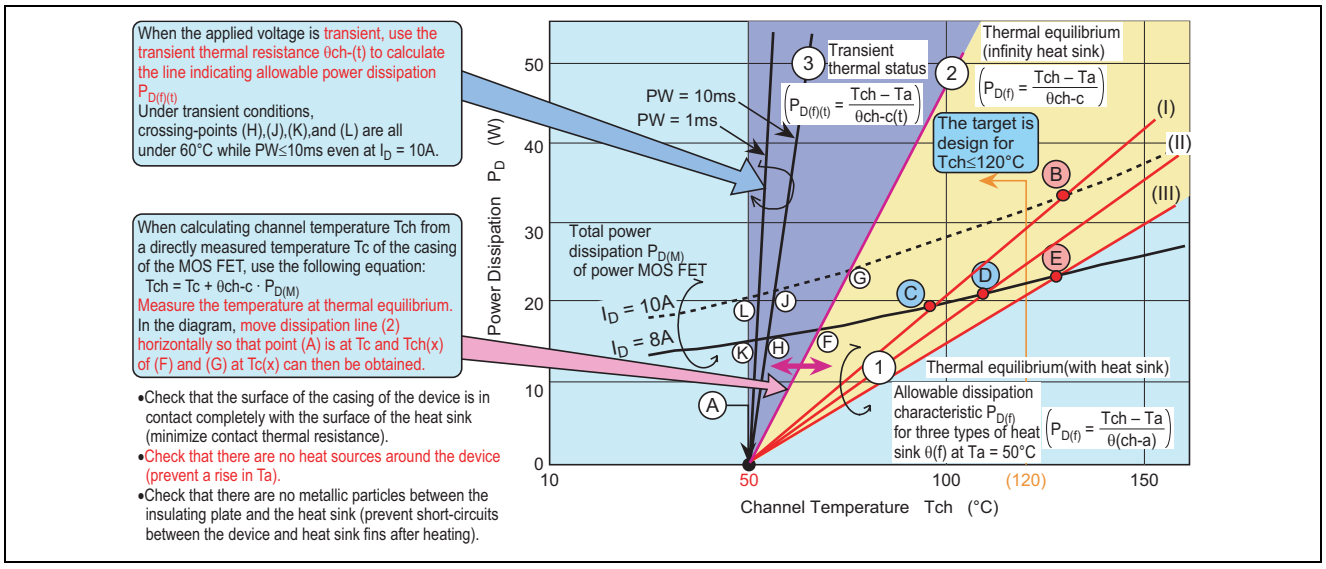
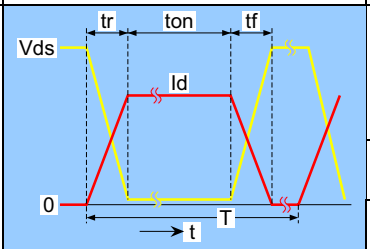
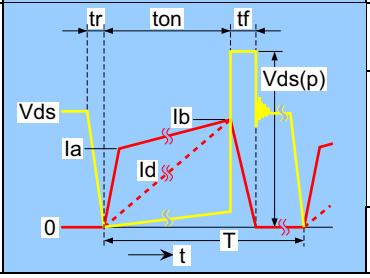


Figure 2.19 Relationship between Channel Temperature Tch and Power Dissipation P_D

(4) Power MOS FET loss calculation

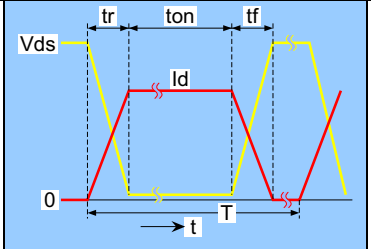
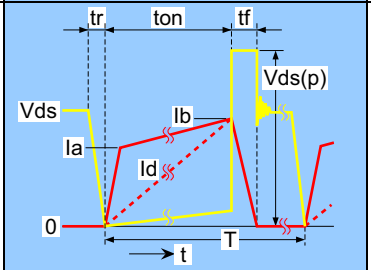
Table 2.4 Power MOS FET Loss Calculation

Category	Operating Waveform	No.	Operation Period		Average Loss Calculation
Resistance R load		1	tr period Ptr		$Ptr = \frac{1}{6}(Vds \cdot Id + 2Id^2 \cdot Ron \cdot \alpha)\frac{tr}{T}$ Smaller than term 1 and can be ignored.
		2	ton period Pton		$Pton = Id^2 \cdot Ron \cdot \alpha \cdot \frac{ton}{T}$
		3	tf period Ptf		$Ptf = \frac{1}{6}(Vds \cdot Id + 2Id^2 \cdot Ron \cdot \alpha)\frac{tf}{T}$ Smaller than term 1 and can be ignored.
Inductance L load		1	tr period Ptr		[Much smaller than item 2 or 3 and can be ignored.
		2	ton period Pton	Solid line	$Pton = \frac{1}{3}(Ia^2 + Ia \cdot Ib + Ib^2)\,Ron \cdot \alpha \frac{ton}{T}$
				Dashed line	$Pton = \frac{1}{3}Ib^2 \cdot Ron \cdot \alpha \cdot \frac{ton}{T}$
		3	tf period Ptf		$Ptf = \frac{1}{2}Vds(p) \cdot Ib \cdot \frac{tf}{T}$

Note: 1. α: Ron thermal coefficient (= T(×°C)/T (25°C))

(5) Examples of power MOS FET loss calculation (for reference)

Table 2.5 Examples of Power MOS FET Loss Calculation (for Reference)

Category	Operating Waveform	Loss Calculation (Ron thermal coefficient α omitted)
Resistance R load <u>Ptf loss during tf period</u>		$Ptf = \frac{1}{T}\int_0^{tf} Vds(t) \cdot Id(t)\,dt$ $= \frac{1}{T}\int_0^{tf}\left\{\left(\frac{Vds - Id \cdot Ron}{tf}\right)t + Id \cdot Ron\right\}\left(-\frac{Id}{tf}t + Id\right)dt$ $= \frac{1}{T}\int_0^{tf}\left\{\left(\frac{Id^2 \cdot Ron - Id \cdot Vds}{tf^2}\right)t^2 + \left(\frac{Id \cdot Vds - 2Id^2 \cdot Ron}{tf}\right)t + Id^2 \cdot Ron\right\}dt$ $= \frac{1}{T}\left[\left(\frac{Id^2 \cdot Ron - Id \cdot Vds}{3tf^2}\right)t^3 + \left(\frac{Id \cdot Vds - 2Id^2 \cdot Ron}{2tf}\right)t^2 + Id^2 \cdot Ron \cdot t\right]_0^{tf}$ $\therefore Ptf = \frac{1}{6T}tf(Vds \cdot Id + 2Id^2 \cdot Ron) \approx \frac{1}{6}Vds \cdot Id\frac{tf}{T}$
Inductance L load <u>Pton loss during ton period</u> (Current is indicated by solid line)		$Pton = \frac{1}{T}\int_0^{ton} Id^2(t) \cdot Ron\,dt$ $= \frac{1}{T}\int_0^{ton}\left(\frac{Ib - Ia}{ton}t + Ia\right)^2 \cdot Ron\,dt$ $= \frac{1}{T}\int_0^{ton}\left\{\left(\frac{Ia^2 - 2Ia \cdot Ib + Ib^2}{ton^2}\right)t^2 + 2\left(\frac{Ib - Ia}{ton}t \cdot Ia\right) + Ia^2\right\}Ron\,dt$ $= \frac{1}{T}\left[\left\{\left(\frac{Id^2 \cdot Ron - Id \cdot Vds}{3tf^2}\right)t^3 + \left(\frac{Ia \cdot Ib - Ia^2}{ton}\right)t^2 + Ia^2 \cdot t\right\}Ron\right]_0^{ton}$ $\therefore Pton = \frac{1}{3}(Ia^2 + Ia \cdot Ib + Ib^2)\,Ron\frac{ton}{T}$

(6) Repetition frequency Tch(peak), thermal resistance θch-c(PW/T)

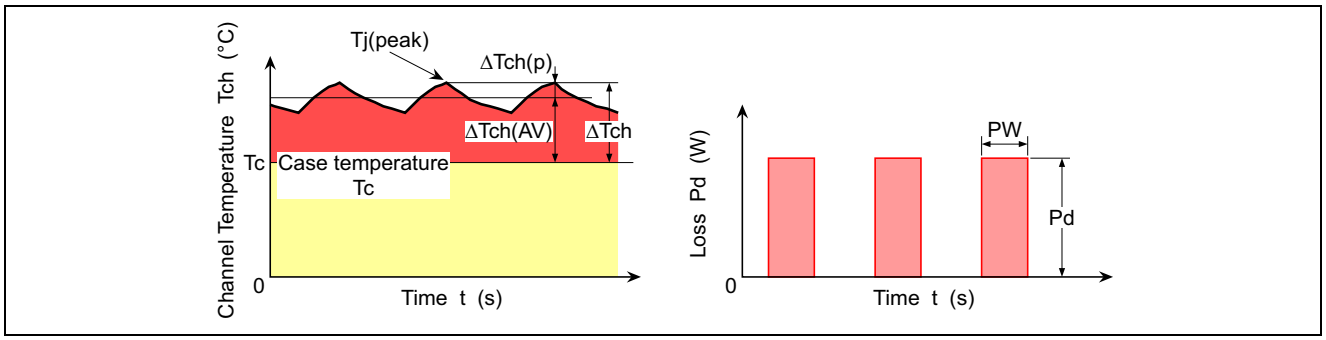


Figure 2.20 Repetition Frequency Tch(peak), Thermal Resistance θch-c(PW/T)

$$Tch(peak) = Tc + \Delta Tch = Tc + Pd\left\{\frac{PW}{T}\,\theta ch\text{-}c + \left(1 - \frac{PW}{T}\right)\theta ch\text{-}c^{(PW)}\right\} \quad \ldots\ldots\ldots\ldots\ldots(1)$$

$$\theta ch\text{-}c\left(\frac{PW}{T}\right) = \frac{Tch(peak) - Tc}{Pd} = \frac{\Delta Tch}{Pd} \quad \ldots\ldots\ldots\ldots\ldots(2)$$

From equations (1) and (2):

$$\theta ch\text{-}c\left(\frac{PW}{T}\right) = \theta ch\text{-}c\left\{\frac{PW}{T} + \left(1 - \frac{PW}{T}\right)\frac{\theta ch\text{-}c^{(PW)}}{\theta ch\text{-}c}\right\} \quad \ldots\ldots\ldots\ldots\ldots(3)$$

Normalized transient thermal resistance $\gamma s^{(PW)} = \dfrac{\theta ch\text{-}c^{(PW)}}{\theta ch\text{-}c}$ $\ldots\ldots\ldots\ldots\ldots(4)$

Repetition ducy cycle $n(\%) = \dfrac{PW}{T} \times 100$ $\ldots\ldots\ldots\ldots\ldots(5)$

From equations (4) and (5), thermal resistance $\theta ch\text{-}c^{(PW/T)}$ for a pulse of width t = PW and perioed of one repetition T is given by equation (6):

$$\theta ch\text{-}c\left(\frac{PW}{T}\right) = \theta ch\text{-}c\left\{\frac{n}{100} + \left(1 - \frac{n}{100}\right)\gamma s^{(PW)}\right\} \quad \ldots\ldots\ldots\ldots\ldots(6)$$

Here, θch-c is a dc thermal resistance.

2.4 Internal Diode Destruction

2.4.1 Explanation of Internal Diode Destruction

Internal diode destruction is a destruction mode that occurs when the parasitic diode between the drain and source of a power MOS FET is used actively. It is limited to use in DC/AC inverters utilized in motor control, uninterruptible power supply (UPS), and similar H bridge circuits.

Internal diode destruction occurs only in the above uses, and applies especially to components with a withstand voltage of 250 V or above used at high voltages, but in recent years the destruction mechanism has been clarified, and component diode destruction resistance has been improved. With most 250 to 600 V high-withstand-voltage AP3-H, AP3-HF (internal high-speed diode), and AP4-H series products, destruction countermeasures are incorporated into the component design. From an application standpoint, the AP3-H and AP5-HF series are recommended for these uses. With components with a low withstand voltage of 100 V or below, this destruction problem almost never occurs as the voltage used is also low.

Figure 2.21 shows an inverter circuit using general power MOS FETs and the power MOS FET operation waveform in a full bridge circuit. In this circuit, Q1 and Q4 operate and PWM control is performed by the Q1 component. Q4 is always on during the Q1 PWM control period.
When Q1 current I_{D1} flows and is then turned off, motor inductance L regenerative current I_F flows through the Q2 internal diode. When Q1 is turned on again in this state, due to the influence of Q2 internal diode reverse recovery time trr, in this period Q1 and Q2 enter the conduction state, short-circuit current irr flows and recovers, and at the same time the internal diode voltage (V_{DS}) also recovers.

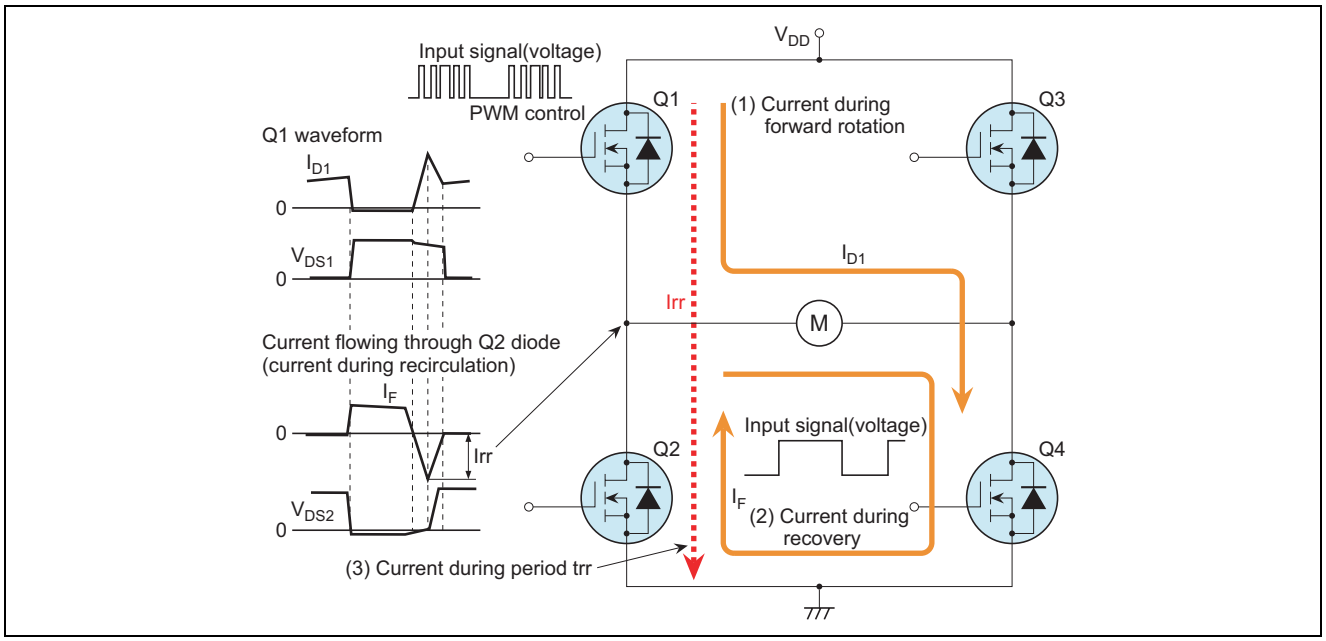


Figure 2.21 Power MOS FET Operation in Full Bridge

Figure 2.22 shows the structure and equivalent circuit of a power MOS FET. As shown in this figure, an internal diode is formed between the source and drain structurally, and is also called a parasitic diode.

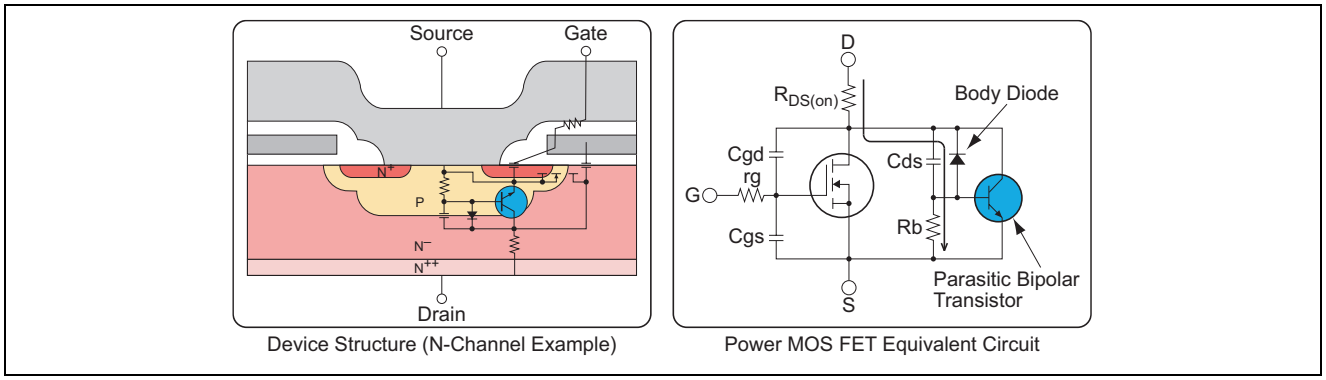


Figure 2.22 Power MOS FET Component Structure and Equivalent Circuit

Figure 2.23 shows the internal diode destruction mechanism.
As stated earlier, internal diode destruction resistance has improved considerably, and structural measures have been taken to inhibit parasitic bipolar transistor operation, so that the problem of destruction almost never occurs during normal use.

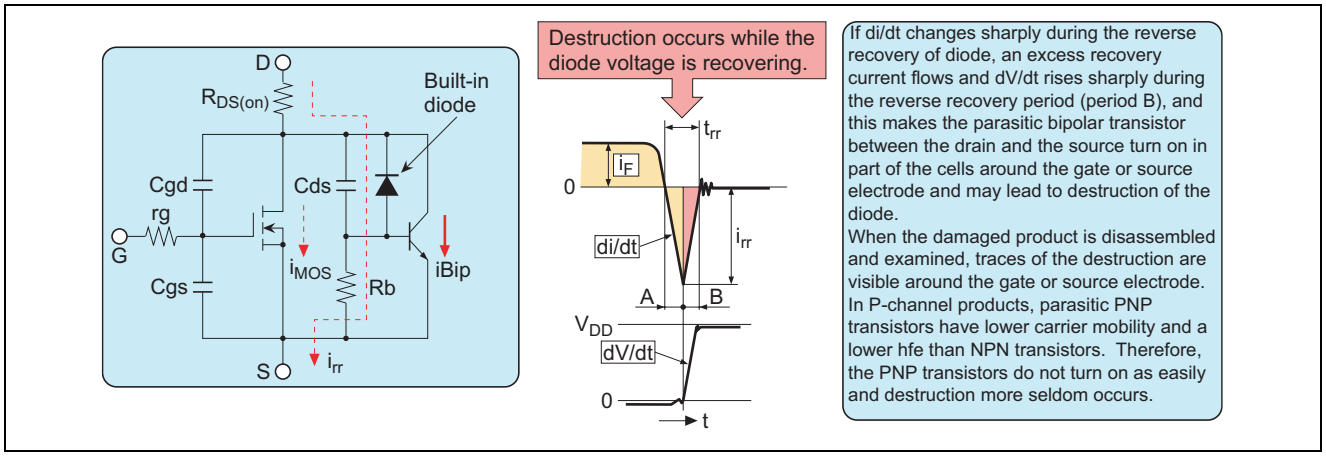


Figure 2.23 Internal Diode Destruction Mechanism

2.4.2 Example of Internal Diode Destruction Circuit Countermeasures

Figure 2.24 shows examples of internal diode destruction circuit countermeasures (usage precautions).

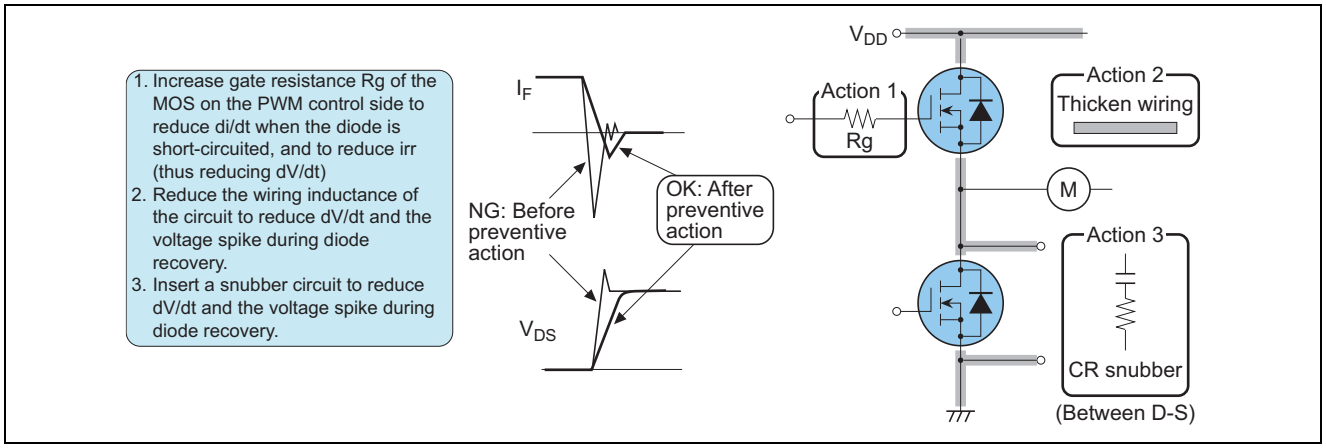
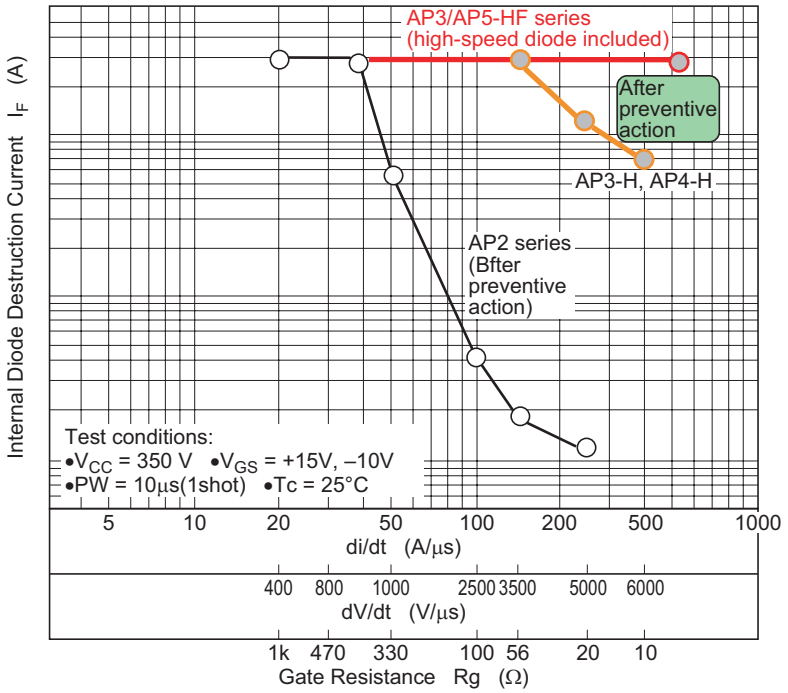


Figure 2.24 Examples of Internal Diode Destruction Circuit Countermeasures

Figure 2.25 shows actual data before and after countermeasures for internal diode destruction resistance of 500 V high-withstand-voltage components (now discontinued).



Note: The relationship between gate resistance Rg and di/dt or dV/dt depends on the voltage used and the wiring inductance of the application system. Check the waveform in the actual application.

Figure 2.25 Internal Diode Destruction Resistance (500 V/10 A Class Examples)

2.5 Destruction Due to Parasitic Oscillation

2.5.1 Explanation of Destruction Due to Parasitic Oscillation

Gate parasitic oscillation mainly occurs when power MOS FETs are connected in parallel and are directly connected without inserting a gate resistance. This parasitic oscillation occurs in a resonant circuit formed by gate-drain capacitance Cgd(Crss) and gate lead inductance Lg when the drain-source voltage is turned on and off at high speed. When the resonance condition ($\omega L = 1/\omega C$) occurs, an oscillation voltage much larger than drive voltage Vgs(in) is generated in Vgs between the gate and source, as a result of which gate destruction occurs due to a voltage exceeding the gate-source rated voltage, or the oscillation voltage when the drain-source voltage is turned on and off is superimposed on the Vgs waveform via gate-drain capacitance Cgd and positive feedback occurs, leading to oscillation destruction due to mal operation.

2.5.2 Power MOS FET Parasitic Oscillation Mechanism

Figure 2.26 shows a parallel equivalent circuit.

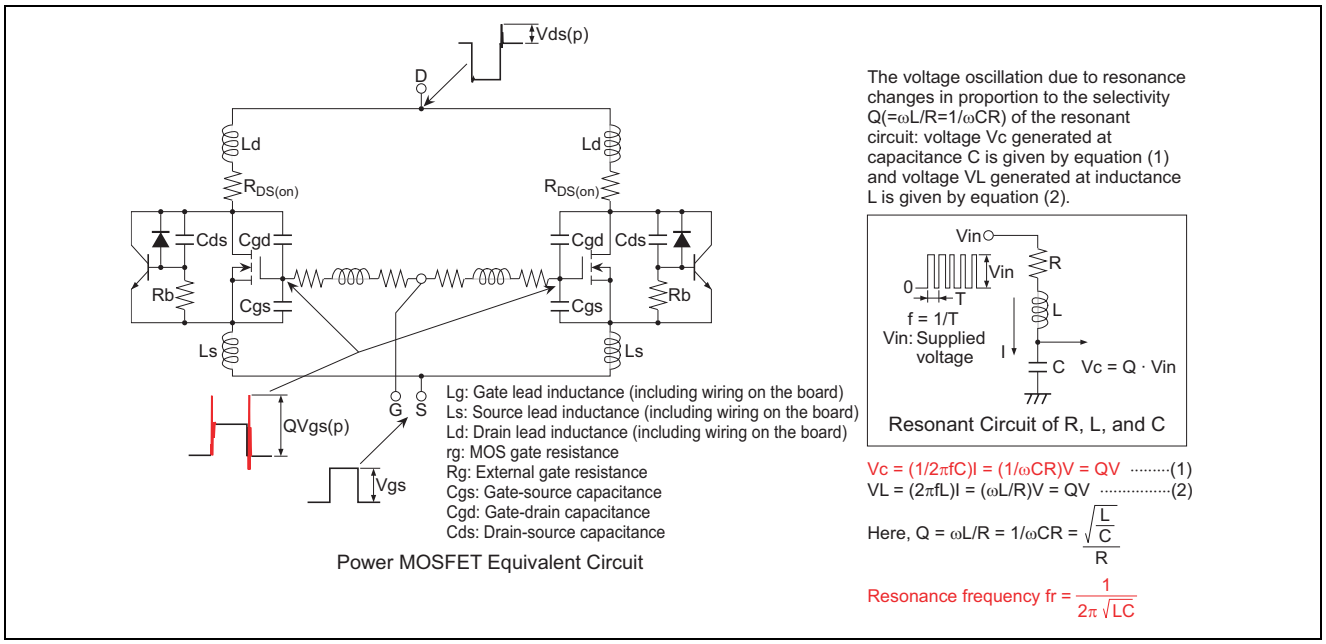


Figure 2.25 Power MOS FET Parasitic Oscillation Mechanism

When power MOS FET parallel connection is performed by means of direct connection without using a gate series resistance, a parasitic oscillation waveform appears in the gate. With this parasitic oscillation, oscillation voltage Vds(p) passes through gate-drain capacitance Cgd(Crss) due to load wiring inductance Ld when the drain-source voltage is turned on and off at high speed, and particularly when it is turned off, and a resonant circuit with gate lead inductance Lg is formed. As gate internal resistance rg of a large-current, high-speed power MOS FET is extremely small, at 1 to 2 Ω, when there is no gate external resistance Rg, oscillation circuit Q — that is $\sqrt{L/C}/R$ — becomes large, and when the resonance condition occurs, a large oscillation voltage is generated between that point and Cgd(Crss) or Lg (that is to say, between the MOS gate and source), and parasitic oscillation is caused.

In particular, as large-current operation is performed in the case of parallel connection, if transient current balance becomes poor when switching off, all the currents flow in one MOS FET in a period with deviation of this timing. Generally, this period is an extremely short time of several ns to several tens of ns, and therefore power MOS FET thermal stress is not a problem, but drain-source oscillation voltage Vds(p) may be logically n times greater than this or more (as Ld also appears to be larger due to the skin effect* since a high-frequency large current actually flows in a transition).

Skin effect: Phenomenon whereby a high-frequency current flows only through the surface of a conductor, and not through the inner part. When current flows in a conductor, a magnetic flux is generated around the current, and as this crossing with the current, an inductance effect is produced. When a current is passed through a thick conductor that handles large currents, a magnetic flux is also generated in the conductor, and therefore the inductance effect is more intense toward the center of the conductor. Consequently, when a high-frequency current flows in a thick conductor, there is a strong inductance effect in the central part, making it difficult for current to pass through, and current deviates toward the surface of the conductor. In this case, the cross-sectional area through which the current flows is reduced, and thus viewed from outside, electrical resistance — that is, inductance — appears to be large.

Figure 2.27 shows parasitic oscillation and destruction countermeasures in the case of parallel connection.

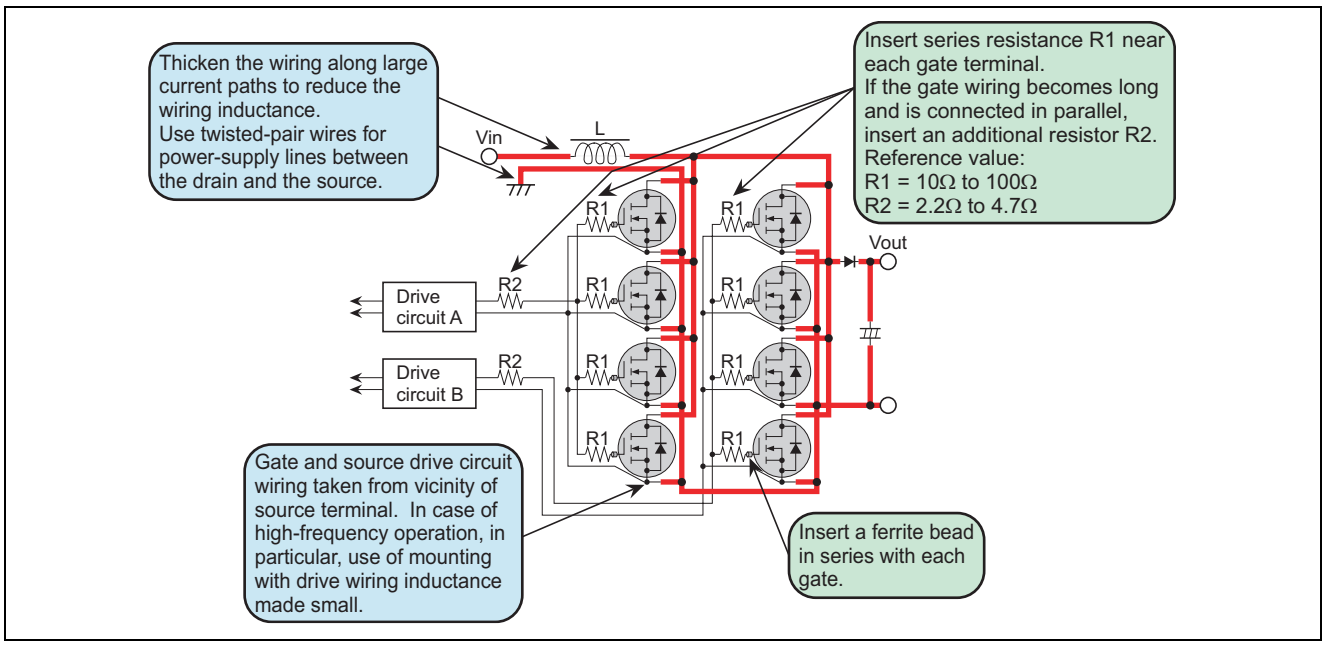


Figure 2.27 Parasitic Oscillation Reduction and Destruction Countermeasures

2.6 Notes on Parallel Connection

Notes on mounting covering precautions concerning parallel connection, and advice on the selection and use of power MOS FET components, are given below.

2.6.1 Notes on Mounting

- Low-inductance wiring
- Make drain and source wiring lengths equal, and use twisted-pair wiring, etc.
- Pay attention to parasitic oscillation (see attachment on parasitic oscillation countermeasures)

2.6.2 Advice on Selection and Use of Power MOS FETs

Discussion and agreement with the semiconductor manufacturer are necessary.

Align Vth($V_{GS(off)}$) value (higher value preferable)	⇒	Off-time transient current balance reduction
Align on-resistance $R_{DS(on)}$	⇒	On current balance reduction
Apply adequate gate drive voltage (4 V drive product: V_{GS} = 5 to 10 V, 10 V drive product: V_{GS} = 10 to 12 V)	⇒	Heat radiation balance reduction
Avoid avalanche operation as far as possible	⇒	Current concentration in low-withstand-voltage components

2.7 Electrostatic Destruction

2.7.1 Explanation of Electrostatic Destruction

Electrostatic destruction refers to destruction due to static electricity or a surge voltage from a human body or equipment when a product is handled or is being mounted.

2.7.2 Electrostatic Destruction Countermeasures

Figure 2.28 shows countermeasures against electrostatic destruction.

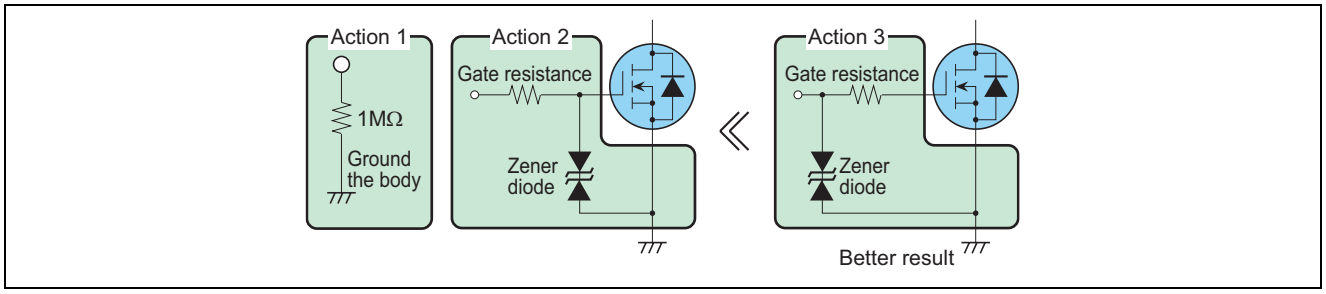


Figure 2.28 Electrostatic Destruction Countermeasures

In electrostatic destruction, the gate oxide film is destroyed when static electricity or a surge voltage generated by a human body, mounting equipment, etc., is applied to a gate. Characteristics seen after destruction are a voltage drop or shorting between the gate and source, shorting between the drain and source, or increased leakage current. (See figure 2.29.)

The following three methods are used as countermeasures to electrostatic destruction.

(1) Earth human bodies via a 1 MΩ resistance before handling devices.
(2) Ensure that equipment is properly earthed.
(3) To prevent the application of gate surge voltages that may occur after board mounting, insert a gate resistance and Zener diode.

2.7.3 Destruction Progression Modes after Electrostatic Destruction

In figure 2.29, post-gate-destruction characteristic modes are broadly classified into two kinds, and their respective natures are illustrated if the respective destruction products maybe adopted to a set circuit.

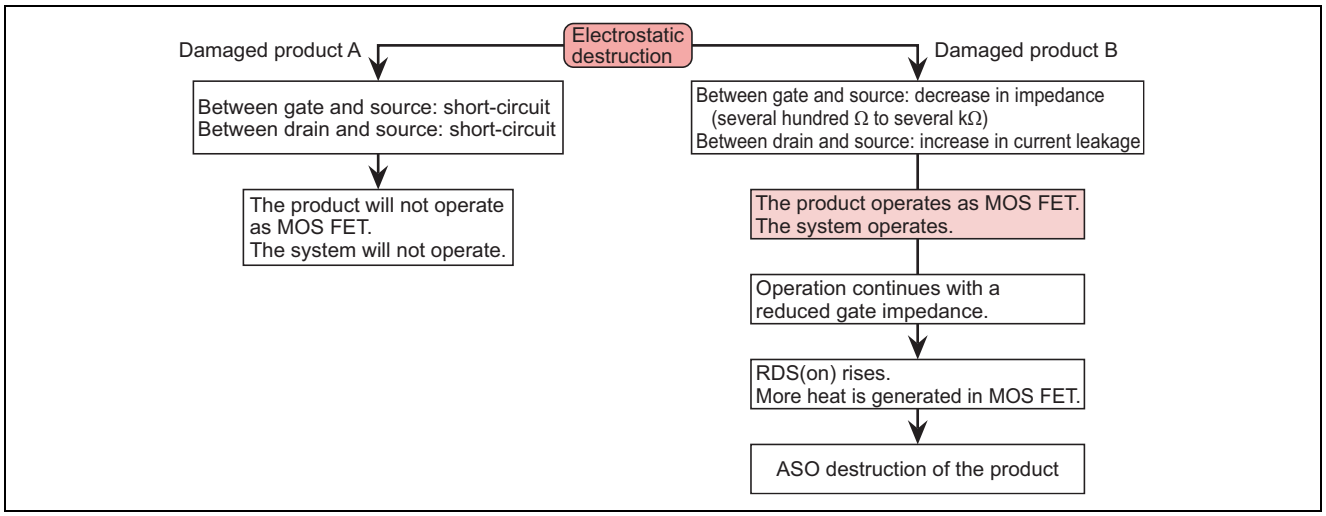


Figure 2.29 Destruction Progression Modes after Electrostatic Destruction

Figure 2.30 illustrates the characteristic modes of destruction products A and B. In the destruction product A mode, there is almost complete shorting between the gate and source and between the drain and source. In the destruction product B mode, although a certain level of resistance (several tens of Ω or more) is maintained between the gate and source, and a curve shape of standing to reverse voltage is keeping although leakage current I_{DSS} between the drain and source is large at several hundred mA to several tens of mA.

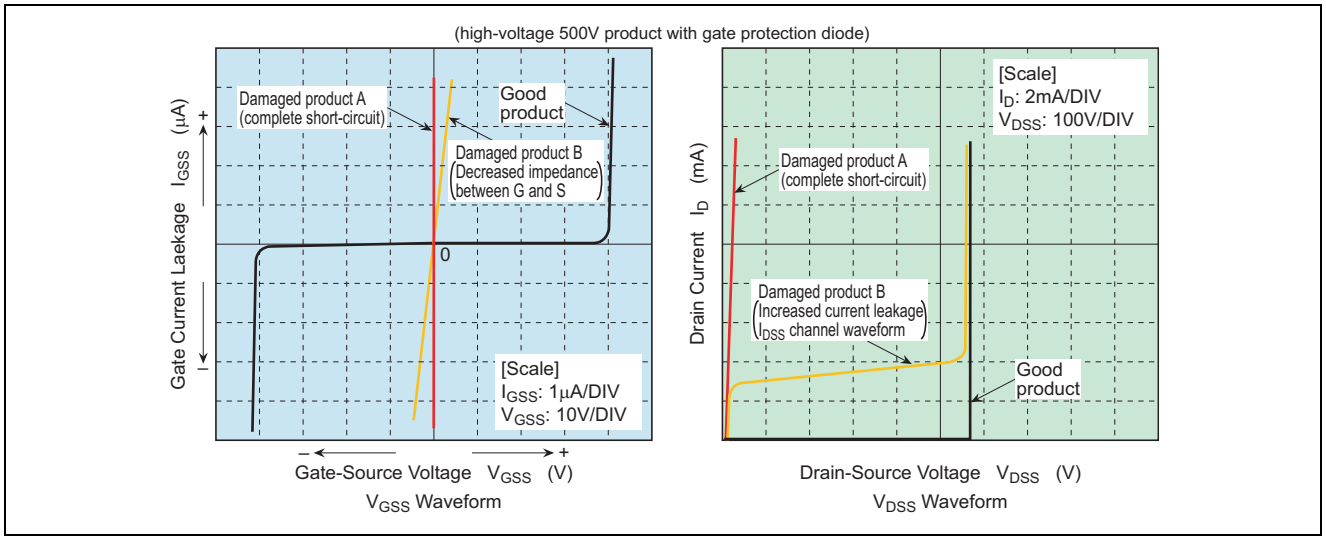


Figure 2.30 Sample Electrostatic Destruction Product V_{GSS} and V_{DSS} Waveforms

2.7.4 Mechanism whereby Gate Destruction Product B Come to ASO Destruction

When the destruction product A mode is temporarily incorporated in a set circuit, the circuit naturally does not operate, a short-circuit current flows between the MOS FET gate and source when power is turned on, and destruction traces increase.

When a mode such as the destruction product B mode is temporarily adopted to a set circuit, since drain-source withstand voltage is maintained (although when leakage current I_{DSS} is large, power consumption increases in the off state and causes a rise in component temperature), according to the circuit gate signal source resistance R_S constant and gate-source resistance R_{GS} immediately after destruction, a voltage with drive capability is applied between the gate and source, so that although drive voltage V_{GS} appears to fall, switching operation is performed. This state is illustrated in figure 2.31.

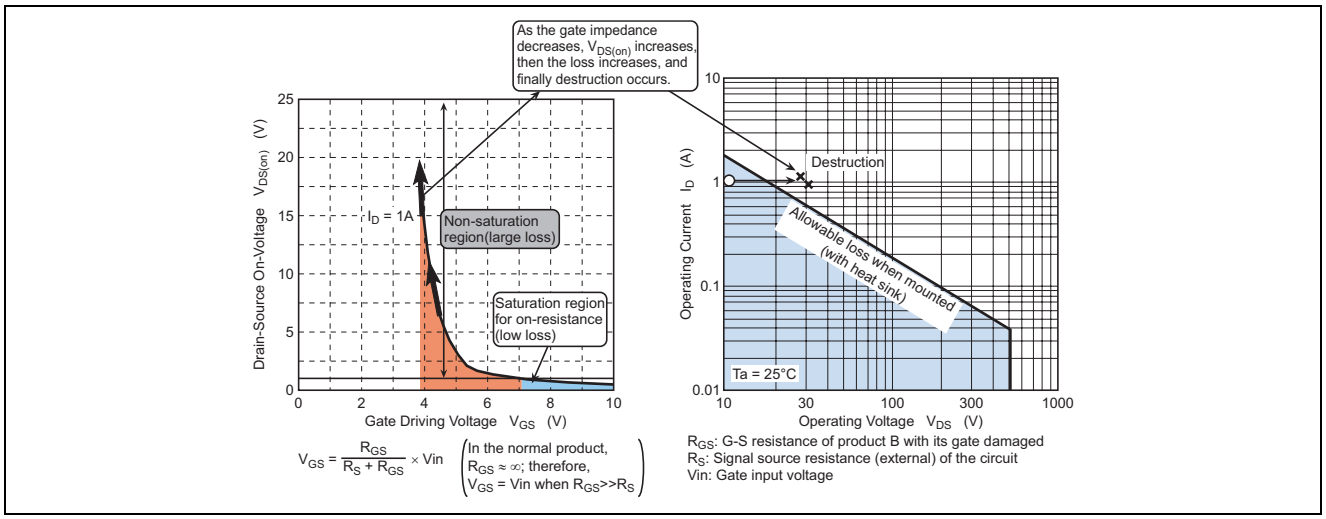


Figure 2.31 Mechanism whereby Gate Destruction Product B Reaches ASO Destruction

When, for example, a destroyed product B mode gate destruction sample with gate-source resistance value R_{GS} = 100 Ω immediately after gate destruction and drain-source leakage current I_{DSS} = 1 mA is temporarily incorporated in an operating circuit with power supply voltage V_{DD} = 24 V, gate input voltage Vin = 10 V, gate signal source resistance R_S = 22 Ω, and on-duty D = 0.3, when the actual gate drive voltage V_{GS} and off-time power consumption Poff of this component are calculated, V_{GS} = 8.2 V and Poff = 16.8 mW as shown below, and generally, in the case of a logic-level drive component, the component operates adequately.

$$V_{GS} = \frac{R_{GS}}{R_S + R_{GS}} \times Vin = \frac{100}{22 + 100} \times 10 \approx 8.2V$$

$$Poff = V_{DD} \times I_{DSS} \times (1 - D) = 24 \times 1 \times 10^{-3} \times 0.7 = 16.8mW$$

However, as gate-source resistance value R_{GS} of this destroyed product may well decrease further, in that process gate drive voltage V_{GS} becomes insufficient. As a result, on-resistance increases (a complete on-resistance operation on-state is not established, and operation is performed in a state in which $V_{DS(on)}$ has increased as shown in figure 2.31), and power consumption increases, and eventually component ASO destruction occurs.

In a case such as this, subsequent analysis of the destroyed product shows a close resemblance to thermal destruction due to exceeding of the component ASO, but it is possible that the destruction mode constituting the initial trigger was a gate destruction mode. However, it is extremely difficult to determine whether it is the latter case or not by destroyed product because destruction traces have increased.
Therefore, at the very least, care must be taken in handling (including component measurement) up to embedding in a circuit.

2.8 Usage Notes

2.8.1 Power MOS FET Main Loss Frequency Dependence and Relationship to Main Characteristics

Figure 3.32 shows “power MOS FET main loss frequency dependence and relationship to main characteristics” in the case of use in a DC-DC converter.

Switching loss and drive loss increase at higher frequencies.

In order to make full use of component performance and reduce total loss, it is necessary to achieve a balance with on-resistance loss by appropriately setting and controlling the gate drive voltage in the high-frequency region.

In general, when a logic-level drive component is operated at operating frequency f = 200 to 300 kHz or below, in order to minimize on-resistance, applying a gate drive voltage V_{GS} of around 10 V is effective from a total loss standpoint. Applying a higher voltage (for example, V_{GS} = 15 to 17 V) is not really recommendable as drive loss only increases.

At high-frequency operation of f = 500 kHz or more, reducing total loss by optimization in a gate drive voltage V_{GS} range of 5 to 8 V is effective in achieving higher efficiency.

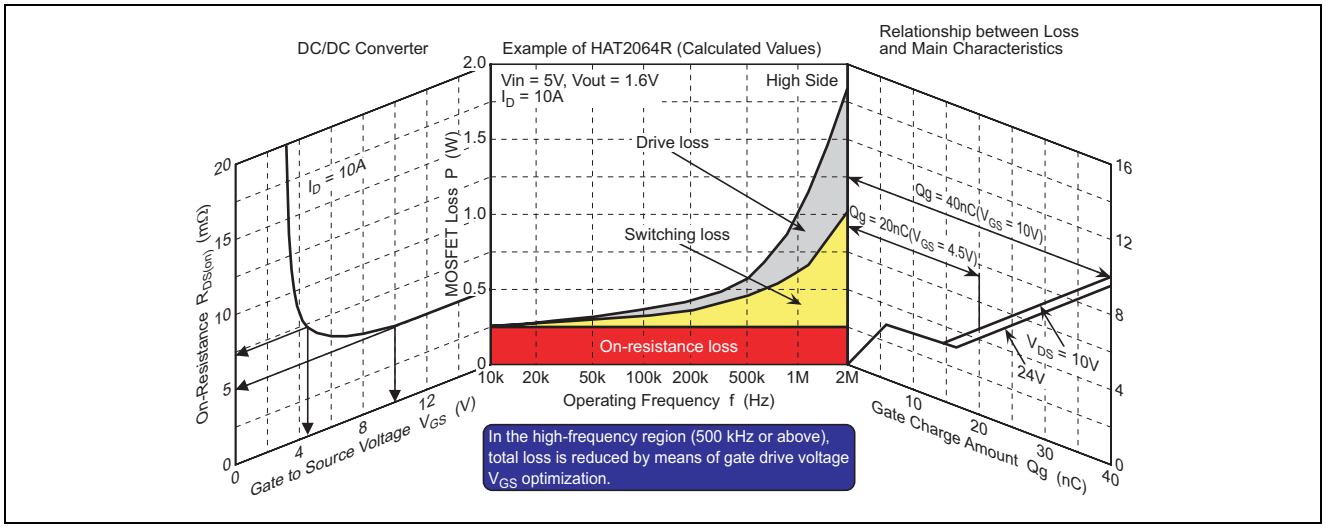


Figure 2.32 Power MOS FET Main Loss Frequency Dependence and Relationship to Main Characteristics

2.8.2 Malfunction (Arm Shorting) Countermeasures in Motor Application

Figure 2.33 illustrates arm shorting in a small motor drive application, and applicable countermeasures, when P-channel and N-channel MOS FETs are used in combination.

This figure shows the upper P-channel MOS FET in the off state and the lower N-channel MOS FET in a chopping operating state.

In figure 2.33, the voltage waveform at point A is as shown in the figure, but as the lower N-channel MOS FET is now turned on and V_{DD} changes to 0 V, a charge current flows transiently via Crss and Ciss of the upper P-channel MOS FET, and a $\Delta V_{GS(t)} = \{Crss/(Ciss+Crss)\}\Delta V_{DS(t)}$ peak voltage is generated between the gate and source. When this $\Delta V_{GS(t)}$ peak voltage exceeds Vth of the P-channel MOS FET, the upper and lower components go to the on state simultaneously, an arm short-circuit current flows, and excessively large loss is caused.

In the case of use in an H bridge circuit, the other arm is also similarly susceptible to the occurrence of this phenomenon with an N-channel component.

The upper/lower component shorting phenomenon at the time of this transition is liable to occur under the following conditions.

1. More likely to occur the faster the switching operation (especially turn-on time) and the steeper dV/dt
2. More likely to occur the larger signal source resistance R_G (gate off-time constant)
3. More likely to occur the larger the Crss/Ciss values of the components used (K_S = {Crss/(Ciss+Crss)} · V_{DD} is a larger value than Vth of the component)
4. More likely to occur the higher power supply voltage V_{DD}

Of items 1 to 4, item 4, power supply voltage V_{DD} is determined by the application and cannot be changed, so countermeasures are shown for remaining items 1 to 3.

1. Slow the turn-on time to suppress dV/dt (make gate resistance R1 in the figure larger).
2. Make gate off-time signal source resistance R_G (MOS FET driver signal source resistance R_S and off-time external resistance constant Rg) smaller, and set low impedance between the gate and source.
3. Insert capacitance C1 between the gate and source, make (K_S = {Crss/(Ciss+C1+Crss)}V_{DD} smaller, and provide a margin.
   Also, select an component with a small K_S and high Vth.

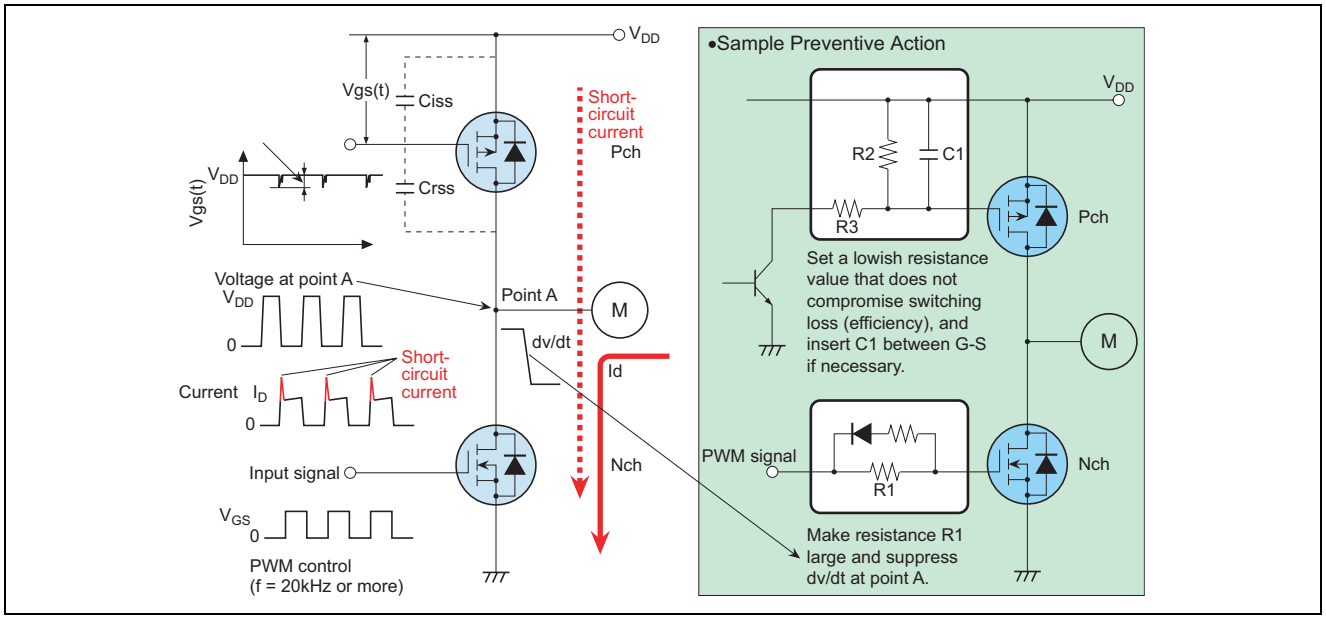


Figure 2.33 Malfunction (Arm Shorting) Countermeasures In Motor Application

2.8.3 Non-Isolated Synchronous Rectification Converter Low-Side Self-Turn-On Phenomenon

In appearance, this is similar to the above-described arm shorting phenomenon.

Figure 3.34 illustrates the low-side self-turn-on phenomenon in a non-isolated synchronous rectification circuit.

This phenomenon occurs at the switching timing at which high-side component Q1 is turned on while low-side component Q2 is off, and when the Q2 drain-source voltage changes abruptly from $V_{DS} \approx 0$ to V_{DS} = Vin, Ciss is charged via Crss of Q2, and Q2, which should really be off, is turned on.

That is to say, when $V_{GS}(Q2) = (Crss/Ciss + Crss) \times dV(t)$ (equation (1)) exceeds Vth of Q2, self-turn-on occurs. As a result, Q1 and Q2 become on simultaneously, and excessive loss is generated, component heat radiation and a temperature rise are caused, leading to degradation of efficiency.

Regarding the low-side component characteristics, due to large-current operation, low $R_{DS(on)}$ design is necessary, and therefore there is a tendency for the capacitance relationship (Ciss, Crss) to be large. Regarding the high-side component characteristics, due to the design emphasizing high speed, high-speed switching characteristics are implemented, and dV/dt becomes steeper. This suggests a tendency of susceptibility to the self-turn-on phenomenon.

Generally, the following two circuit countermeasures can be used.

1. Make only the high-side component turn-on time slower (suppress dV/dt).
2. Insert a capacitance C externally between the gate and source of the low-side component and (by making (K_S = (Crss/Ciss + Crss) smaller) improve the self-turn-on margin.

As a future trend, it is necessary to make both Ciss and Crss smaller in component design for high-frequency operation (1 MHz or above) and also make improvements that take account of the ratio of Ciss and Crss (Crss<<Ciss). Also, it is necessary not only to implement component improvements, but also to make the impedance between the gate and source when Q2 is off ($R_S + j\omega L_S$) as small as possible from the circuit design and mounting standpoints (since the above $V_{GS}(Q2)$ expression essentially holds true when ($R_S + j\omega L_S$) >> $1/j\omega$Ciss), and component performance can be fully exploited by means of these techniques.

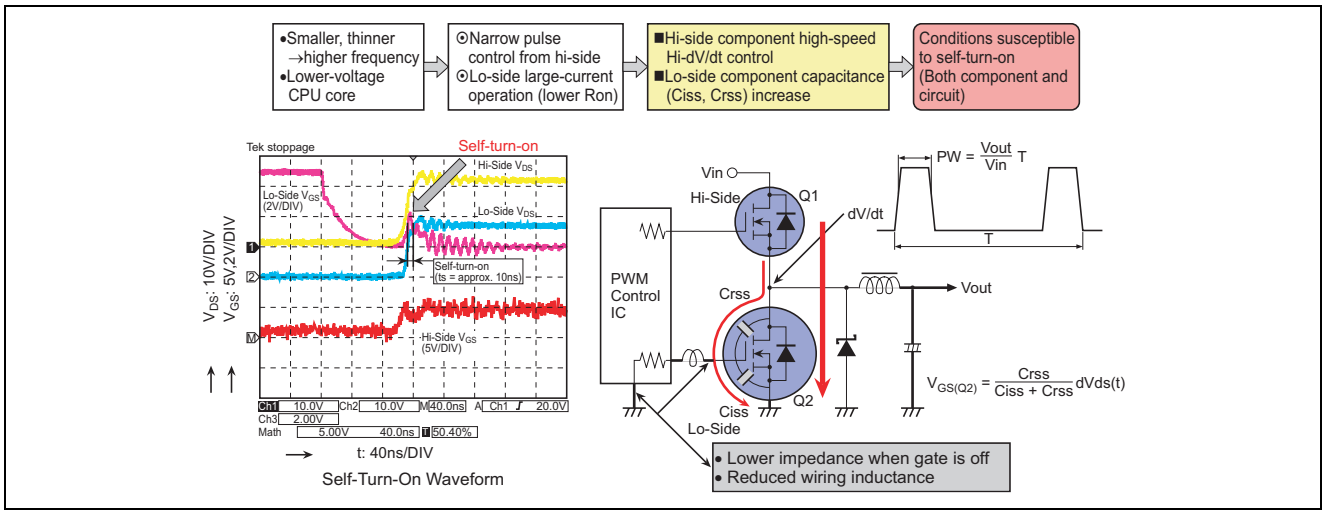


Figure 2.34 Problems in Synchronous Rectification Circuit

3. Power MOS FET Applications

3.1 Application Map

Figure 3.1 shows a power MOS FET and IGBT application map.

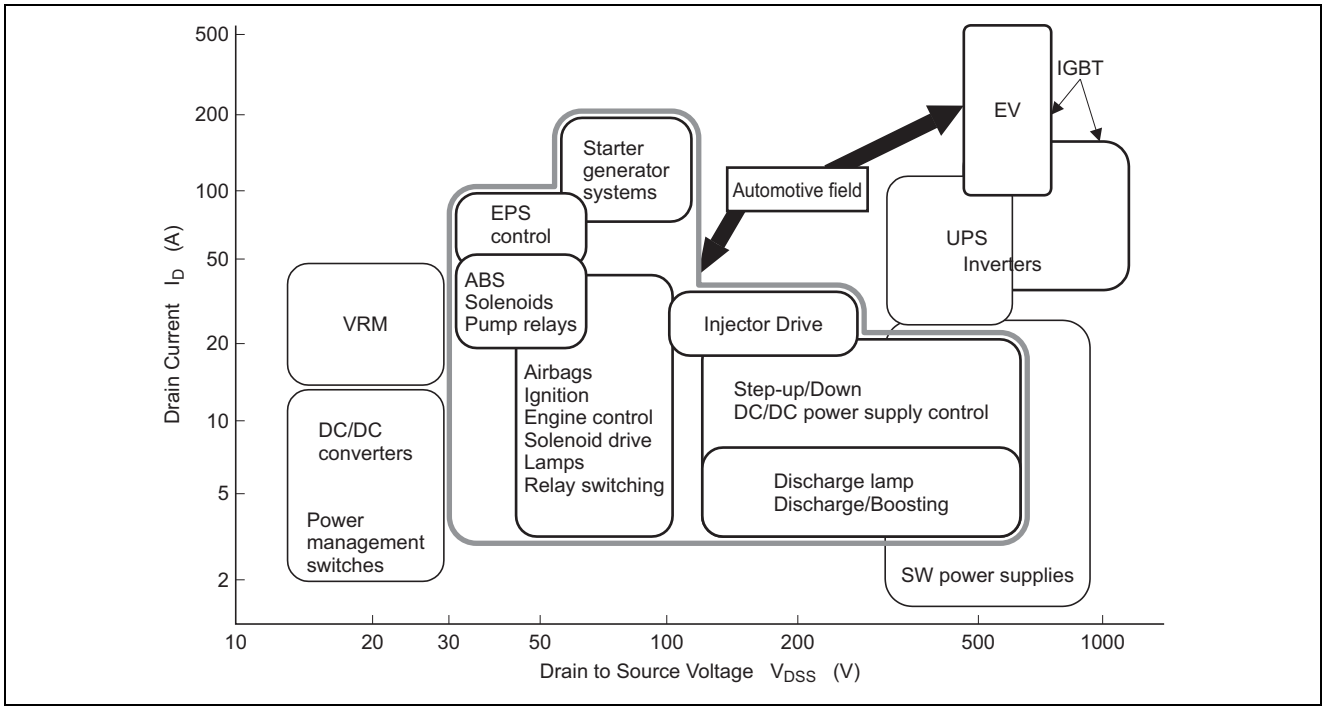


Figure 3.1 Power MOS FET and IGBT Applications

3.2 Automotive Applications

3.2.1 Technological Trends in Automotive Electrical Equipment

Figure 3.2 illustrates technological trends in automotive electrical equipment.

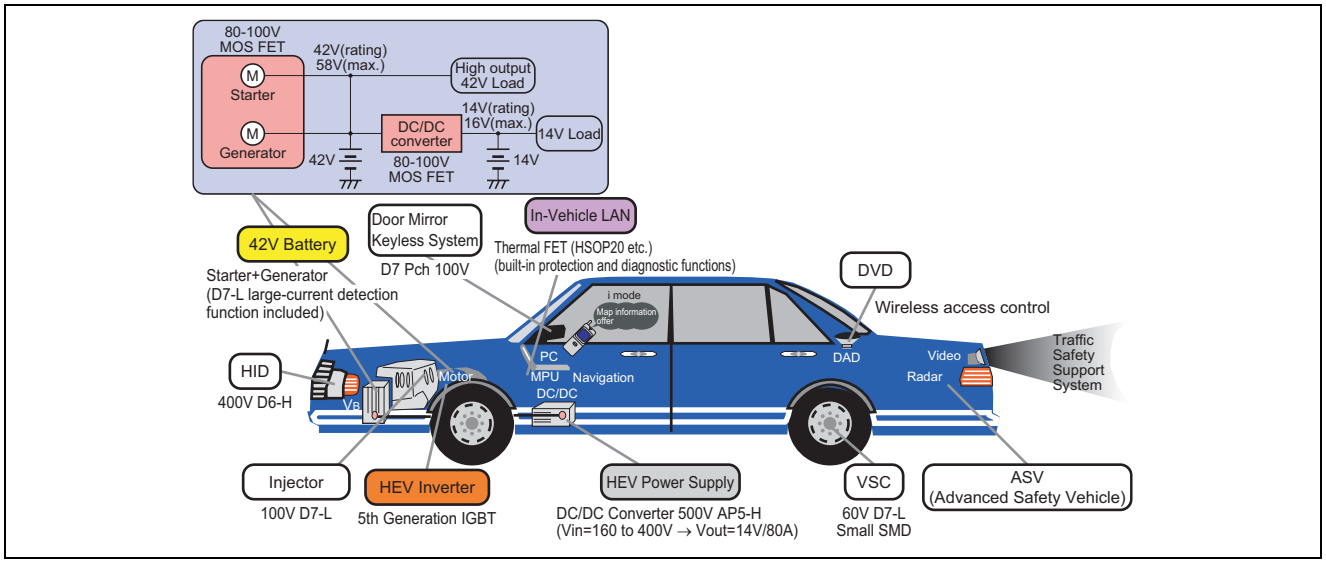


Figure 3.2 Technological Trends in Automotive Electrical Equipment

3.2.2 Sample Automobile ABS Application

Figure 3.3 shows a sample automobile ABS application.

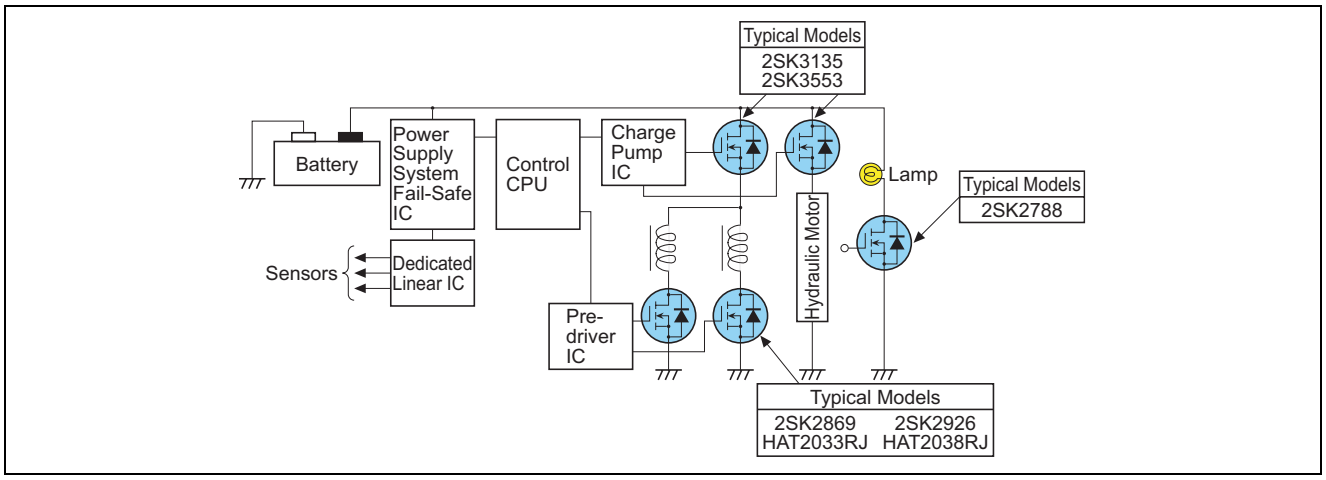


Figure 3.3 Sample Automobile ABS Application

3.2.3 Sample Automobile Power Steering Application

Figure 3.4 shows a sample automobile power steering application.

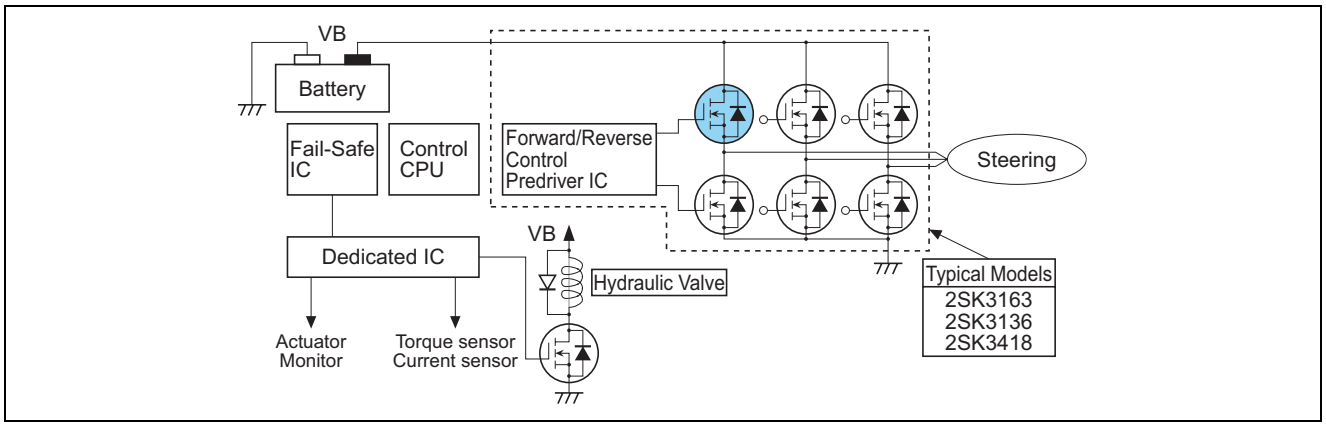


Figure 3.4 Sample Automobile Power Steering Application

3.2.4 Sample Automobile HID Headlamp Control Application

Figure 3.5 shows a sample automobile HID headlamp control application.

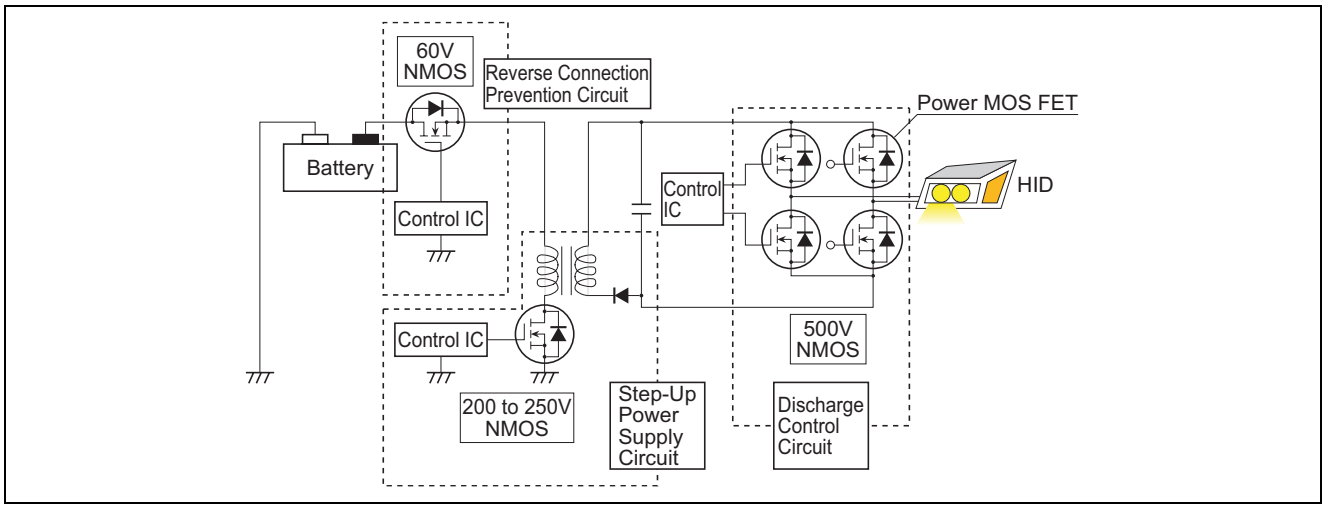


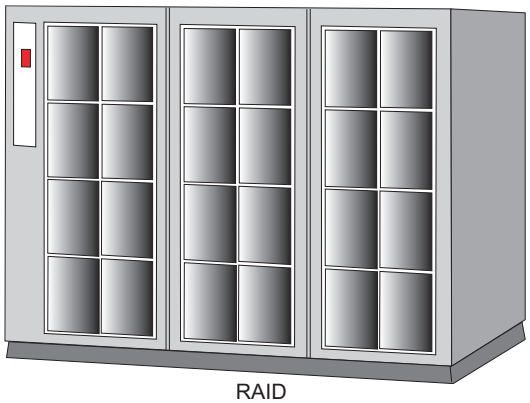
Figure 3.5 Sample Automobile HID Headlamp Control Application

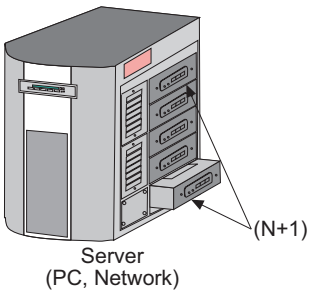
3.3 Power Supply Applications

3.3.1 Switching Power Supplies

- Application equipment
  Network servers, WS (workstations), RAID

Figure 3.6 shows a sample switching power supply application.

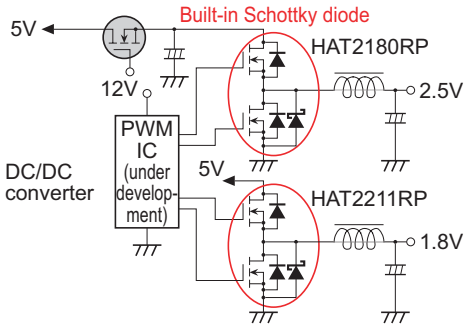




Application Blocks

Application	MOS FET	Control IC
PFC PFC+PWM	500V	HA16142 HA16158*
DC/DC	500V	HA16341 HA16342
Secondary-side synchronous rectification	30 to 60V	
Hot swap	20 to 30V	
VRM	20 to 30V	—

* : Under development



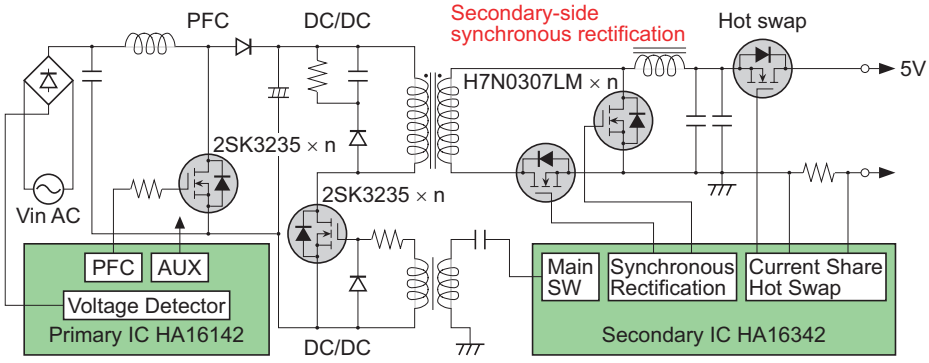


Figure 3.6 Sample Switching Power Supply Application

3.3.2 DC/DC Converters

- Application equipment
  Notebook PCs, VCR cameras, on-board power supply secondary side, lithium-ion battery pack overcharging protection

Figure 3.7 shows a sample DC-DC converter application.

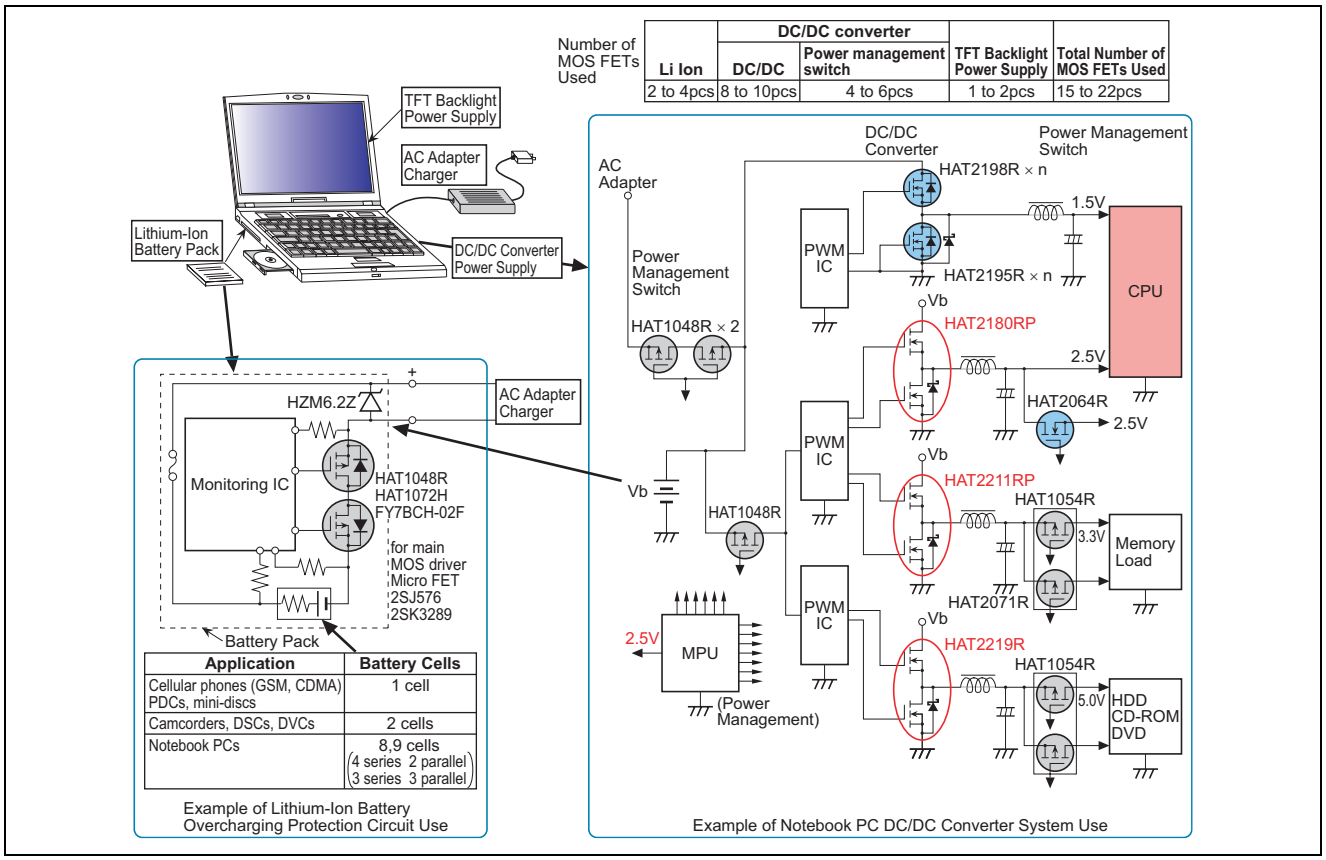


Figure 3.7 Sample DC/DC Converter Application

3.3.3 VRM (Voltage Regulator Module)

- Application equipment
  Desktop PCs, notebook PCs, network servers, WS (workstations)

Figure 3.8 shows a sample VRM application.

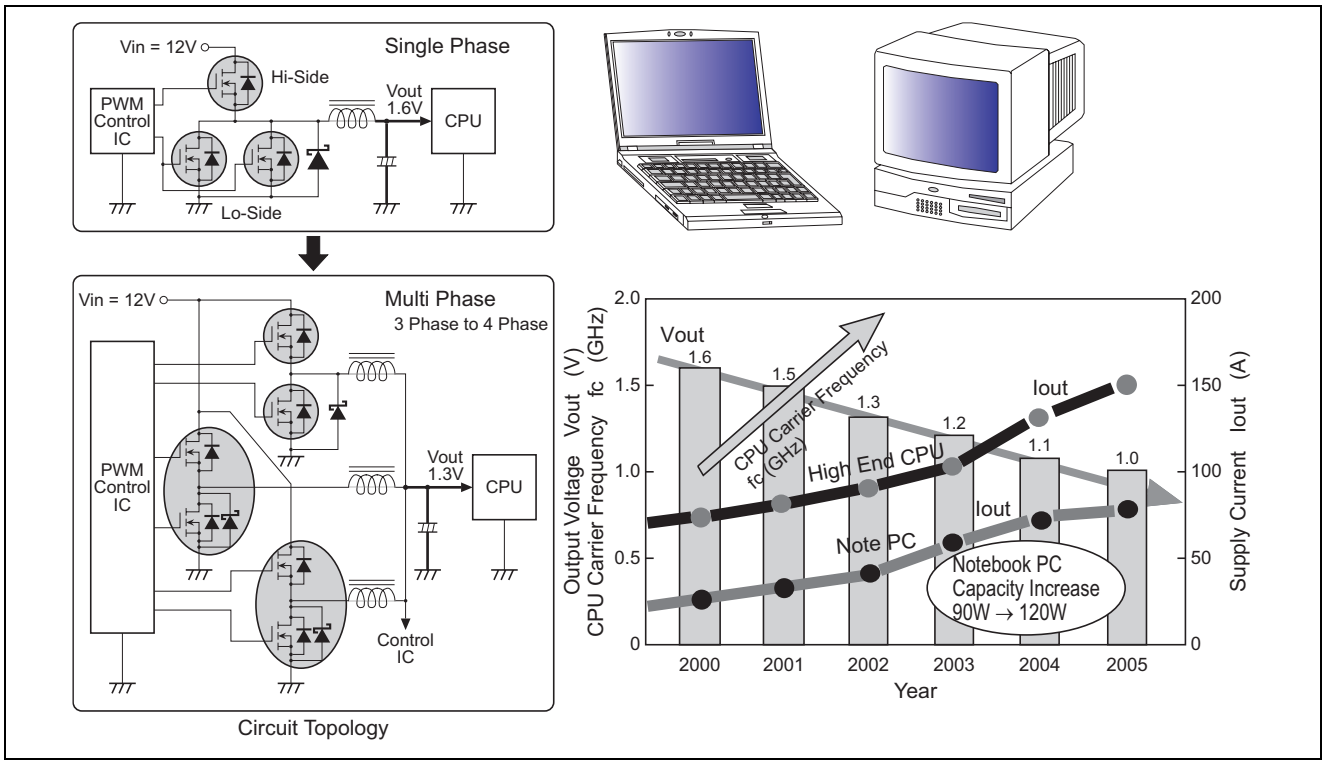


Figure 3.8 Sample VRM Application

3.3.4 Base Station SMPS (Switch-Mode Power Supply)

Figure 3.9 shows a sample base station SMPS application.

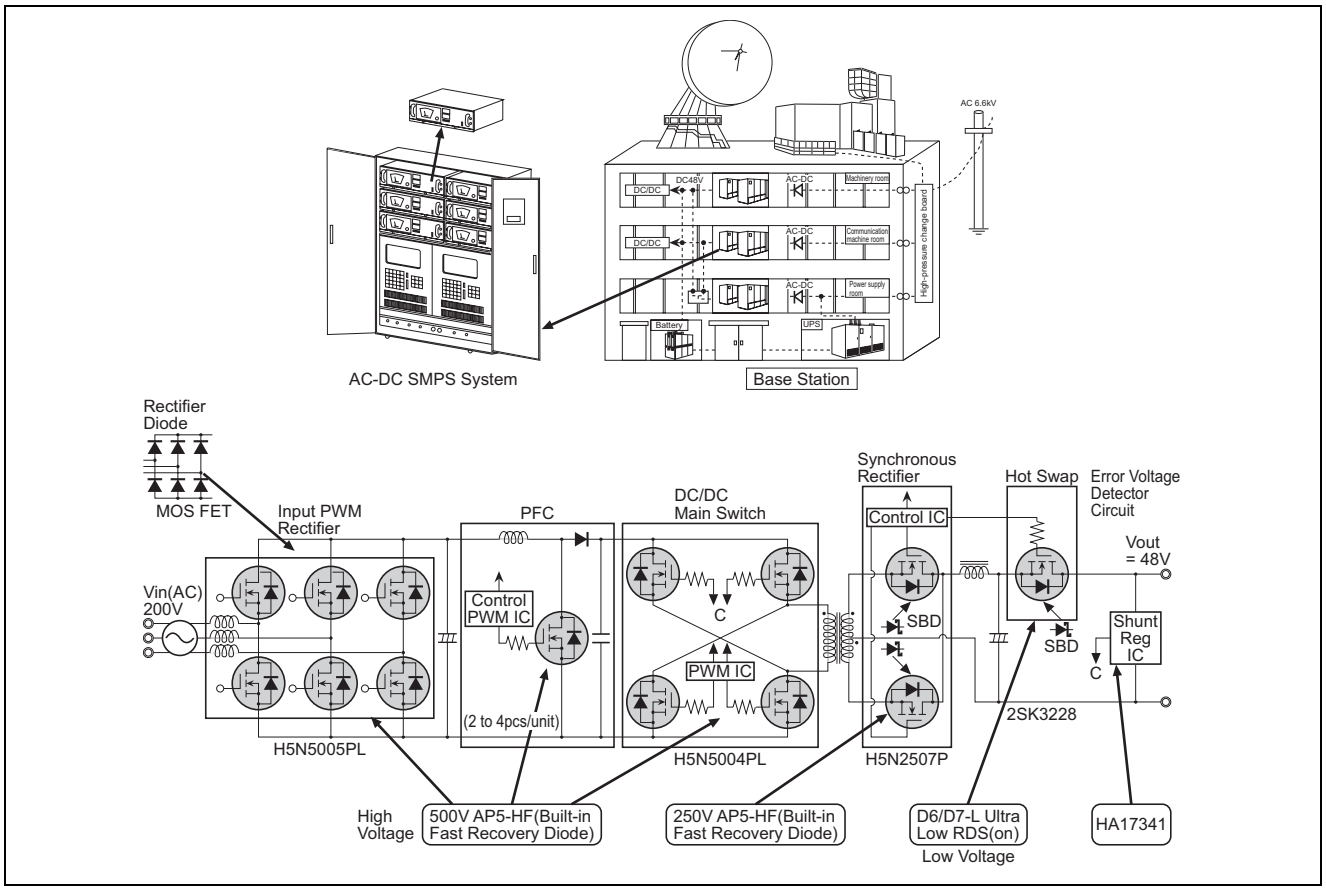


Figure 3.9 Sample Base Station SMPS Application

3.3.5 Communication Equipment DC/DC Converter

Figure 3.10 shows a sample communication equipment DC/DC converter application.

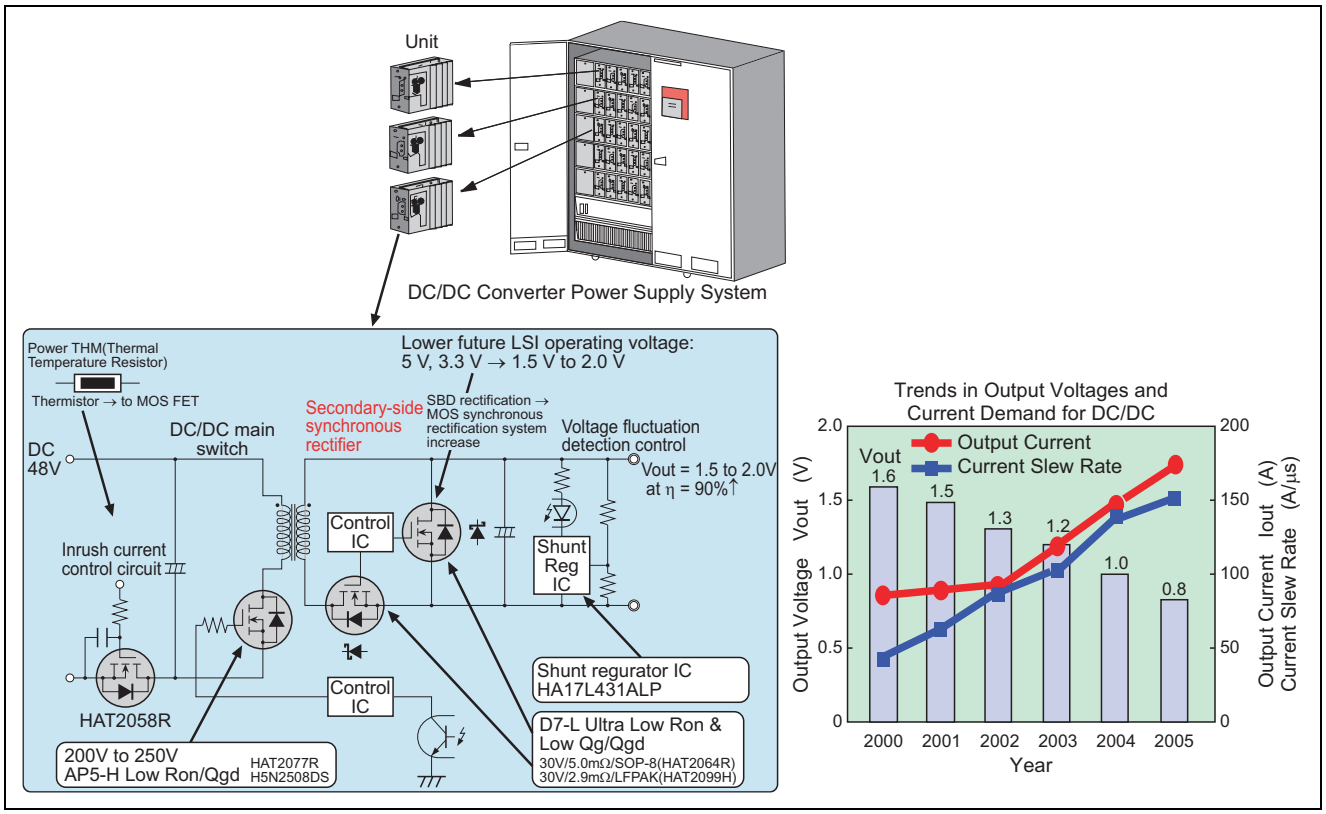


Figure 3.10 Sample Communication Equipment DC/DC Converter Application

3.4 Motor Drive Applications

3.4.1 Small Motor Drive

- Application equipment

Application	Function
H bridge	HDD (voice coil motor)
	Camera motor, electronic throttle
3-phase	HDD (spindle motor)
	PPC, printer (paper feed motor, polygon mirror)

Figure 3.11 shows sample small motor drive applications.

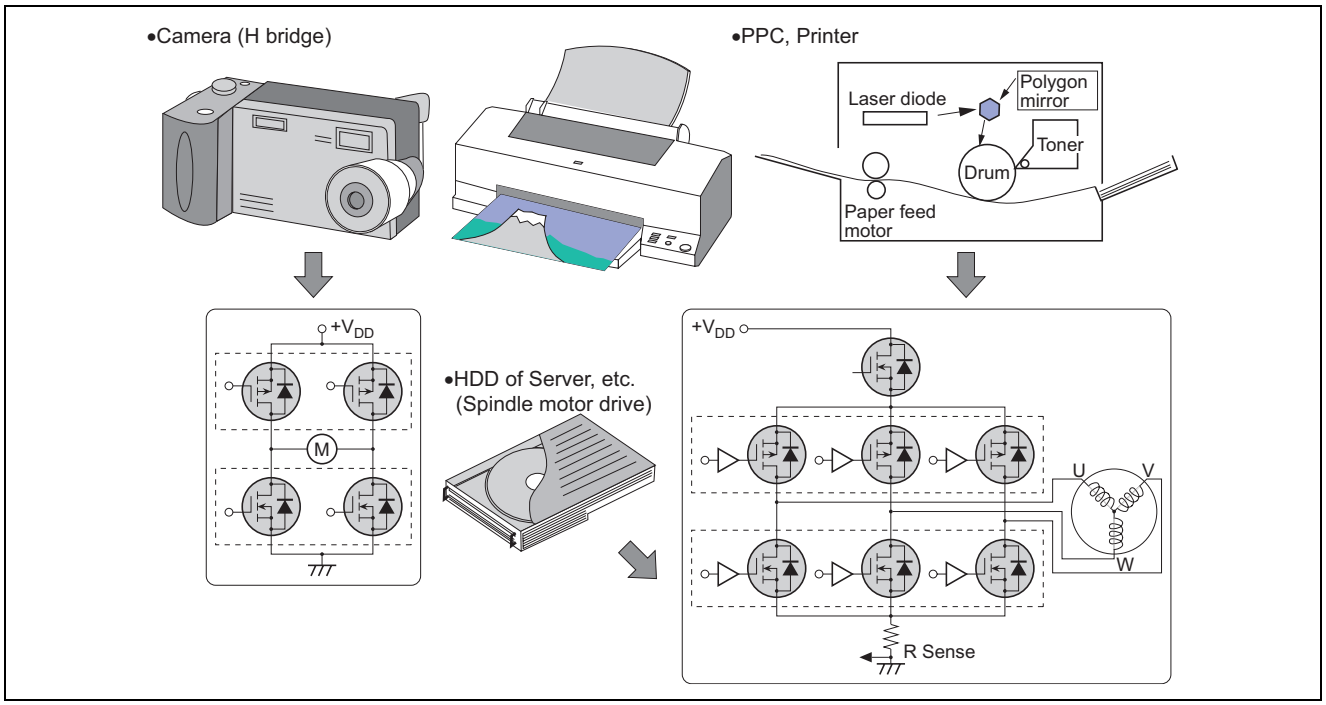


Figure 3.11 Sample Small Motor Drive Applications

Power MOS FET Application Note

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