R32C/100 Series

Example of External Bus Operation

R01AN0389EJ0101
Rev. 1.01
Nov. 30, 2011

Abstract

This document describes an example of external bus operation for the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications

This document describes the operation of a program written on the external device. The MCU and external device are connected using a separate bus (with a 16-bit data bus width).
Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Connection Example.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
External bus	Connection to the external device
Timer A (timer A0)	Program written on the external device is used

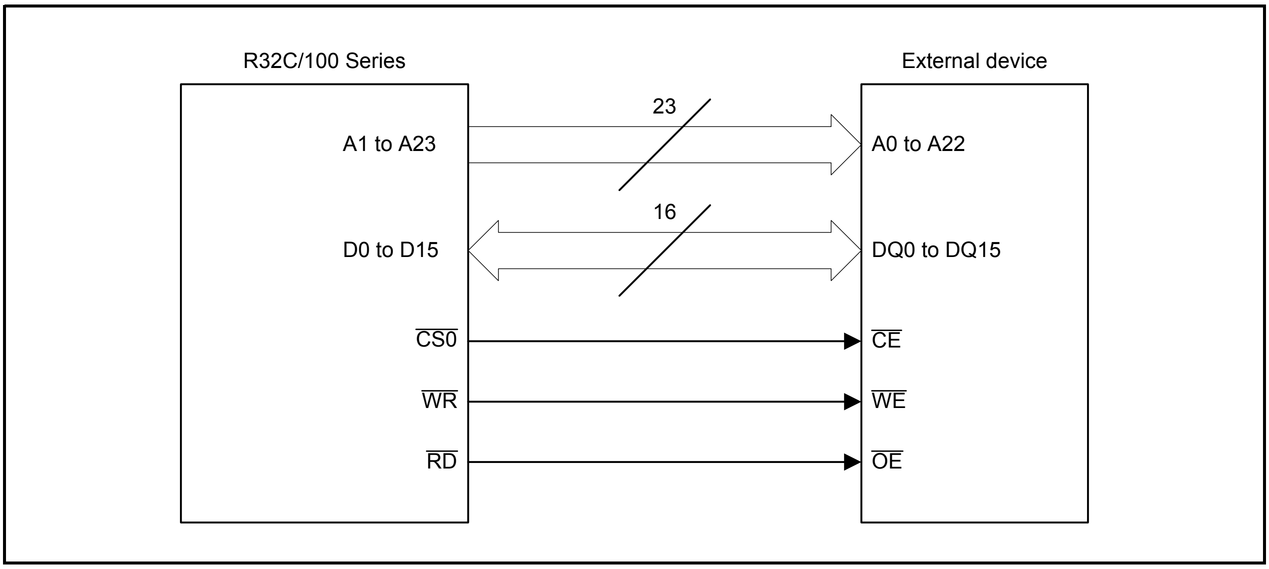


Figure 1.1 Connection Example

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	• Main clock: 16 MHz • PLL clock: 100 MHz • Base clock: 50 MHz • CPU clock: 50 MHz • Peripheral bus clock: 25 MHz • Peripheral clock source: 25 MHz
Operating voltage	3.3 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler Package V.1.02 Release 01
	Complie options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir "$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Memory expansion mode
Sample code version	Version 1.00
Debugger used (1)	E30A Emulator E30A Emulater Debugger, V1.02 Release 00
Tool used	External Flash Definition Editor (EFE)

Note:

1. The E8a debugger cannot be used to download this sample program.

3. Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221)
- R32C/100 Series Timer A Operation in Timer Mode (REJ05B1230)

4. Peripheral Functions

This chapter provides supplementary information on the external bus. The basic information is described in User's Manual: Hardware.

The R32C/100 Series MCU has the external bus to connect to the external device (ROM, etc.). The timing setting for communication with the external device is shown below.
Calculate the bus timing with the external device based on the electrical characteristics from the external device and the R32C/100 Series MCU.

Table 4.1 lists the External Device Parameters used in this application note. Refer to the datasheets from User's Manual: Hardware and the external device.

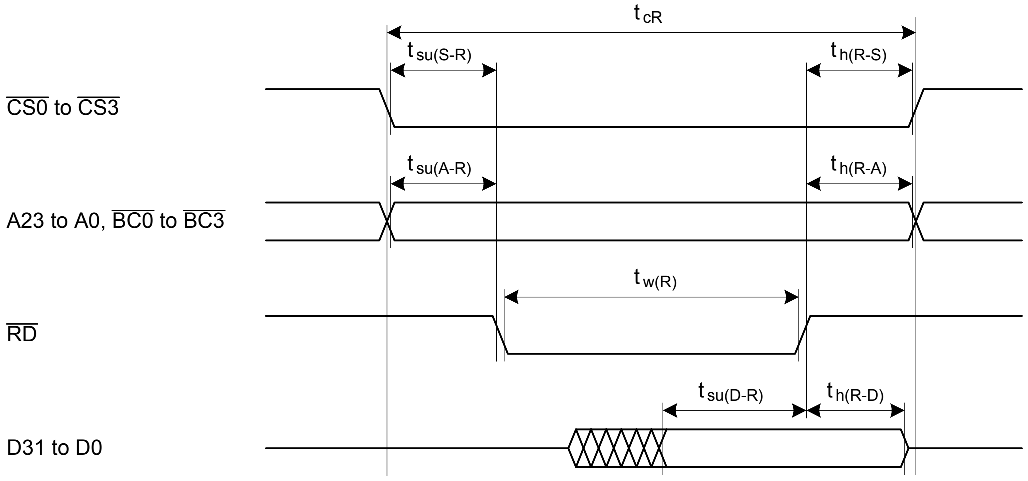
Table 4.1 External Device Parameters

Symbol	Content	Value
t_{CE}	Chip-select access time	70 ns (Max.)
t_{OE}	Output enable access time	25 ns (Max.)
t_{CS}	Chip-select setup time	0 ns (Min.)
t_{WP}	Write pulse width	45 ns (Min.)

The external bus timings (tsu(A-R), tw(R), tsu(A-W), and tw(W)) are determined by the base clock and the number of bus cycles. Use registers EBC0 to EBC3 to set the number of bus cycles. 50 MHz is set to the base clock (20 ns per cycle) in this application note.

4.1 Read Timing

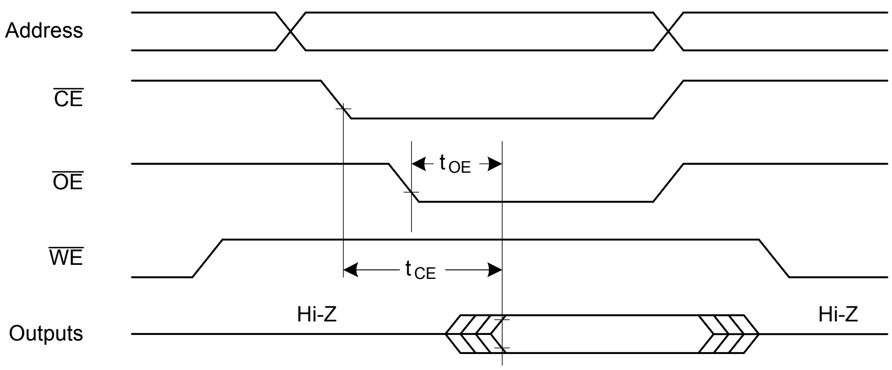
This section shows the bus timing calculation for reading from the external device. Figure 4.1 shows the Read Cycle of the R32C/100 Series.



t_{cR}: Read cycle time
tsu(S-R): Chip-select setup time for read
th(R-S): Chip-select hold time after read
tsu(A-R): Address setup time for read
th(R-A): Address hold time after read
tw(R): Read pulse width
tsu(D-R): Data setup time for read
th(R-D): Data hold time after read
tsu(S-R), th(R-S), tsu(A-R), tw(R), and th(R-D) are needed for the bus timing calculation.

Figure 4.1 Read Cycle of the R32C/100 Series

Figure 4.2 shows an Example of External Device Bus Timing When Reading.



t_{CE}: Chip-select access time
t_{OE}: Output enable access time

Figure 4.2 Example of External Device Bus Timing When Reading

tsu(A-R)(= tsu(S-R)) and tw(R) of the external bus timings are calculated using the external device requested timings (tCE and tOE). Figure 4.3 shows the Read Bus Timing Comparison between the R32C/100 Series and an External Device.

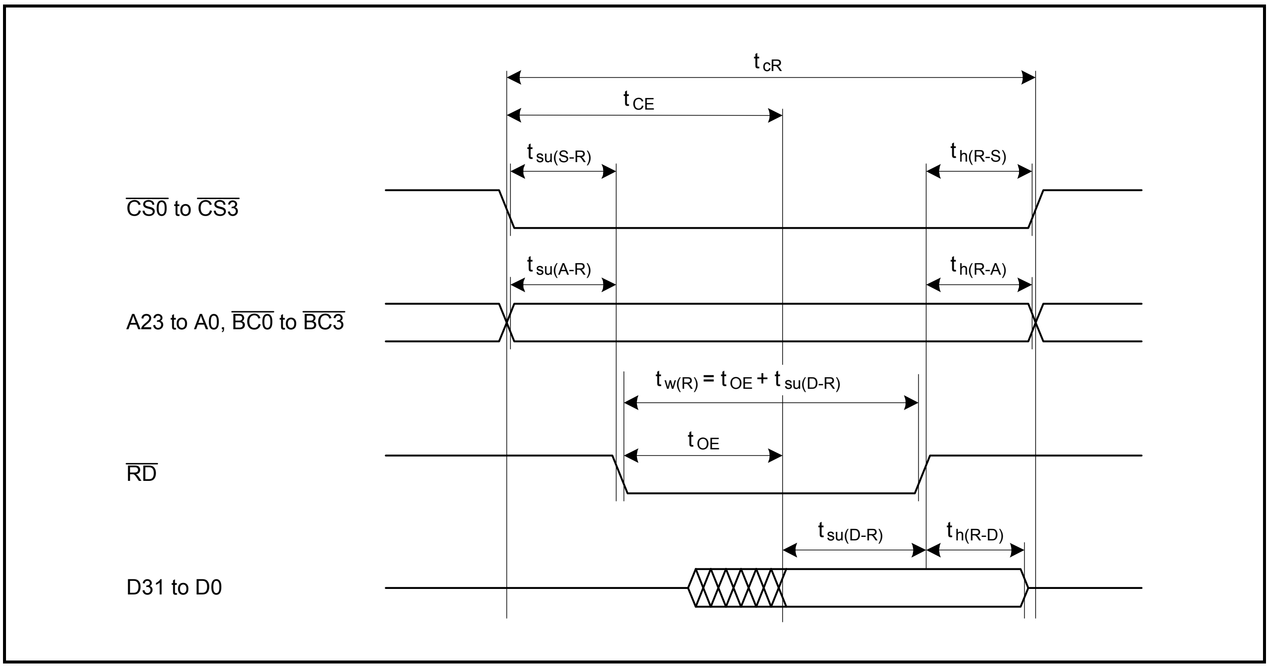


Figure 4.3 Read Bus Timing Comparison between the R32C/100 Series and an External Device

Calculating read cycle time:
tsu(A-R) and tw(R) for the read cycle time can be calculated using the following equation.

$$t_{CE} + tsu(D\text{-}R) \leq tsu(A\text{-}R) + tw(R)$$

Because tCE is 70 ns from Table 4.1 and tsu(D-R) is 40 ns from the User's Manual, the left side of the equation above may be shown as

70 ns + 40 ns = 110 ns.

Therefore, those times are determined by

110 ns $\leq$ tsu(A-R) + tw(R).

Set tw(R) to be tOE + tsu(D-R) or more from Figure 4.3. Because tsu(D-R) is 40 ns from the User's Manual and tOE is 25 ns from Table 4.1, tw(R) should be 65 ns or more. The optimal value for tw(R) is 80 ns from Table 4.2.

Table 4.2 Tw(R)(tw(R)) and Bit Settings: MPY1, MPY0, EWR1, and EWR0

EWR1 and EWR0 Bit Settings		MPY1 and MPY0 Bit Settings			
		00b	01b	10b	11b
		mpy = 1	mpy = 2	mpy = 3	mpy = 4
00b	wr = 1	1.5 (20 ns)	2.5 (40 ns)	3.5 (60 ns)	4.5 (80 ns)
01b	wr = 2	2.5 (40 ns)	4.5 (80 ns)	6.5 (120 ns)	8.5 (160 ns)
10b	wr = 3	3.5 (60 ns)	6.5 (120 ns)	9.5 (180 ns)	12.5 (240 ns)
11b	wr = 4	4.5 (80 ns)	8.5 (160 ns)	12.5 (240 ns)	16.5 (320 ns)
Formula		Tw(R) = wr × mpy + 0.5			

Notes:
1. Gray colored cell: Values do not meet the requirements.
2. Unit: cycles

The calculated tw(R) value is put into the equation.

$110 \text{ ns} \leq tsu(A\text{-}R) + 80 \text{ ns}$

Therefore, tsu(A-R) is 30 ns or more. The optimal value tsu(A-R) is 35 ns from Table 4.3.

Table 4.3 Tsu(A-R)(tsu(A-R)) and Bit Settings: MPY1, MPY0, ESUR1 and ESUR0

ESUR1 and ESUR0 Bit Settings		MPY1 and MPY0 Bit Settings			
		00b	01b	10b	11b
		mpy = 1	mpy = 2	mpy = 3	mpy = 4
00b	sur = 0	0.5 (-5 ns)	0.5 (-5 ns)	0.5 (-5 ns)	0.5 (-5 ns)
01b	sur = 1	1.5 (15 ns)	2.5 (35 ns)	3.5 (55 ns)	4.5 (75 ns)
10b	sur = 2	2.5 (35 ns)	4.5 (75 ns)	6.5 (115 ns)	8.5 (155 ns)
11b	sur = 3	3.5 (55 ns)	6.5 (115 ns)	9.5 (175 ns)	12.5 (235 ns)
Formula		Tsu(A-R) = sur × mpy + 0.5			

Notes:

1. Gray colored cell: Values do not meet the requirements.
2. Unit: cycles

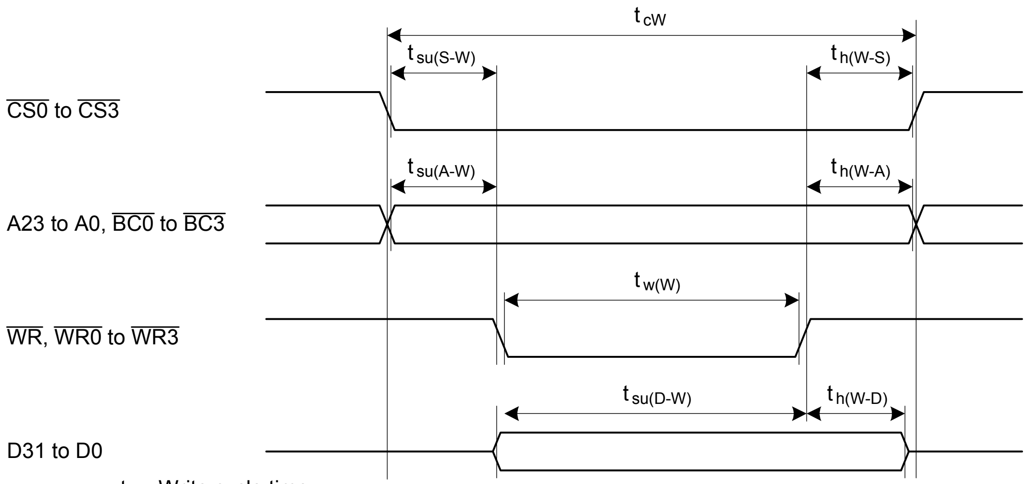
mpy, sur, and wr setting values corresponding to tw(R) and tsu(A-R) can be determined from Table 4.2 and Table 4.3.

Table 4.4 mpy, sur, and wr Setting Values

mpy	sur	wr
1	2	4
2	1	2
3	No corresponding value	No corresponding value
4	No corresponding value	1

4.2 Write Timing

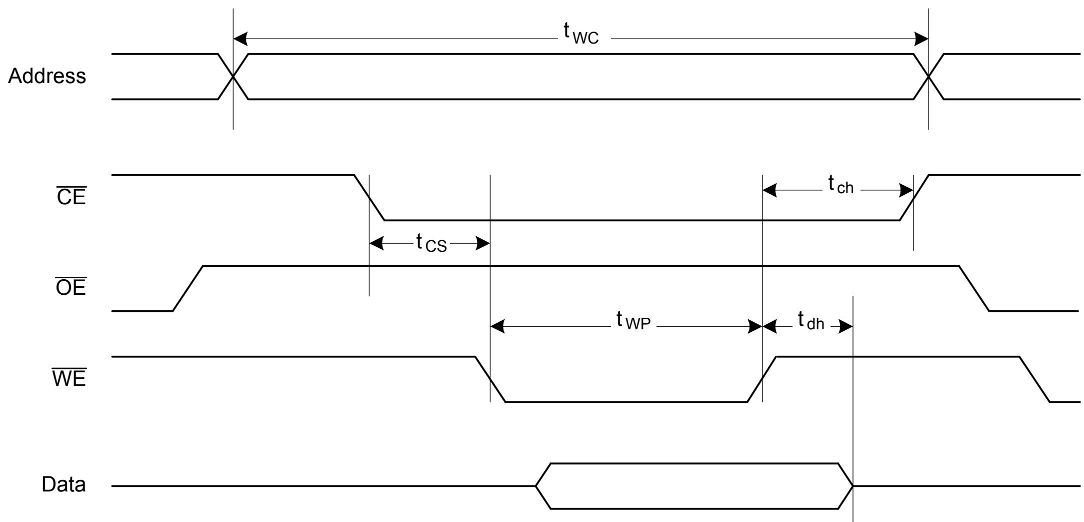
This section shows the bus timing calculation for writing to the external device. Figure 4.4 shows the R32C/100 Series Write Cycle.



t_{cW}: Write cycle time
tsu(S-W): Chip-select setup time for write
th(W-S): Chip-select hold time after write
tsu(A-W): Address setup time for write
th(W-A): Address hold time after write
tw(W): Write pulse width
tsu(D-W): Data setup time for write
th(W-D): Data hold time after write
tsu(S-W), th(W-S), tsu(A-W), tw(W), and th(D-W) are needed for the bus timing calculation.

Figure 4.4 R32C/100 Series Write Cycle

Figure 4.5 shows an Example of External Device Bus Timing (Write).



t_{WC}: Write cycle time
t_{CS}: Chip-select setup time
t_{ch}: Chip-select hold time
t_{WP}: Write pulse width
t_{dh}: Data hold time

Figure 4.5 Example of External Device Bus Timing When Writing

tsu(A-W)(= tsu(S-W)) and tw(W) of the external bus timings are calculated using the external device requested timings (tCS and tWP). Figure 4.6 shows the Write Bus Timing Comparison between the R32C/100 Series and the External Device.

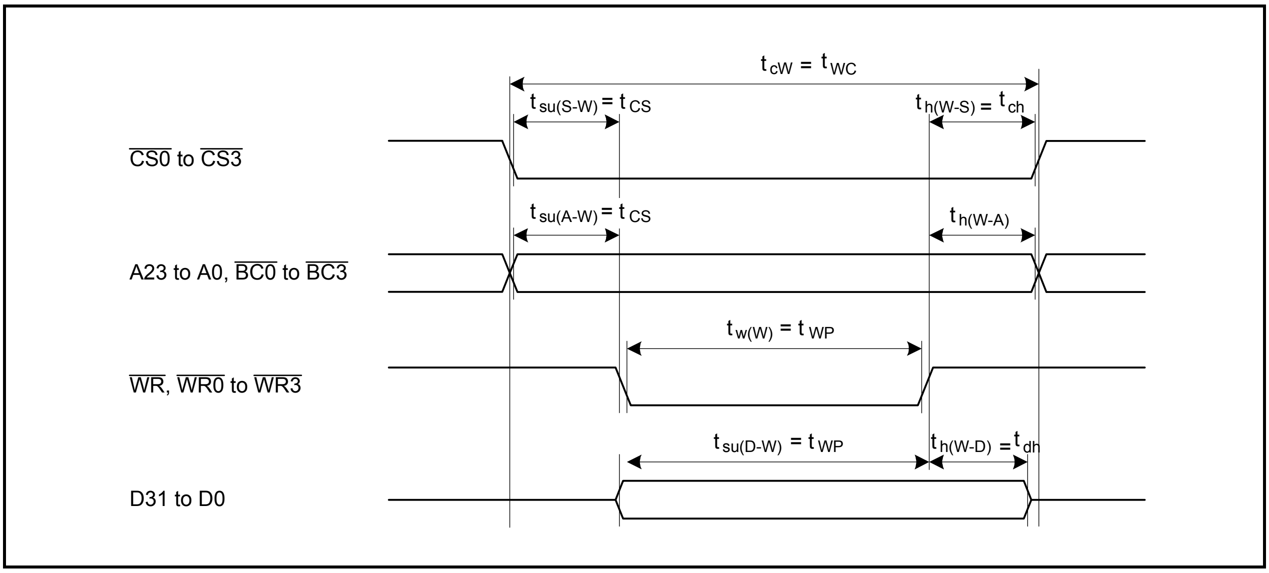


Figure 4.6 Write Bus Timing Comparison between the R32C/100 Series and the External Device

Calculating the write cycle time:
tsu(A-W) and tw(W) for the write cycle time can be calculated using the following equation as:

$$t_{CW} \leq tsu(A\text{-}W) + tw(W) + th(W\text{-}A)$$

Set tw(W) to be tWP or more from Figure 4.6. Because tWP is 45 ns from Table 4.1, tw(W) should be 45 ns or more. The optimal value for tw(W) is 60 ns from Table 4.5.

Table 4.5 Tw(W)(tw(W)) and Bit Settings: MPY1, MPY0, EWW1, and EWW0

EWW1 and EWW0 Bit Settings		MPY1 and MPY0 Bit Settings			
		00b	01b	10b	11b
		mpy = 1	mpy = 2	mpy = 3	mpy = 4
00b	ww = 1	0.5 (1)	1.5 (20 ns)	2.5 (40 ns)	3.5 (60 ns)
01b	ww = 2	1.5 (20 ns)	3.5 (60 ns)	5.5 (100 ns)	7.5 (140 ns)
10b	ww = 3	2.5 (40 ns)	5.5 (100 ns)	8.5 (160 ns)	11.5 (220 ns)
11b	ww = 4	3.5 (60 ns)	7.5 (140 ns)	11.5 (220 ns)	15.5 (300 ns)
Formula		Tw(W) = ww × mpy - 0.5			

Notes:
1. Do not set this value.
2. Gray colored cell: Values do not meet the requirements.
3. Unit: cycles

The calculated tw(W) value is put into the equation as
$70 \text{ ns} \leq tsu(A\text{-}W) + 60 \text{ ns} + th(W\text{-}A)$.
th(W-A) may be calculated from the User's Manual as
$1.5 \times tc(BASE) - 15 = 15$ ns.
Then,
$70 \text{ ns} \leq tsu(A\text{-}W) + 60 \text{ ns} + 15 \text{ ns}$.

Therefore, tsu(A-W) will be -5 ns. When the calculated value is less than 0, use 0 ns or more. The optimal value for tsu(A-W) is 5 ns from Table 4.6.

Table 4.6 Tsu(A-W)(tsu(A-W)) and Bit Settings: MPY1, MPY0, ESUW1, and ESUW0

ESUW1 and ESUW0 Bit Settings		MPY1 and MPY0 Bit Settings			
		00b	01b	10b	11b
		mpy = 1	mpy = 2	mpy = 3	mpy = 4
00b	suw = 0	1 (5 ns)	1 (5 ns)	1 (5 ns)	1 (5 ns)
01b	suw = 1	2 (35 ns)	3 (45 ns)	4 (65 ns)	5 (85 ns)
10b	suw = 2	3 (45 ns)	5 (85 ns)	7 (125 ns)	9 (165 ns)
11b	suw = 3	4 (65 ns)	7 (125 ns)	10 (185 ns)	13 (245 ns)
Formula		Tsu(A-W) = suw × mpy + 1			

Note:
1. Unit: cycles

mpy, suw, and ww setting values corresponding to tw(W) and tsu(A-W) can be determined from Table 4.5 and Table 4.6.

Table 4.7 mpy, suw, and ww Setting Values

mpy	suw	ww
1	0	4
2	0	2
3	0	No corresponding value
4	0	1

4.3 EBC0 to EBC3 Setting Values

Table 4.8 lists the Optimal Values of Registers EBC0 to EBC3. They are selected from Table 4.4 and Table 4.7 to meet the clock and the external device requirements. Registers EBC0 to EBC3 setting values are xx01 1100 00x1 1110b.

Table 4.8 Optimal Values of Registers EBC0 to EBC3

Contents	Setting value
mpy	1
sur	2
wr	4
suw	0
ww	4

5. Hardware

5.1 Pins Used

Table 5.1 lists the Pins Used and Their Functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
P2_1/A1 to P2_7/A7	Output	Output addresses to the external device
P3_0/A8 to P3_7/A15		
P4_0/A16 to P4_7/A23		
P0_0/D0 to P0_7/D7	I/O	Data is input/output with the external device
P1_0/D8 to P1_7/D15		
P11_0/$\overline{CS0}$	Output	Outputs chip-select signal to the external device
P5_0/$\overline{WR0}$/$\overline{WR}$	Output	Outputs write signal to the external device
P5_2/$\overline{RD}$	Output	Output read signal to the external device
P6_0	Output	Interrupt request confirmation port (This pin is used in the program operated by the external device.)

6. Software

6.1 Operation Overview

The program diverges to the program written on the external device and then executes it. The program on the external device must be written in advance to operate timer A0 in timer mode.

External bus initial setting:

- Separate bus
- 16-bit bus width
- Chip-select area setting
- Bus timing setting
- Memory expansion mode

Figure 6.1 shows the Sample Code Operation.

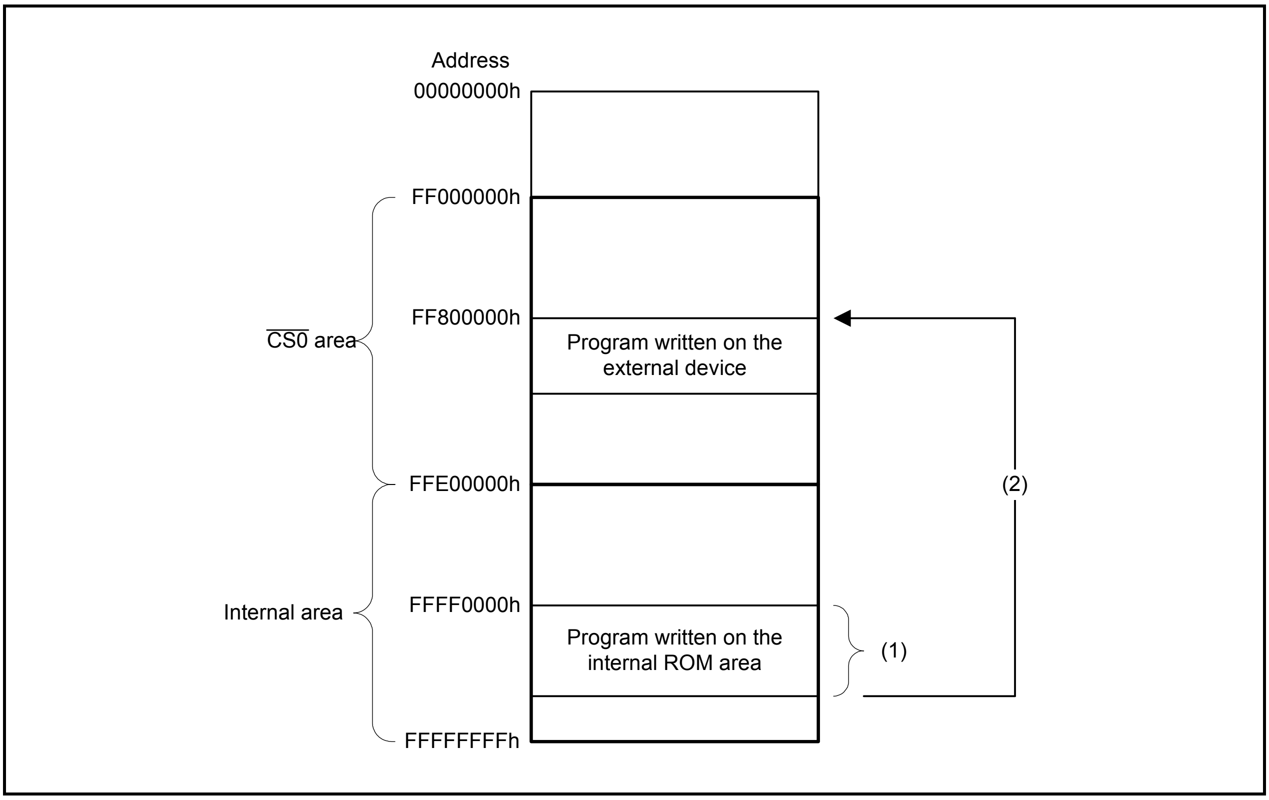


Figure 6.1 Sample Code Operation

6.2 Invariable Table

Table 6.1 lists the Invariables Used in the Sample Code.

Table 6.1 Invariables Used in the Sample Code

Invariable Name	Setting Value	Contents
DEF_CB01	C0h	Sets to the values from A25 to A18 of the start address of CS0 space (FF000000h)
DEF_CB12	80h	Sets to the values from A25 to A18 of the start address of CS1 space (FE000000h)
DEF_CB23	40h	Sets to the values from A25 to A18 of the start address of CS2 space (01000000h)

6.3 Flowcharts

Flowcharts for the sample code are shown below. Numbers in the flowcharts relate to the numbers in the source code.

6.3.1 Main Processing

Figure 6.2 shows the Main Processing.

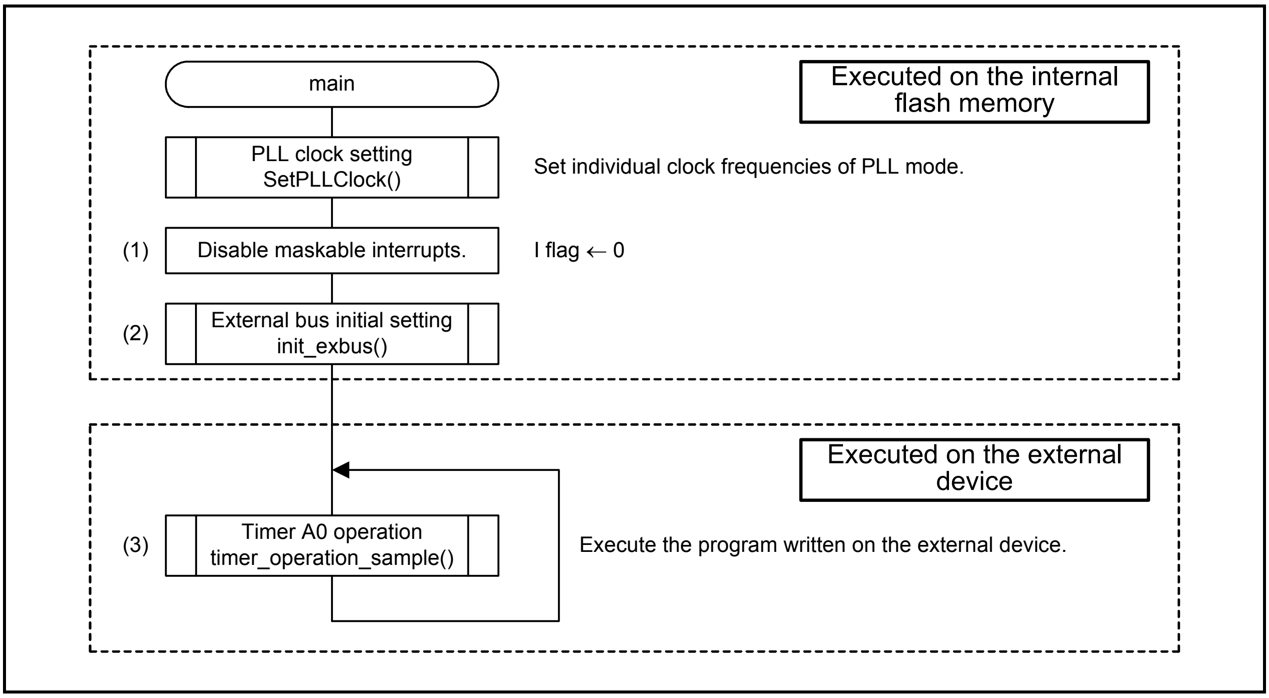


Figure 6.2 Main Processing

6.3.2 External Bus Initial Setting

Figure 6.3 shows the External Bus Initial Setting.

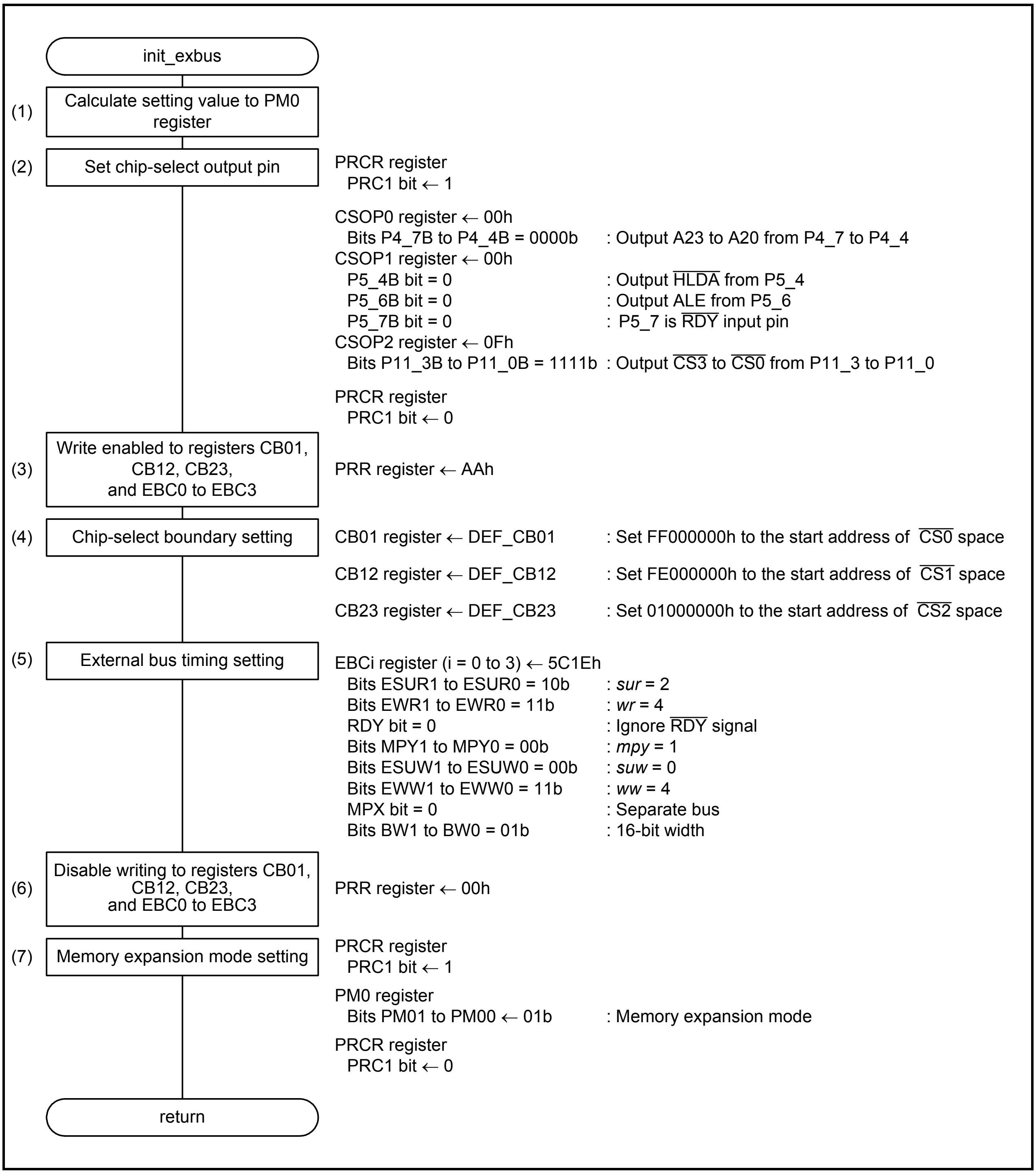


Figure 6.3 External Bus Initial Setting

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10
R32C/117 Group User's Manual: Hardware Rev.1.10
R32C/118 Group User's Manual: Hardware Rev.1.10
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package
C Compiler User's Manual Rev.2.00
The latest version can be downloaded from the Renesas Electronics website.

Website and Support

Renesas Electronics website
http://www.renesas.com/

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Revision History	R32C/100 Series Example of External Bus Operation

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 28, 2011	—	First edition issued
1.01	Nov. 30, 2011	6	Modfied: Figure 4.1 “t_{cr}” → “t_{cR}” “Address setup time after read” → “Address hold time after read”

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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