R32C/100 Series

Using Mirror Registers with Three-Phase Motor Control Timers While in Triangular Wave Modulation Mode and Three-Phase Mode 1

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Abstract

This document describes using mirror registers with the three-phase motor control timers in the R32C/100 Series.

Products

R32C/120 Group
R32C/121 Group
R32C/145 Group
R32C/151 Group
R32C/152 Group
R32C/153 Group
R32C/156 Group
R32C/157 Group
R32C/160 Group
R32C/161 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

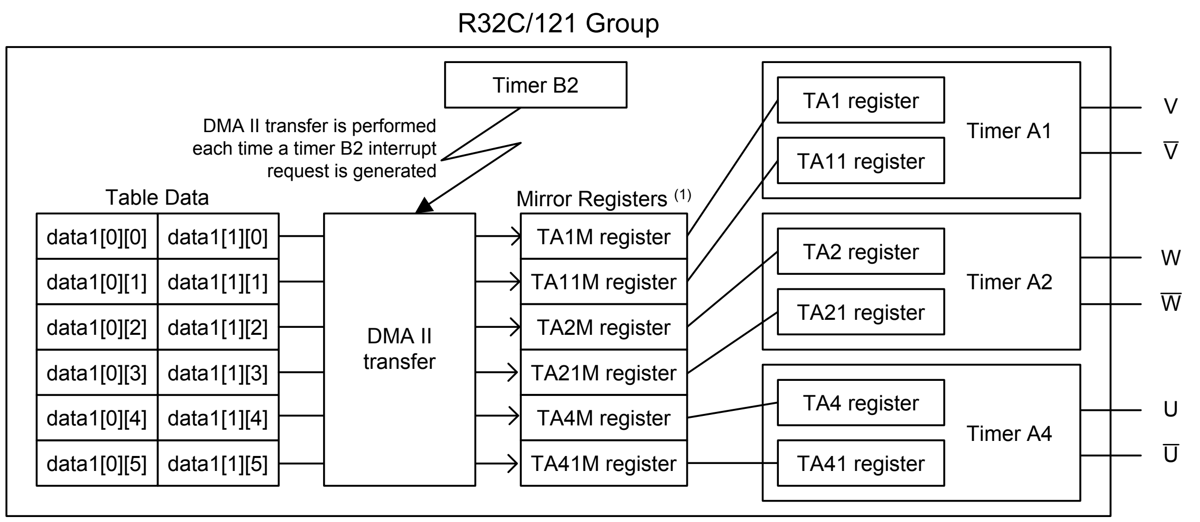
1. Specifications

When using three-phase motor control timers to output a triangular wave, by combining the timer Ai/timer Ai-1 mirror registers with a DMAC II burst transfer, the timer value can be set by a single transfer request (i = 1, 2, 4).

Table 1.1 lists the Peripheral Functions and Their Applications. Figure 1.1 shows a Block Diagram.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
Timer A (timers A1, A2, and A4)	Three-phase motor control timers
Timer B (timer B2)	Three-phase motor control timers
DMAC II	Transfers setting values to timer Ai/timer Ai-1 mirror registers



Note:
1. Values written to the TAiM and TAi1M registers are reflected in the TAi and TAi1 registers (i = 1, 2, 4).

Figure 1.1 Block Diagram

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64219JFB (R32C/121 Group)
Operating frequencies	• Main clock: 8 MHz • PLL clock: 128 MHz • Base clock: 64 MHz • CPU clock: 64 MHz • Peripheral bus clock: 32 MHz • Peripheral function clock source: 32 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics R32C/100 Series C Compiler V.1.02 Release 01
	Compile options -D__STACKSIZE__=0X300 -D__ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFBDC -c -finfo -dir “$(CONFIGDIR)” Default setting is used in the integrated development environment.
Operating mode	Single-chip mode
Sample code version	Version 1.00

3. Reference Application Notes

Application notes associated with this application note are listed below. Refer to these application notes for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)
- R32C/100 Series Three-phase Motor Control Timers (Triangular Wave Modulation Mode, Three-phase Mode 1) (R01AN0029EJ0100)
- R32C/100 Series DMA II Setting Example (Memory-to-memory Burst Transfer) (REJ05B1228-0100)

4. Peripheral Functions

This chapter provides supplementary information on the timer Ai/timer Ai-1 mirror registers (i = 1, 2, 4). Refer to the User's Manual (Hardware) for general information.

4.1 Timer Ai/Timer Ai-1 Mirror Registers

Values set to timer Ai and timer Ai-1 mirror registers can be reflected in timer Ai and timer Ai-1 registers (TAi and TAi1 registers). For example, if a value is set to the TA1M register, the same value is set to the TA1 register.

Figure 4.1 shows the timer Ai and timer Ai-1 registers, and Figure 4.2 shows the timer Ai and timer Ai-1 mirror registers.

Timer Ai/Timer Ai-1 Registers (i = 1, 2, 4) (1 to 6)

b15 b8 b7 b0

Symbol	Address	Reset Value
TA1, TA2, TA4	0349h to 0348h, 034Bh to 034Ah, 034Fh to 034Eh	Undefined
TA11, TA21, TA41	0303h to 0302h, 0305h to 0304h, 0307h to 0306h	Undefined

Function	Setting Range	RW
The timer stops when the nth count source is counted after a start trigger is generated. Output signal for each phase is switched when timers A1, A2, and A4 stop (n = setting value)	0000h to FFFFh	WO

Notes:
1. A 16-bit write access to these registers should be performed.
2. When these registers are set to 0000h, the counter does not start, and no timer Ai interrupt request is generated.
3. The MOV instruction should be used to set these registers.
4. When the INV15 bit in the INVC1 register is set to 0 (dead time enabled), the turn-on output signal is switched to its active state with a delay. It is switched when the dead time timer stops.
5. When the INV11 bit in the INVC1 register is set to 0 (three-phase mode 0), the value of the TAi register is transferred to the reload register by a timer Ai start trigger. When the INV11 bit is set to 1 (three-phase mode 1), firstly the value of the TAi1 register is transferred to the reload register by a timer Ai start trigger. Then the value of the TAi register is transferred by the next timer Ai start trigger. After that the value of these registers TAi1 and TAi is alternately transferred to the reload register.
6. These registers should not be written when the timer B2 underflows.

Figure 4.1 Timer Ai/Timer Ai-1 Registers

Timer Ai/Timer Ai-1 Mirror Registers (i = 1, 2, 4) (1 to 7)

b15 b8 b7 b0

Symbol	Address	Reset Value
TA1M, TA11M	0221h to 0220h, 0223h to 0222h	Undefined
TA2M, TA21M	0225h to 0224h, 0227h to 0226h	Undefined
TA4M, TA41M	0229h to 0228h, 022Bh to 022Ah	Undefined

Function	Setting Range	RW
The timer stops when the nth count source is counted after a start trigger is generated. Output signal for each phase is switched when timers A1, A2, and A4 stop (n = setting value)	0000h to FFFFh	WO

Notes:
1. A 16-bit write access to these registers should be performed.
2. The values written in these registers are reflected to registers TAj and TAj1.
3. When these registers are set to 0000h, the counter does not start, nor the timer Ai interrupt request is generated.
4. The MOV instruction should be used to set these registers.
5. When the INV15 bit in the INVC1 register is set to 0 (dead time enabled), the turn-on output signal is switched to its active state with a delay; It is switched when the dead time timer stops.
6. When the INV11 bit in the INVC1 register is set to 0 (three-phase mode 0), the value of the TAi register is transferred to the reload register by a timer Ai start trigger. When the INV11 bit is set to 1 (three-phase mode 1), firstly the value of the TAi1 register is transferred to the reload register by a timer Ai start trigger. Then the value of the TAi register is transferred by the next timer Ai start trigger. After that the value of these registers TAi1 and TAi is alternately transferred to the reload register.
7. These registers should not be written at the timing when the timer B2 underflows.

Figure 4.2 Timer Ai/Timer Ai-1 Mirror Registers

4.2 Notes on Setting the TAi and TAi1 Registers (i = 1, 2, 4)

Note the following when setting values to the TAi and TAi1 registers.

(1) TAi setting value

When 0 is set to the TAi register (0 or 1 when the dead time timer count source is f1 divided by 2), as the TAi timer does not count and a falling edge does not occur, the current output waveform level is maintained.

If a value larger than the TB2 setting value is set to TAi (when the dead time timer count source is f1 divided by 2, a value larger than the TB2 setting value - 1), the TAi timer continues to be counted in the TB2 period, a falling edge is not generated, and the output waveform maintains its current level. Therefore, only set a value larger than the TB2 setting value to TAi when the output waveform level needs to be maintained.

(2) Restarting the dead time timer

Depending on the data set to the TAi register, if a dead time timer activation source is generated during a dead time timer count, the dead time timer will not restart. If the conditions below are met, note that the dead time timer will not restart.

In triangular wave modulation mode (three-phase mode 0): dead time timer count source f1
((TB2 setting value + 1) - even numbered TAi setting value) + odd numbered TAi setting value is less than the dead time timer setting value
Even numbered TAi setting value + ((TB2 setting value + 1) - odd numbered TAi setting value) is less than the dead time timer setting value

In triangular wave modulation mode (three-phase mode 1): dead time timer count source f1
((TB2 setting value + 1) - TAi1 setting value) + TAi setting value is less than the dead time timer setting value
TAi1 setting value + ((TB2 setting value + 1) - TAi setting value) is less than the dead time timer setting value

Sawtooth wave modulation mode: dead time timer count source f1
((TB2 setting value + 1) - TAi1 setting value) - 1 is less than the dead time timer setting value
TAi setting value - 1 is less than the dead time timer setting value

5. Hardware

5.1 Pins Used

Table 5.1 lists the Pins Used and Their Functions.

Table 5.1 Pins Used and Their Functions

Pin Name	I/O	Function
P7_2/TA1OUT/V	Output	Three-phase PWM waveform output (V-phase)
P7_3/TA1IN/$\overline{V}$	Output	Three-phase PWM waveform output ($\overline{V}$-phase)
P7_4/TA2OUT/W	Output	Three-phase PWM waveform output (W-phase)
P7_5/TA2IN/$\overline{W}$	Output	Three-phase PWM waveform output ($\overline{W}$-phase)
P8_0/TA4OUT/U	Output	Three-phase PWM waveform output (U-phase)
P8_1/TA4IN/$\overline{U}$	Output	Three-phase PWM waveform output ($\overline{U}$-phase)

6. Software

This chapter describes using the three-phase motor control timers to alternately output two types of triangular waves. DMA II transfer occurs every two times timer B2 underflows, and the timer Ai/timer Ai-1 mirror register values are rewritten (i = 1, 2, 4). The timer Ai/timer Ai-1 mirror register values are changed in the DMAC II transfer complete interrupt handling. The settings are shown below.

DMAC II settings

- Interrupt request level 7 is available for DMA II transfer.
- Set the transfer source to memory-to-memory transfer.
- Set the transfer size to 16 bits.
- Set the source addressing to increment.
- Set the destination addressing to increment.
- Set the transfer mode to burst transfer.
- Set the number of DMA II transfer complete interrupts to 6.

Three-phase motor control timer settings

- Set to triangular wave modulation mode (three-phase mode 1).
- Set frequency of timer B2 interrupt occurrence to 2.
- Set timer B2 underflow as the ICTB2 count condition.
- Set timer B2 underflow as the timer A1, A2, and A4 start trigger.
- Enable dead time.
- Use the P7 and P8 U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ pins for three-phase output.

6.1 Operation Overview

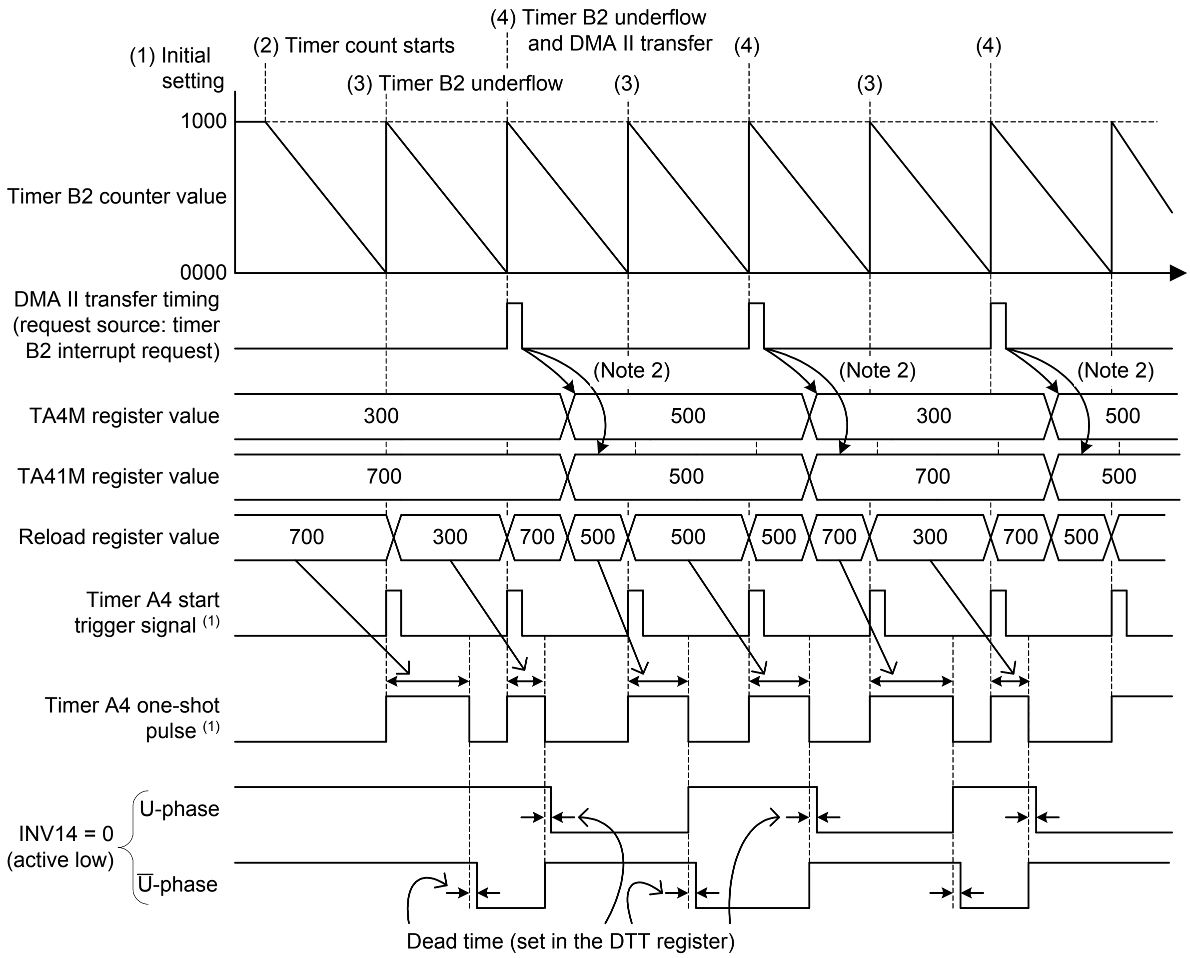
(1) Initial setting
Perform initial setting of three-phase motor control timers and DMAC II.

(2) Start timer count
Set 96h to the TABSR register, and start the count of timers A1, A2, A4, and B2. At this point, only timer B2 starts counting.

(3) Timer B2 underflow
When timer B2 underflows the first time, timers A1, A2, and A4 start counting.

(4) Timer B2 underflow and DMA II transfer
When timer B2 underflows the second time, timers A1, A2, and A4 start counting, a DMA II transfer occurs, and the timer Ai/timer Ai-1 mirror register values are rewritten (i = 1, 2, 4).

Figure 6.1 shows the U-Phase and $\overline{U}$-Phase Output Timing Diagram.



The above diagram assumes the following:
- The INV11 bit in the INVC1 register is 1 (three-phase mode 1)
- The ICTB2 register is 02h.

Notes:
1. Internal signal
2. Values for registers TA4M and TA41M are set using DMA II transfer.

Figure 6.1 U-Phase and $\overline{U}$-Phase Output Timing Diagram

6.2 Constant

Table 6.1 lists the Constant Used in the Sample Code.

Table 6.1 Constant Used in the Sample Code

Constant Name	Setting Value	Contents
D_DMAC2_DATA_MAX	6	Number of DMAC II transfers

6.3 Structure/Union List

Figure 6.2 shows the Structure/Union Used in the Sample Code.

```
/* DMAC II index */
struct{
  union {
    struct{
      int16_t size : 1;       /* Transfer size select bit */
      int16_t imm : 1;        /* Transfer source select bit */
      int16_t upds : 1;       /* Source addressing select bit */
      int16_t updd : 1;       /* Destination addressing select bit */
      int16_t oper : 1;       /* Calculation transfer select bit */
      int16_t brst : 1;       /* Burst transfer select bit */
      int16_t inte : 1;       /* DMA II transfer complete interrupt select bit */
      int16_t chain : 1;      /* Chained transfer select bit */
      int16_t reserve : 7;    /* Reserved */
      int16_t mult : 1;       /* Multiple transfer select bit */
    }mod_bit;
    uint16_t mod_word;
  }mod;                       /* Transfer mode */
  uint16_t  count;            /* Transfer counter */
  uint16_t* sadr;             /* Source address */
  uint16_t* dadr;             /* Destination address */
  void (*iadr)(void);         /* DMA II transfer complete interrupt vector address */
}dm_index;
```

Figure 6.2 Structure/Union Used in the Sample Code

The interrupt vector for the peripheral function interrupt becomes the DMAC II request source. Set the DMAC II index starting address to the interrupt vector. In this document, the timer B2 interrupt is used as the request source for DMAC II.
Figure 6.3 shows a setting example of the asm function programmed in C.

```
asm(" .rvector 23, _dm_index");     /* Define DMAC II Index (Software Interrupt Number 23) */
```

Figure 6.3 Example of Setting the Peripheral Function Variable Vector Table When Using the Timer B2 Interrupt as the DMAC II Request Source

6.4 Variables

Table 6.2 lists the Global Variables.

Table 6.2 Global Variables

Type	Variable Name	Contents	Function Used
unsigned short	data1[ ][ ]	Timer A1, A2, and A4 setting values	timer_init
unsigned char	flg_timer_value	Flag for when timer A1, A2, and A4 setting values change	main, dmac2_int

6.5 Functions

Table 6.3 lists the Functions.

Table 6.3 Functions

Function Name	Outline
dmac2_init	DMAC II initial setting
timer_init	Initial setting for the three-phase motor control timer
dmac2_int	DMAC II transfer completed interrupt handling

6.6 Function Specifications

The following tables list the sample code function specifications.

dmac2_init	
Outline	DMAC II initial setting
Header	None
Declaration	void dmac2_init(void)
Description	Perform the initial setting of the DMAC II.
Argument	None
Returned value	None
Remark	The DMAC II request source is allocated to software interrupt number 23 (interrupt source is timer B2).

timer_init	
Outline	Initial setting for three-phase motor control timers
Header	None
Declaration	void timer_init(void)
Description	• Perform the initial setting of the three-phase motor control timers (timers A1, A2, A4, and B2) • Set the P7 and P8 U, $\overline{U}$, V, $\overline{V}$, W, and $\overline{W}$ pins to three-phase output.
Argument	None
Returned value	None
Remark	

dmac2_int	
Outline	DMAC II transfer complete interrupt handling
Header	None
Declaration	void dmac2_int(void)
Description	Change the timer A setting value and set the DMAC II index.
Argument	None
Returned value	None
Remark	

6.7 Flowcharts

6.7.1 Main Processing

Figure 6.4 shows the Main Processing.

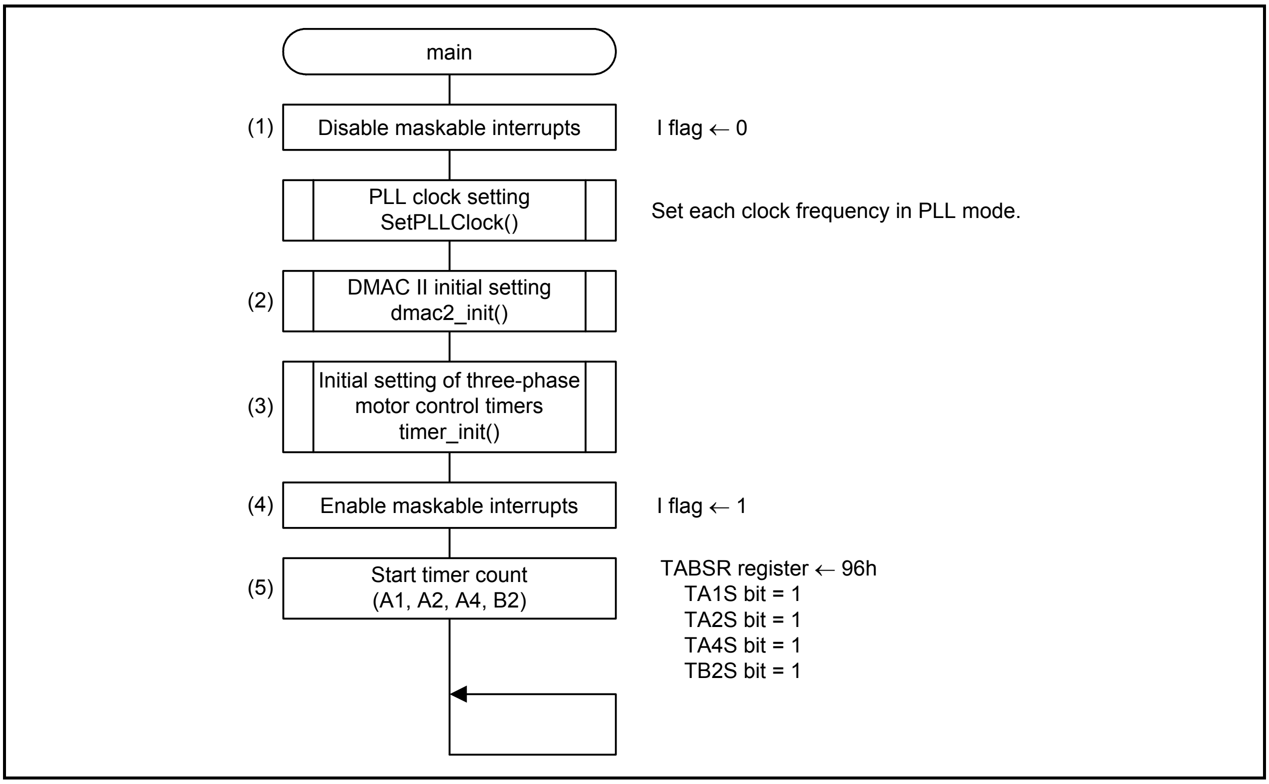


Figure 6.4 Main Processing

6.7.2 DMAC II Initial Setting

Figure 6.5 shows the initial setting for DMAC II.

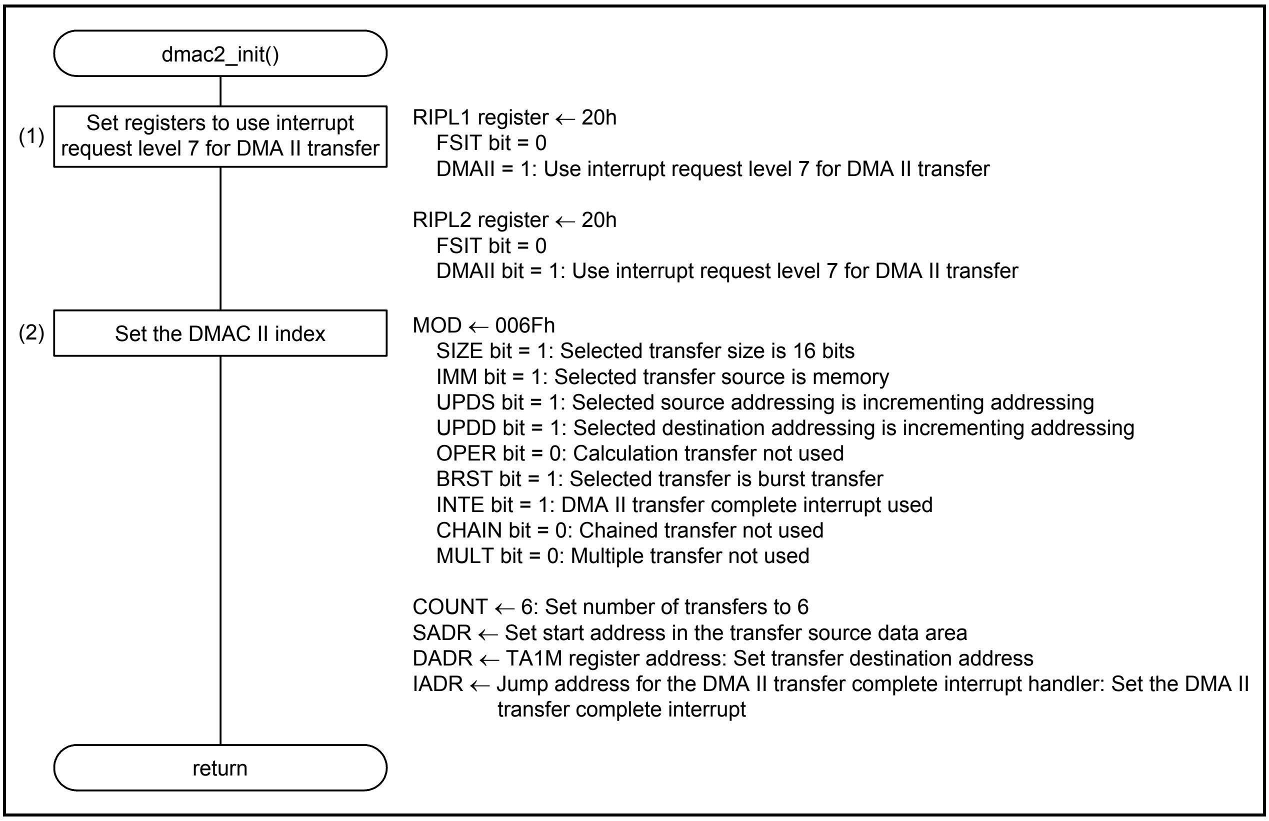


Figure 6.5 DMAC II Initial Setting

6.7.3 Initial Setting of the Three-Phase Motor Control Timers

Figure 6.6 and Figure 6.7 show the initial setting of the three-phase motor control timers.

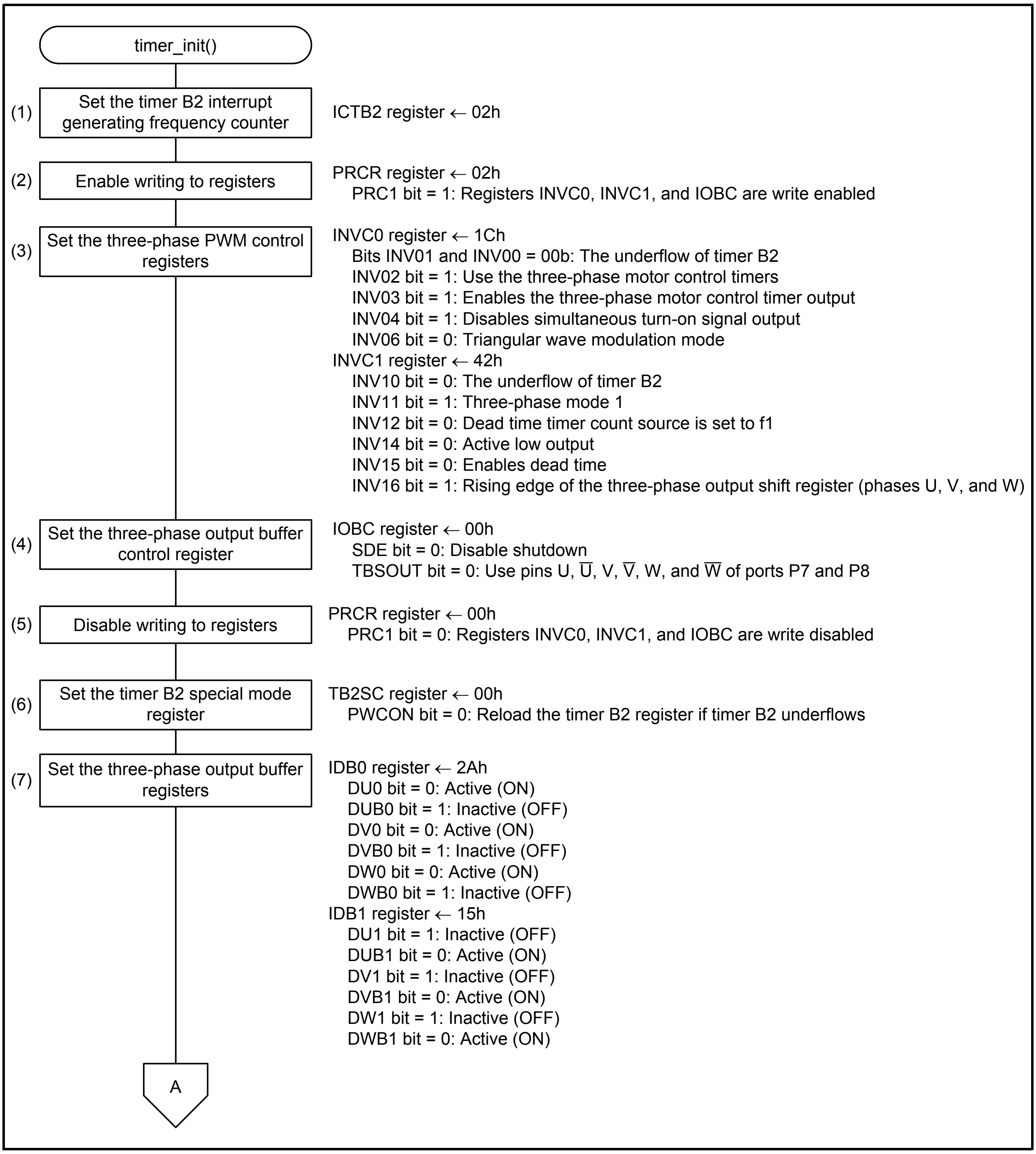


Figure 6.6 Initial Setting of the Three-Phase Motor Control Timers (1/2)

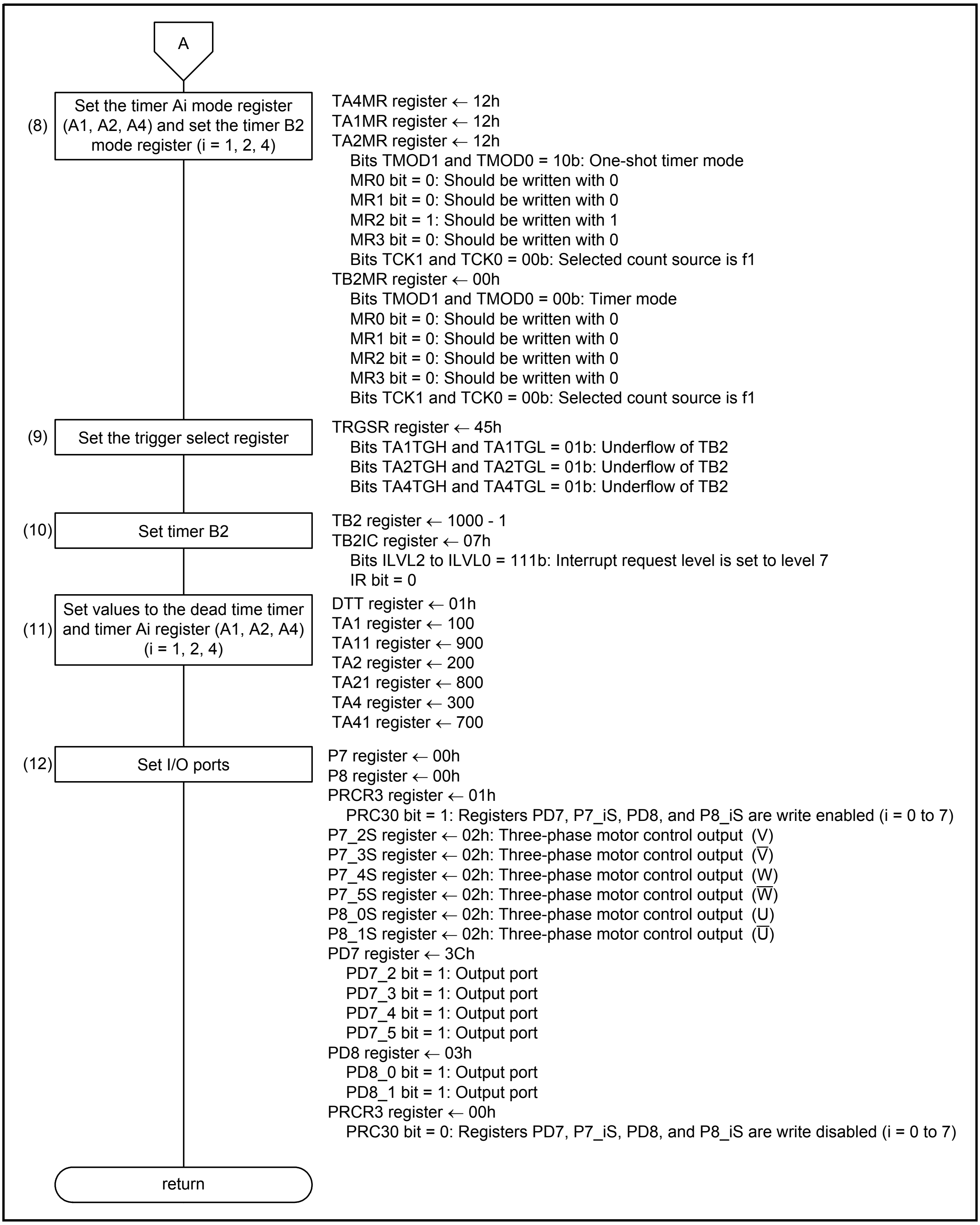


Figure 6.7 Initial Setting of the Three-Phase Motor Control Timers (2/2)

6.7.4 DMAC II Transfer Complete Interrupt Handling

Figure 6.8 shows the transfer complete interrupt handling.

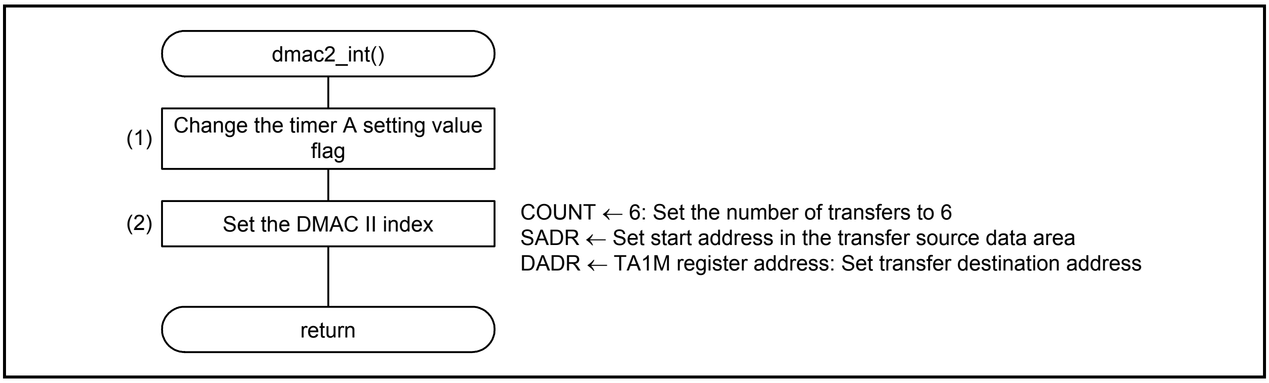


Figure 6.8 DMAC II Transfer Complete Interrupt Handling

7. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

8. Reference Documents

R32C/120 Group User's Manual: Hardware Rev.1.10
R32C/121 Group User's Manual: Hardware Rev.1.10
R32C/145 Group User's Manual: Hardware Rev.1.00
R32C/151 Group User's Manual: Hardware Rev.1.10
R32C/152 Group User's Manual: Hardware Rev.1.10
R32C/153 Group User's Manual: Hardware Rev.1.10
R32C/156 Group User's Manual: Hardware Rev.1.10
R32C/157 Group User's Manual: Hardware Rev.1.10
R32C/160 Group User's Manual: Hardware Rev.1.02
R32C/161 Group User's Manual: Hardware Rev.1.02
The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual
R32C/100 Series C Compiler Package V.1.02
C Compiler User's Manual Rev.2.00
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Revision History	R32C/100 Series Using Mirror Registers with Three-Phase Motor Control Timers While in Triangular Wave Modulation Mode and Three-Phase Mode 1

Rev.	Date	Description	
		Page	Summary
1.00	Feb. 24, 2012	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6278-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Lavied' or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141

Colophon 1.1