
R8C/25 Group

R01AN1285EJ0110

Timer RA in Pulse Output Mode

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1. Abstract

This document describes how to set up and use the timer RA in pulse output mode on the R8C/25 Group device.

2. Introduction

The application example described in this document is applied to the following:

- MCU: R8C/25 Group

This program can be used with other R8C/Tiny Series which have the same SFR (special function register) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

Note on oscillation stabilization wait time

In chapter 4.2.1 , select the high-speed on-chip oscillator after starting the high-speed on-chip oscillator and waiting until oscillation stabilizes.

3. Applications

3.1 Timer RA

Timer RA is an 8-bit timer with an 8-bit prescaler.

The prescaler and timer each consist of a reload register and counter. The reload register and counter are allocated at the same address, and can be accessed when accessing registers TRAPRE and TRA.

Figure 3.1 shows a Block Diagram of Timer RA.

Time RA has the following five modes:

- Timer mode: The timer counts the internal count source.
- Pulse output mode: The timer counts the internal count source and outputs pulses of which polarity inverted by underflow of the timer.
- Event counter mode: The timer counts external pulses.
- Pulse width measurement mode: The timer measures the pulse width of an external pulse.
- Pulse period measurement mode: The timer measures the pulse period of an external pulse.

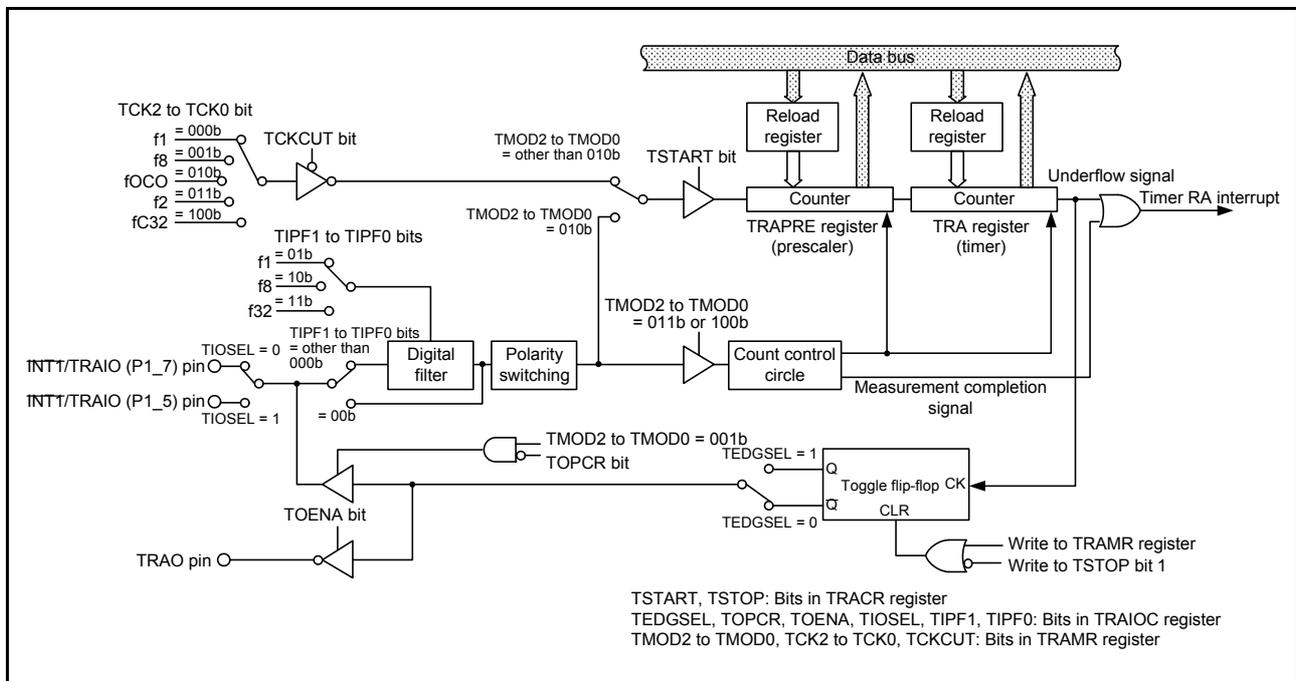


Figure 3.1 Block Diagram of Timer RA

3.2 Pulse Output Mode

In pulse output mode, the internally generated count source is counted, and a pulse with inverted polarity is output from the TRAI0 pin each time the timer underflows (refer to Table 3.1)

Figure 3.2 shows Registers TRACR and TRAI0C in Pulse Output Mode, and Figure 3.3 shows Registers TRAMR, TRAPRE, and TRA in Pulse Output.

Table 3.1 Pulse Output Mode Specifications

Item	Specification
Count source	f1, f2, f8, fOCO, fC32
Count operations	<ul style="list-style-type: none"> • Decrement • When the timer underflows, the contents in the reload register is reloaded and the count is continued.
Divide ratio	$1/(n+1)(m+1)$ n: Value set in TRAPRE register, m: Value set in TRA register
Count start condition	1 (count starts) is written to the TSTART bit in the TRACR register.
Count stop conditions	<ul style="list-style-type: none"> • 0 (count stop) is written to the TSTART bit in the TRACR register. • 1 (count forcibly stops) is written to the TSTOP bit in the TRACR register.
Interrupt request generation timing	<ul style="list-style-type: none"> • When timer RA underflows [timer RA interrupt].
INT1/TRAI0 pin function	Pulse output, programmable output port, or INT1 interrupt ⁽¹⁾
TRAO pin function	Programmable I/O port or inverted output of TRAI0 ⁽¹⁾
Read from timer	The count value can be read by reading registers TRA and TRAPRE.
Write to timer	<ul style="list-style-type: none"> • When registers TRAPRE and TRA are written while the count is stopped, values are written to both the reload register and counter. • When registers TRAPRE and TRA are written during the count, values are written to the reload register and counter (refer to 3.3 Timer Write Control during Count Operation).
Select functions	<ul style="list-style-type: none"> • TRAI0 output polarity switch function The TEDGSEL bit in the TRAI0C register selects the level at the start of pulse output.⁽¹⁾ • TRAO output function Pulses inverted from the TRAI0 output polarity can be output from the TRAO pin (selectable by the TOENA bit in the TRAI0C register). • Pulse output stop function Output from the TRAI0 pin is stopped by the TOPCR bit in the TRAI0C register. • INT1/TRAI0 pin select function P1_7 or P1_5 is selected by the TIOSEL bit in the TRAI0C register.

NOTES:

1. The level of the output pulse becomes the level when the pulse output starts when the TRAMR register is written to.

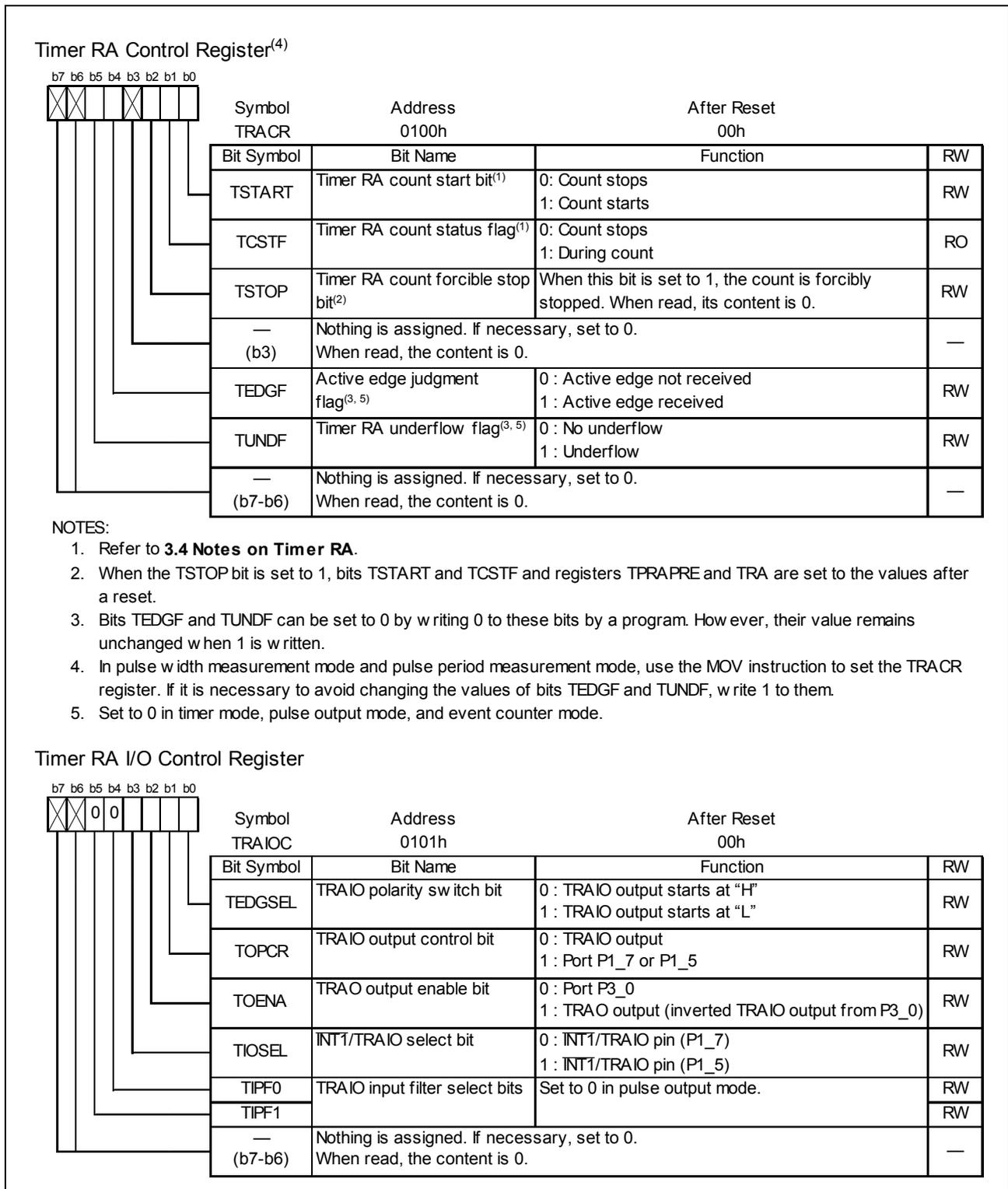


Figure 3.2 Registers TRACR and TRAI0C in Pulse Output Mode

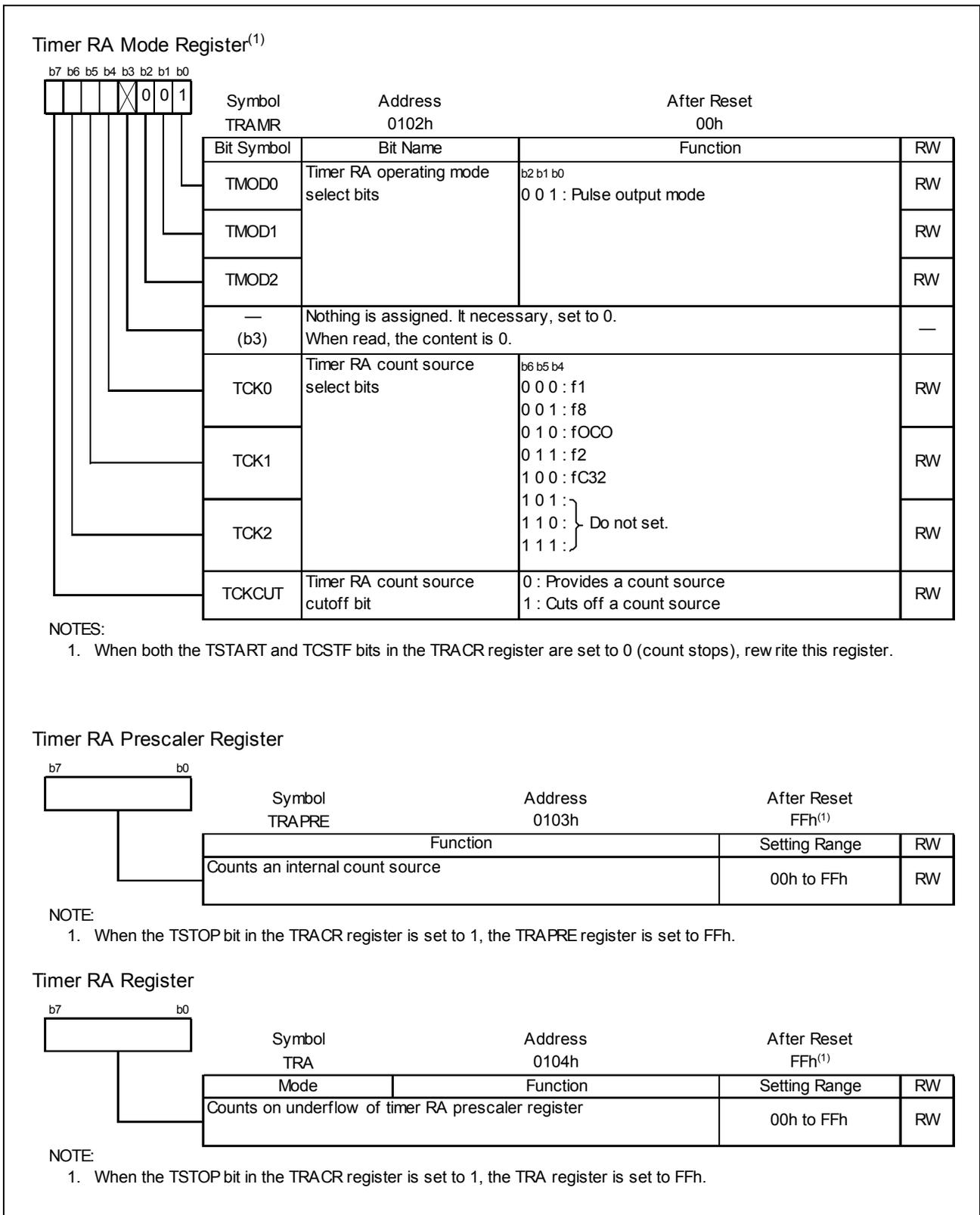


Figure 3.3 Registers TRAMR, TRAPRE, and TRA in Pulse Output

3.3 Timer Write Control during Count Operation

Timer RA has a prescaler and a timer (which counts the prescaler underflows). The prescaler and timer each consist of a reload register and a counter. When writing to the prescaler or timer, values are written to both the reload register and counter.

However, values are transferred from the reload register to the counter of the prescaler in synchronization with the count source. In addition, values are transferred from the reload register to the counter of the timer in synchronization with prescaler underflows. Therefore, if the prescaler or timer is written to when count operation is in progress, the counter value is not updated immediately after the WRITE instruction is executed. Figure 14.5 shows an Operating Example of Timer RA when Counter Value is Rewritten during Count Operation.

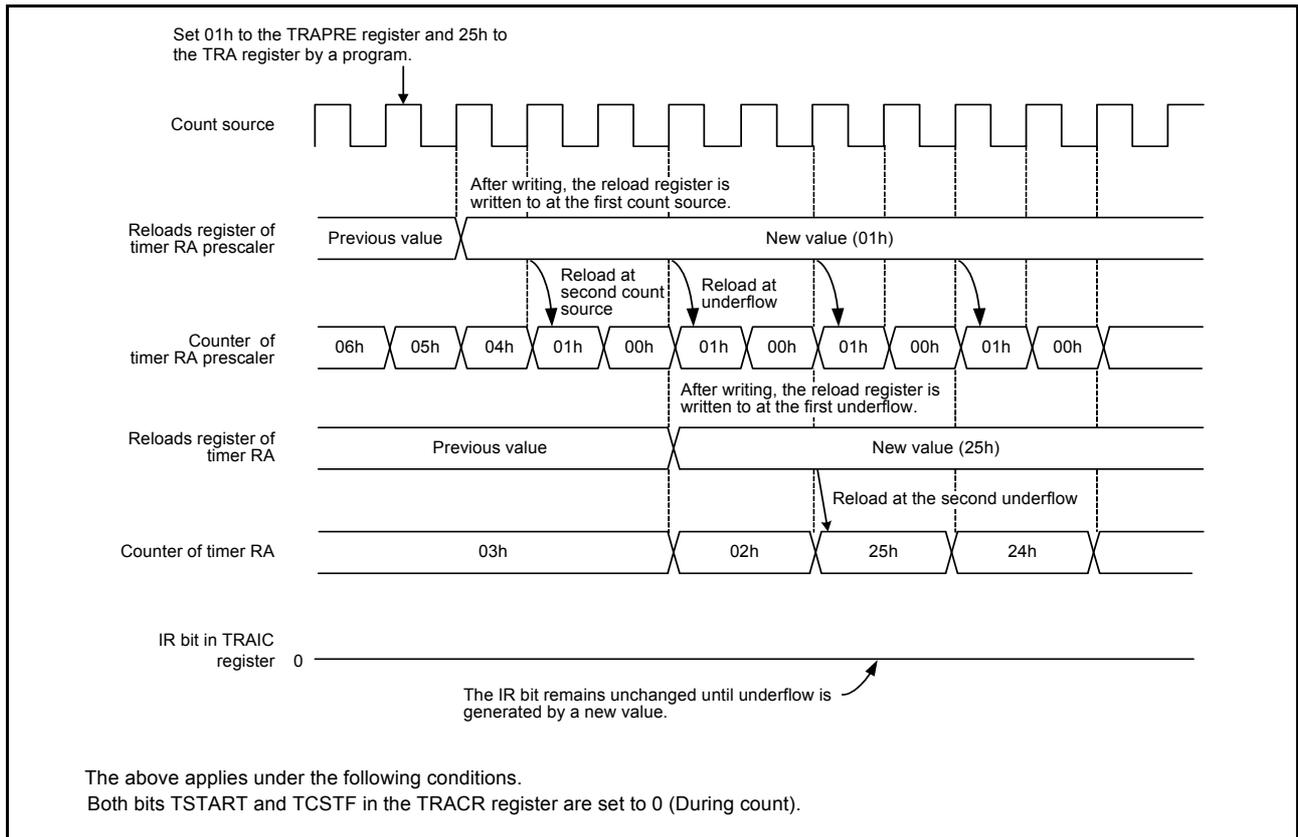


Figure 3.4 Operating Example of Timer RA when Counter Value is Rewritten during Count Operation

3.4 Notes on Timer RA

- Timer RA stops counting after a reset. Set the values in the timer RA and timer RA prescalers before the count starts.
- Even if the prescaler and timer RA are read out in 16-bit units, these registers are read 1 byte at a time by the MCU. Consequently, the timer value may be updated during the period when these two registers are being read.
- In pulse period measurement mode, bits TEDGF and TUNDF in the TRACR register can be set to 0 by writing 0 to these bits by a program. However, these bits remain unchanged if 1 is written. When using the READ-MODIFY-WRITE instruction for the TRACR register, the TEDGF or TUNDF bit may be set to 0 although these bits are set to 1 while the instruction is being executed. In this case, write 1 to the TEDGF or TUNDF bit which is not supposed to be set to 0 with the MOV instruction.
- When changing to pulse period measurement mode from another mode, the contents of bits TEDGF and TUNDF are undefined. Write 0 to bits TEDGF and TUNDF before the count starts.
- The TEDGF bit may be set to 1 by the first timer RA prescaler underflow generated after the count starts.
- When using the pulse period measurement mode, leave two or more periods of the timer RA prescaler immediately after the count starts, then set the TEDGF bit to 0.
- The TCSTF bit retains 0 (count stops) for 0 to 1 cycle of the count source after setting the TSTART bit to 1 (count starts) while the count is stopped.
- During this time, do not access registers associated with timer RA⁽¹⁾ other than the TCSTF bit. Timer RA starts counting at the first valid edge of the count source after The TCSTF bit is set to 1 (during count).
- The TCSTF bit remains 1 for 0 to 1 cycle of the count source after setting the TSTART bit to 0 (count stops) while the count is in progress.
- During this time, do not access registers associated with timer RA⁽¹⁾ other than the TCSTF bit.
- Timer RA counting is stopped when the TCSTF bit is set to 0.

NOTE:

1. Registers associated with timer RA: TRACR, TRAIOC, TRAMR, TRAPRE, and TRA.

4. Program Overview

In pulse output mode, a pulse with inverted polarity will be output from the TRAIO pin at 1 ms.

$$1 \text{ ms} = f_{\text{OCO}}^{(1)} \times (\text{TRAPRE register setting value} + 1) \times (\text{TRA register setting value} + 1) \\ = 25 \text{ ns (40 MHz)} \times 4 (\text{FRA2} = 0x02: \text{divide-by-4 mode}) \times (99 + 1) \times (99 + 1)$$

NOTE:

- fOCO is a clock generated by the high-speed on-chip oscillator. It is applied with at the divide ratio set by the high-speed on-chip oscillator control register (FRA2).

This program uses the following functions:

- Select the $\overline{\text{INT1}}$ /TRAIO (P1_7) pin.
- Start TRAIO output at “H” from the TRAIO pin.
- Start inverted TRAIO output from the TRAIO pin.
- Select fOCO as timer RA counter source.

Figure 4.1 shows the Pin Used.

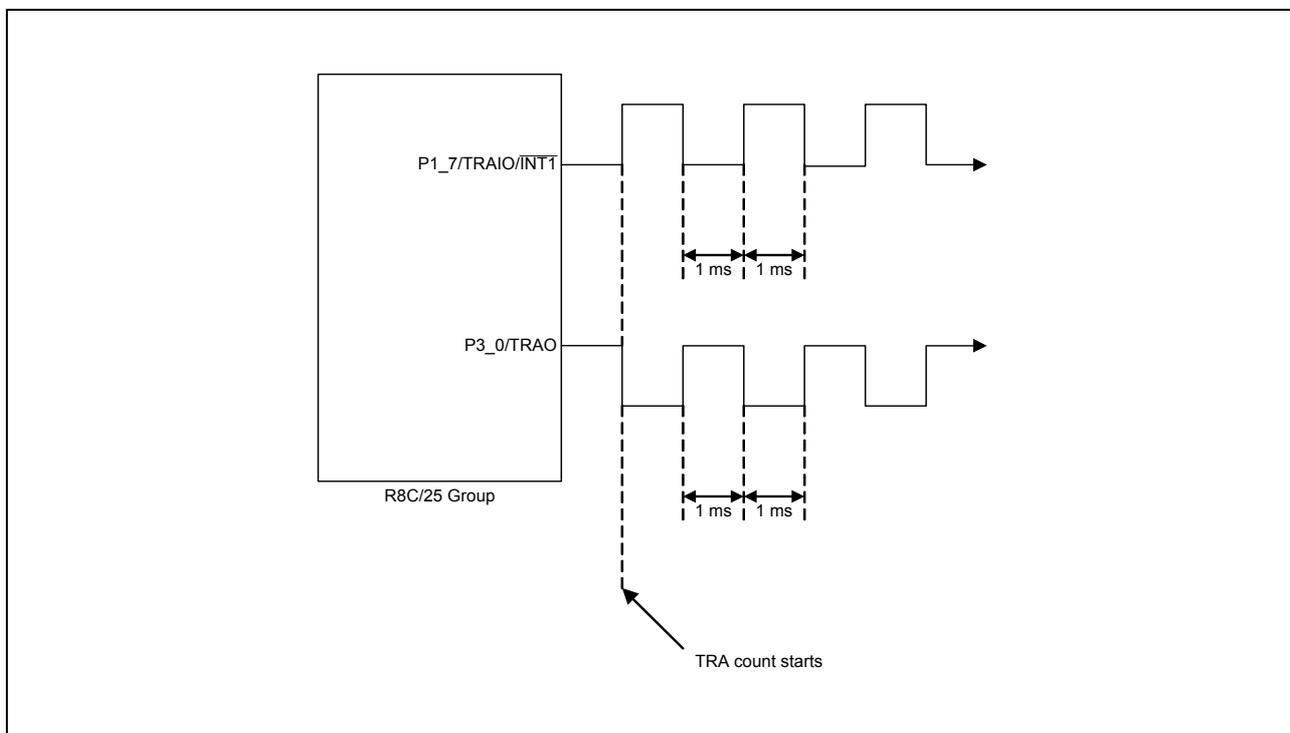


Figure 4.1 Pin Used

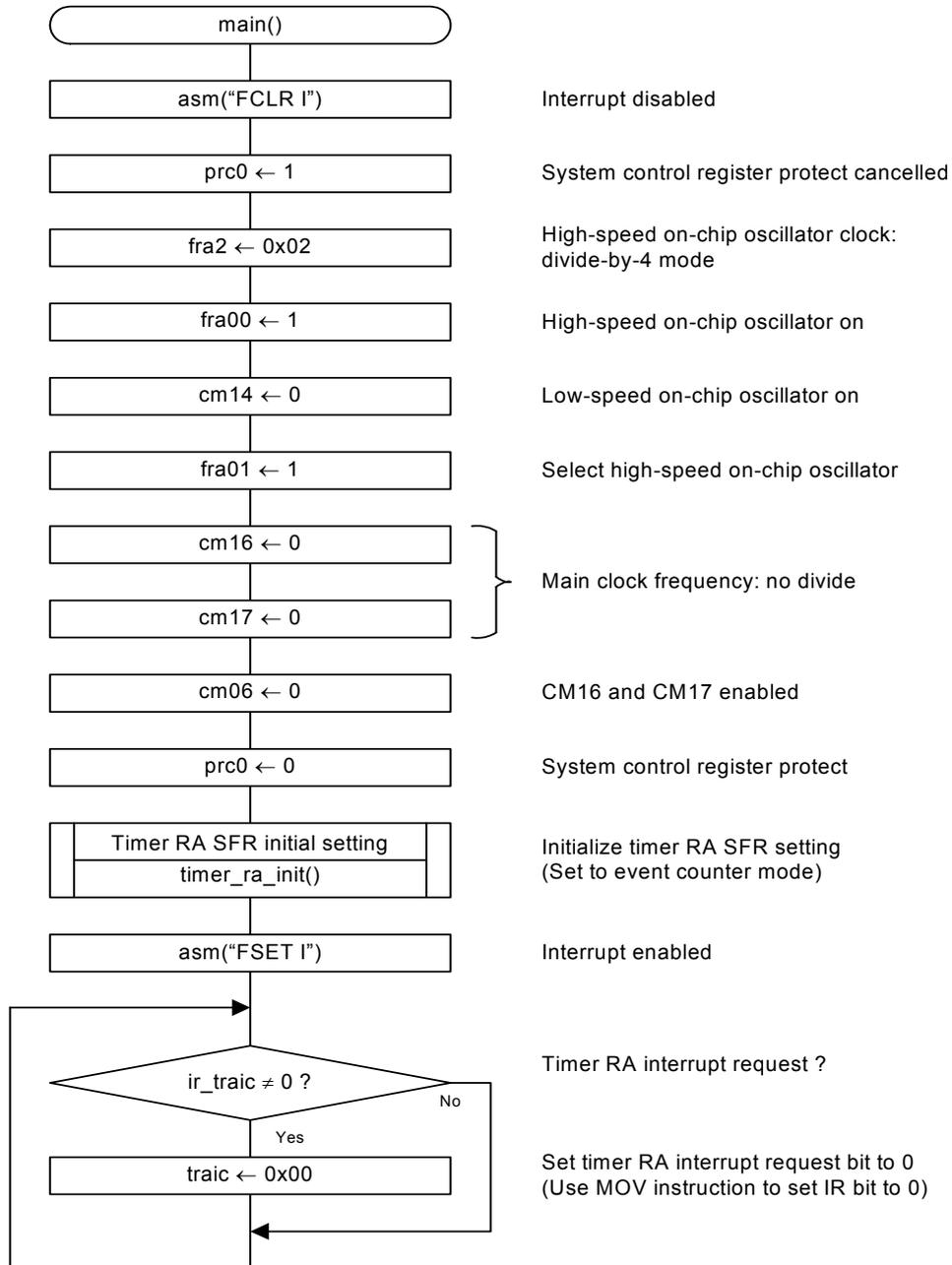
4.1 Function Table

Table 4.1

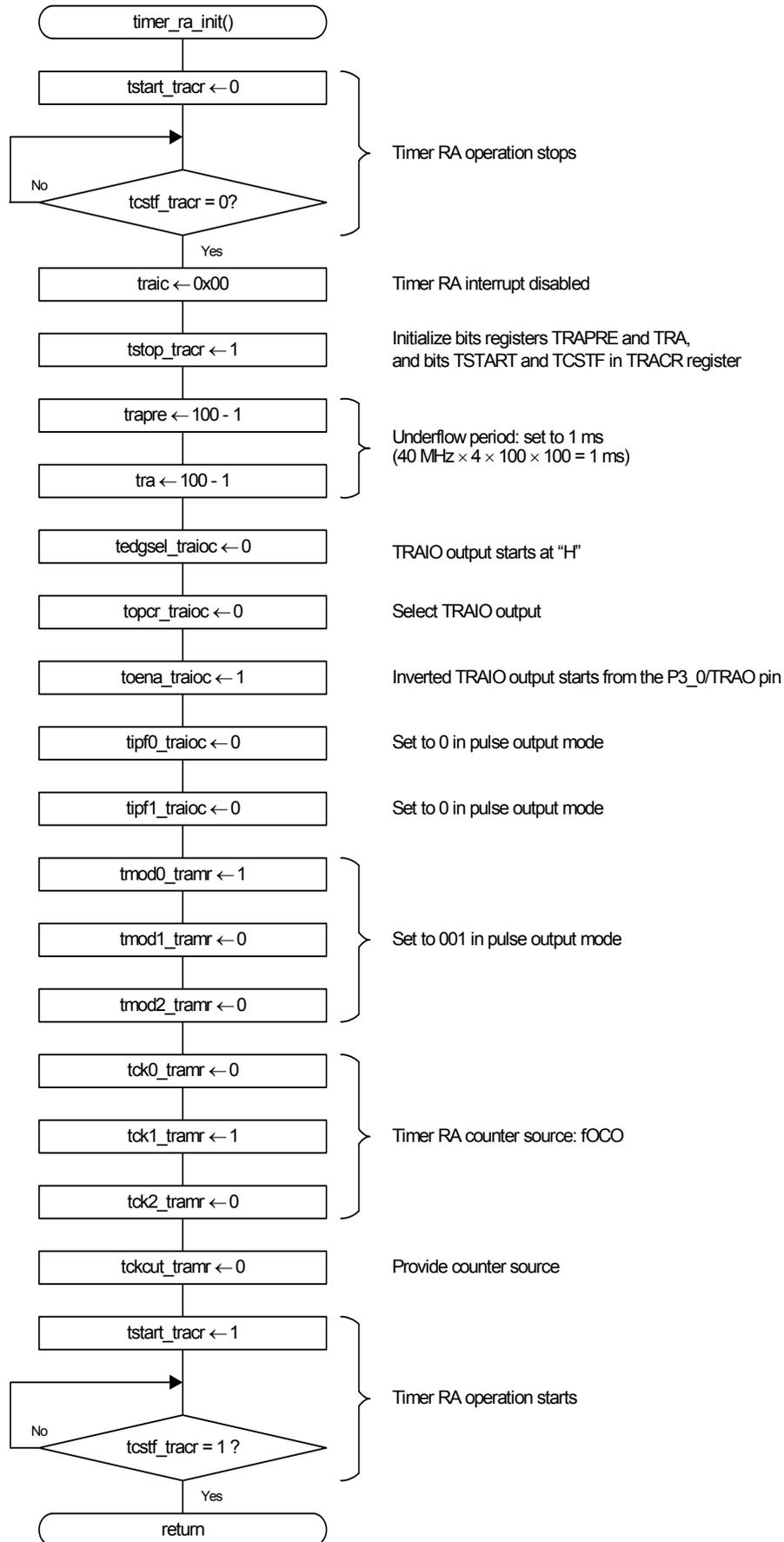
Declaration	void timer_ra_init(void)		
Overview	SFR initial setting associated with timer RA		
Argument	Argument name	Meaning	
	None		
Variable used (global)	Variable name	Usage	
	None		
Return value	Type	Value	Meaning
	None		
Function	Initialize the SFR registers associated with time RA		

4.2 Flow Chart

4.2.1 Main functions



4.2.2 Timer RA SFR Initial Setting



5. Sample Programming Code

Download a sample program from the Renesas Electronics website.

6. Reference Document

User's Manual: Hardware

R8C/25 Group Hardware Manual

(Download the latest version from the Renesas Electronics website.)

Technical News/Technical Update

(Download the latest information from the Renesas Electronics website.)

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REVISION HISTORY	R8C/25 Group Timer RA in Pulse Output Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Sep 15, 2006	–	First Edition issued
1.10	June 1, 2012	1	Note on oscillation stabilization wait time added
		–	Previous document number: REJ05B0829

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1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
1 HarbourFront Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: +65-6213-0200, Fax: +65-6276-8001

Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-3390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
11F., Samik Laved or Bldg., 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141