

RISC-V

Timer Array Unit (Pulse Interval Measurement: Width)

Introduction

This application note describes how the timer array unit (TAU) measures the interval of the pulse. This unit detects both the rising and falling edges of the pulse that are input to the timer input pin (TI02) and measures the high-level width and low-level width of the pulse. Then, measurement results are stored in the on-chip RAM.

Target Device

RISC-V

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.

Contents

1.	Specifications	3
1.1	Overview of Specifications	3
1.2	Outline of Operation	4
2.	Operation Confirmation Conditions	5
3.	Hardware Descriptions	6
3.1	Example of Hardware Configuration	6
3.2	List of Pins to be Used	6
4.	Software Explanation	7
4.1	Setting of Option Byte	7
4.2	List of Constants	7
4.3	List of Variables	7
4.4	List of Functions	8
4.5	Specification of Functions	8
4.6	Flowcharts	9
4.6.1	Main Processing	9
4.6.2	TAU0 Channel 2 Capture End Interrupt Processing	10
5.	Sample Code	12
6.	Reference Documents	12
	Revision History	13

1. Specifications

1.1 Overview of Specifications

This application note describes the measurement of the high-level width and low-level width of the input pulse by using channel 2 of the timer array unit 0 (TAU0).

Each time a valid edge is detected on the timer input pin (TI02), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM. The type of the detected edge is determined by reading the input data in the PCNTR1 register when a valid edge is detected on the timer input pin (TI02).

Table 1.1 shows the required peripheral functions and their uses. Figure 1.1 presents an overview of the pulse interval measurement.

Table 1.1 Peripheral Function and Use

Peripheral Function	Use
Timer array unit 0 (TAU0) channel 2	Measurement of the interval of the pulse input to the timer input pin (TI02)

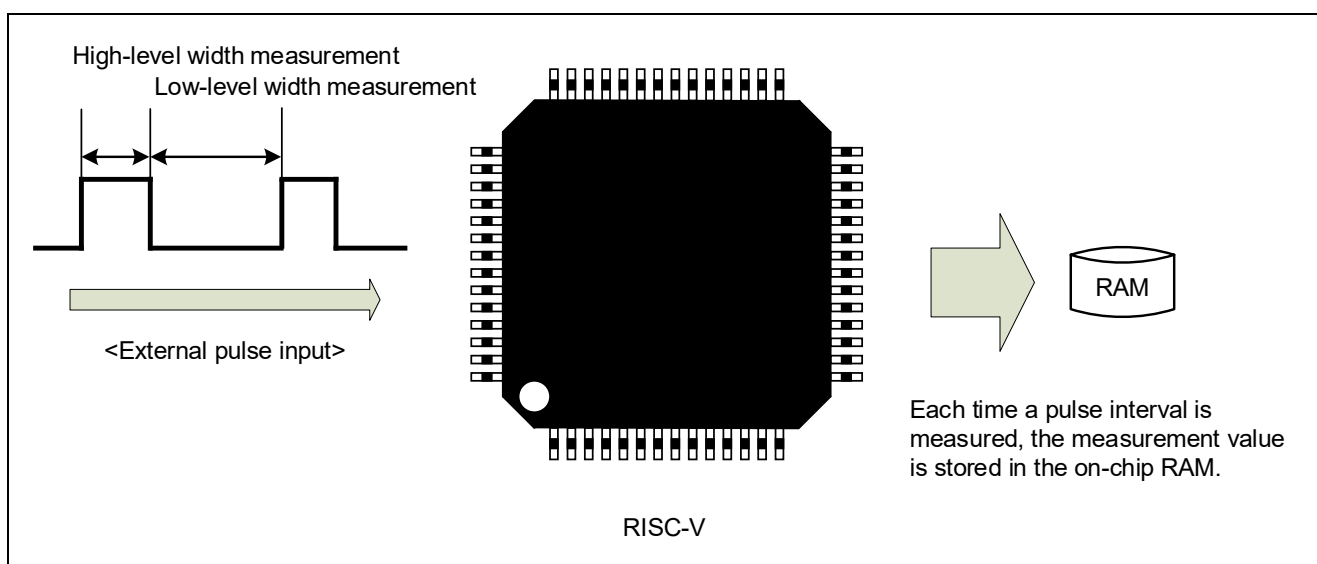


Figure 1.1 Overview of Pulse Interval Measurement

1.2 Outline of Operation

In this sample code, each time a rising edge or a falling edge is detected on the timer input pin (TI02), the counter value of the timer is captured and a high-level width or a low-level width of the pulse input to the timer input pin (TI02) is measured.

To measure the pulse interval accurately, the capture end interrupts of channel 2 of TAU0 (TAU0_ENDI2) after the first capture end interrupt are used. When capture end interrupts occur after the first capture end interrupt, the type of the detected edge (rising or falling) is determined, and the determination result is reflected in the edge determination flag. Then, according to the edge determination flag, the measured high-level width or low-level width is stored in the appropriate variable in the on-chip RAM.

Note that if a short pulse is detected and a counter value of the timer is captured before the measurement result is stored in the variable in the on-chip RAM, the measurement result is discarded.

- (1) Initialize TAU0.
 - Use the P103/TI02 pin for inputting capture trigger.
 - Set the operation clock of TAU0 channel 2 to PCLKB.
 - Set TAU0 channel 2 to the capture mode.
 - Set the TI02 pin input valid edge to “Both edge”.
 - Set the capture trigger of TAU0 channel 2 to “Valid edge of the TI02 pin input”.
 - Use the capture end interrupt (TAU0_ENDI2) from TAU0 channel 2.
- (2) Set the TS[2] bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR02) to 0000H and starts counting.
- (3) Switch to a sleep mode and wait for a detection of a valid edge.
- (4) When a valid edge is detected, the count value of the TCR02 register is captured to the timer data register (TDR02), at the same time, the TCR02 register is cleared to 0000H, and the capture end interrupt (TAU0_ENDI2) is requested, and then a sleep mode is released. After a sleep mode is released, the capture end interrupt request flag is cleared. The first capture value of the TDR02 register is invalid and cannot be used.
- (5) Set the numbers of measurement times of the high-level width and low-level width.
- (6) Enable interrupt requests.
- (7) Switch to a sleep mode and wait for a detection of a valid edge.
- (8) When a valid edge is detected, a sleep mode is released, and in the capture end interrupt processing, the capture value of the TDR02 register is temporarily stored in the on-chip RAM.
- (9) Read the data of the PCNTR1 register twice to determine the detected edge.
- (10) If a valid edge is not detected during the capture end interrupt processing and the two data of the PCNTR1 register are same, the determination result (00H or 01H) of the PCNTR1 register is set to the edge determination flag. According to the value of the edge determination flag, either a high-level width or a low-level width is selected, and the capture value temporarily stored is stored in the variable in the on-chip RAM appropriately for the selected width type.
If a valid edge is detected during the capture end interrupt processing or the two data of the PCNTR1 register are not same, the capture value temporarily stored is not stored in the variable in the on-chip RAM, and the capture end interrupt request flag is cleared, and the number of the discarded edge is incremented.
- (11) Repeat steps (7) to (10) until high-level widths and low-level widths are measured four times each.
- (12) After the measurement of the setting number is finished, set the TT[2] bit of the timer channel stop register 0 (TT0) to 1 to disable count operation, and switch to a sleep mode.

2. Operation Confirmation Conditions

The operation of the sample code provided with this application note has been tested under the following conditions.

Table 2.1 Operation Confirmation Conditions

Item	Description
MCU used	RISC-V (R9A02G021)
Board used	RISC-V-48p Fast Prototyping Board (RTK9FPG021S000W0BJ)
Operating frequency	High-speed on-chip oscillator clock: 48 MHz CPU/peripheral hardware clock: 48 MHz
Operating voltage	3.3 V (can be operated at 1.6 V to 5.5 V)
Integrated development environment (e ² studio)	e ² studio V2024-01.1 (24.1.1) from Renesas Electronics Corp.
C compiler (e ² studio)	LLVM for RISC-V 17.0.2.202401
Smart configurator (SC)	Smart Configurator for RISC-V V24.1.1.v20240125-1623
Board support package (BSP)	V1.00 from Renesas Electronics Corp.

3. Hardware Descriptions

3.1 Example of Hardware Configuration

Figure 3.1 shows an example of the hardware configuration used in the application note.

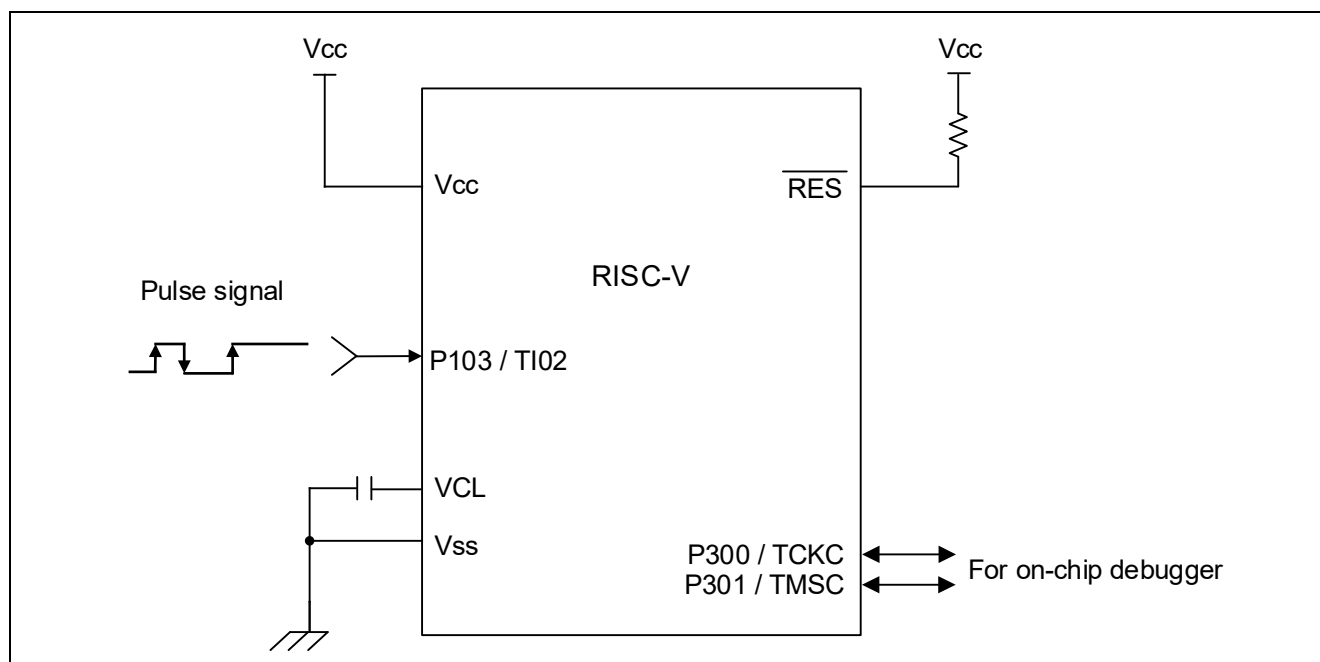


Figure 3.1 Hardware Configuration

Note 1. This simplified circuit diagram was created to show an overview of connections only. When actually designing your circuit, make sure the design includes appropriate pin handling and meets electrical characteristic requirements (connect each input-only port to Vcc or Vss through a resistor).

Note 2. Vcc must not be lower than the reset release voltage (VLVD0) that is specified for the LVD0.

3.2 List of Pins to be Used

Table 3.1 lists the pins to be used and their functions.

Table 3.1 Pins to be Used and Their Functions

Pin name	I/O	Function
P103 / TI02	Input	Timer input pin of TAU0 channel 2

Caution In this application note, only the used pins are processed. When actually designing your circuit, make sure the design includes sufficient pin processing and meets electrical characteristic requirements.

4. Software Explanation

4.1 Setting of Option Byte

Table 4.1 shows the option byte settings. Set the values that are most suited to your system as necessary.

Table 4.1 Option Byte Settings

Address	Setting Value	Contents
0000_0400H	FFFF_FFFFH	Disables the watchdog timer. (Counting stopped after reset)
0000_0404H	FFFF_CFFFH	High-speed on-chip oscillator clock : 48 MHz
0101_0008H	FFFF_FFFFH	Enables on-chip debugging

4.2 List of Constants

Table 4.2 shows the constants that are used in this sample program.

Table 4.2 Constants for the Sample Program

Constant	Setting	Description
_0001_TAU_OVERFLOW_OCCURS	0x0001U	Overflow occurrence is detected

4.3 List of Variables

Table 4.3 lists global variables.

Table 4.3 Global Variables

Type	Variable Name	Description	Function Used
volatile uint8_t	g_count	Number of times to measure pulse interval	main r_Config_TAU0_2_interrupt
volatile uint8_t	g_times_high	Number of times to measure high-level width	main r_Config_TAU0_2_interrupt
volatile uint8_t	g_times_low	Number of times to measure low-level width	main r_Config_TAU0_2_interrupt
volatile uint8_t	g_edge_flag	Edge determination flag	r_Config_TAU0_2_interrupt
uint8_t	g_port_data[2]	Storage of input level of P103/TI02 pin	r_Config_TAU0_2_interrupt
uint32_t	g_width_high[4]	Storage of measurement value of high-level width	r_Config_TAU0_2_interrupt
uint32_t	g_width_low[4]	Storage of measurement value of low-level width	r_Config_TAU0_2_interrupt
uint8_t	g_times_invalid	Number of times of discarded measurement value	r_Config_TAU0_2_interrupt
volatile uint32_t	g_tau0_ch2_width	Temporary storage of measurement value of pulse interval	r_Config_TAU0_2_interrupt

4.4 List of Functions

Table 4.4 shows a list of functions.

Table 4.4 Functions

Function name	Outline
r_Config_TAU0_2_interrupt()	TAU0 channel 2 capture end interrupt processing (TAU0_ENDI2)

4.5 Specification of Functions

The function specifications of the sample code are shown below.

r_Config_TAU0_2_interrupt()	
Outline	TAU0 channel 2 capture end interrupt processing
Header	r_cg_interrupt_handlers.h
Declaration	void r_Config_TAU0_2_interrupt(void)
Description	Determine the type of the input pulse edge and store the measured pulse interval in the variable in the on-chip RAM according to the detected edge.
Argument	None
Return Value	None

4.6 Flowcharts

4.6.1 Main Processing

Figure 4.1 shows the flowchart of the main processing.

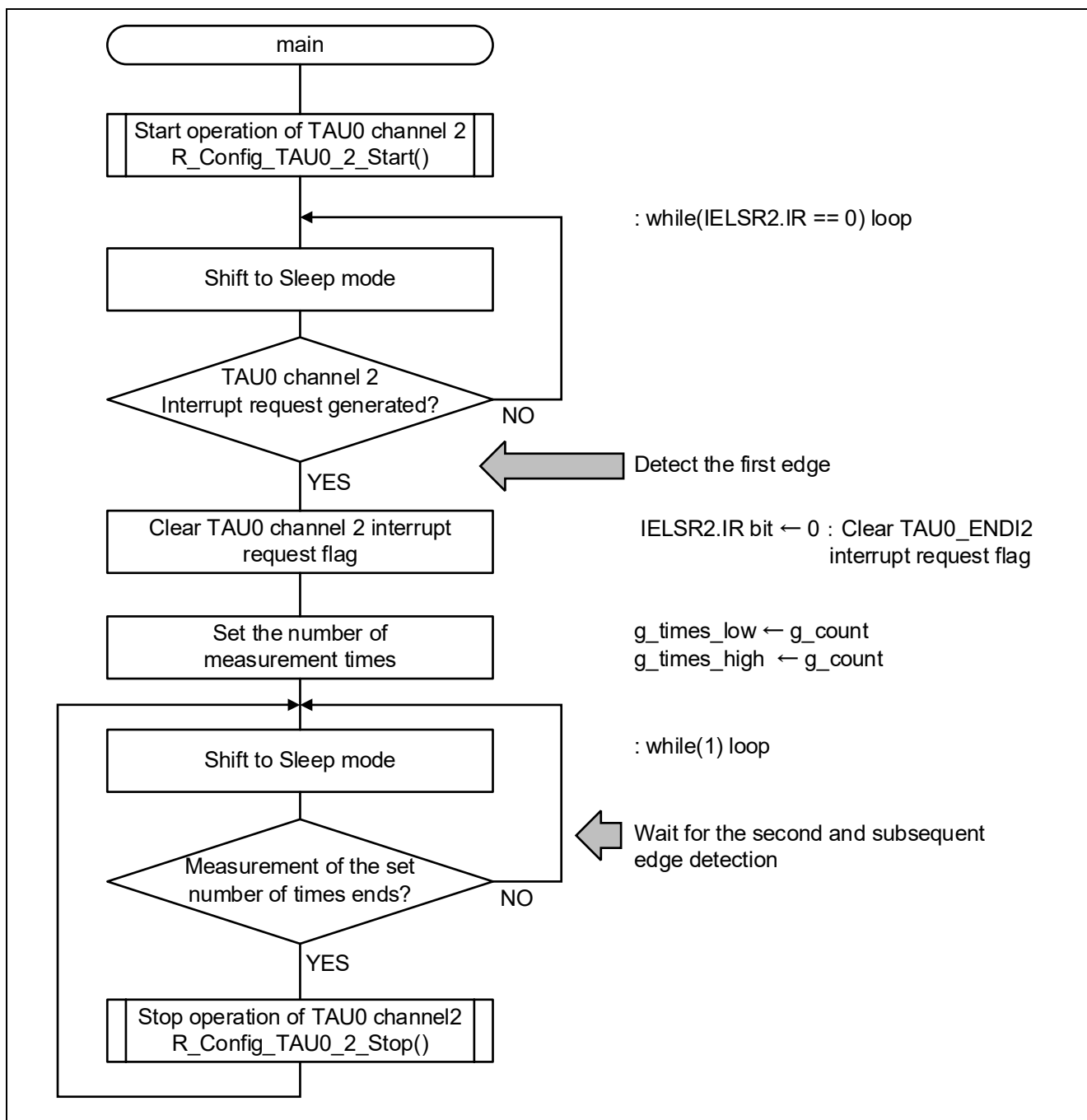


Figure 4.1 Main Processing

4.6.2 TAU0 Channel 2 Capture End Interrupt Processing

Figure 4.2 and Figure 4.3 show the flowchart of TAU0 channel 2 capture end interrupt processing.

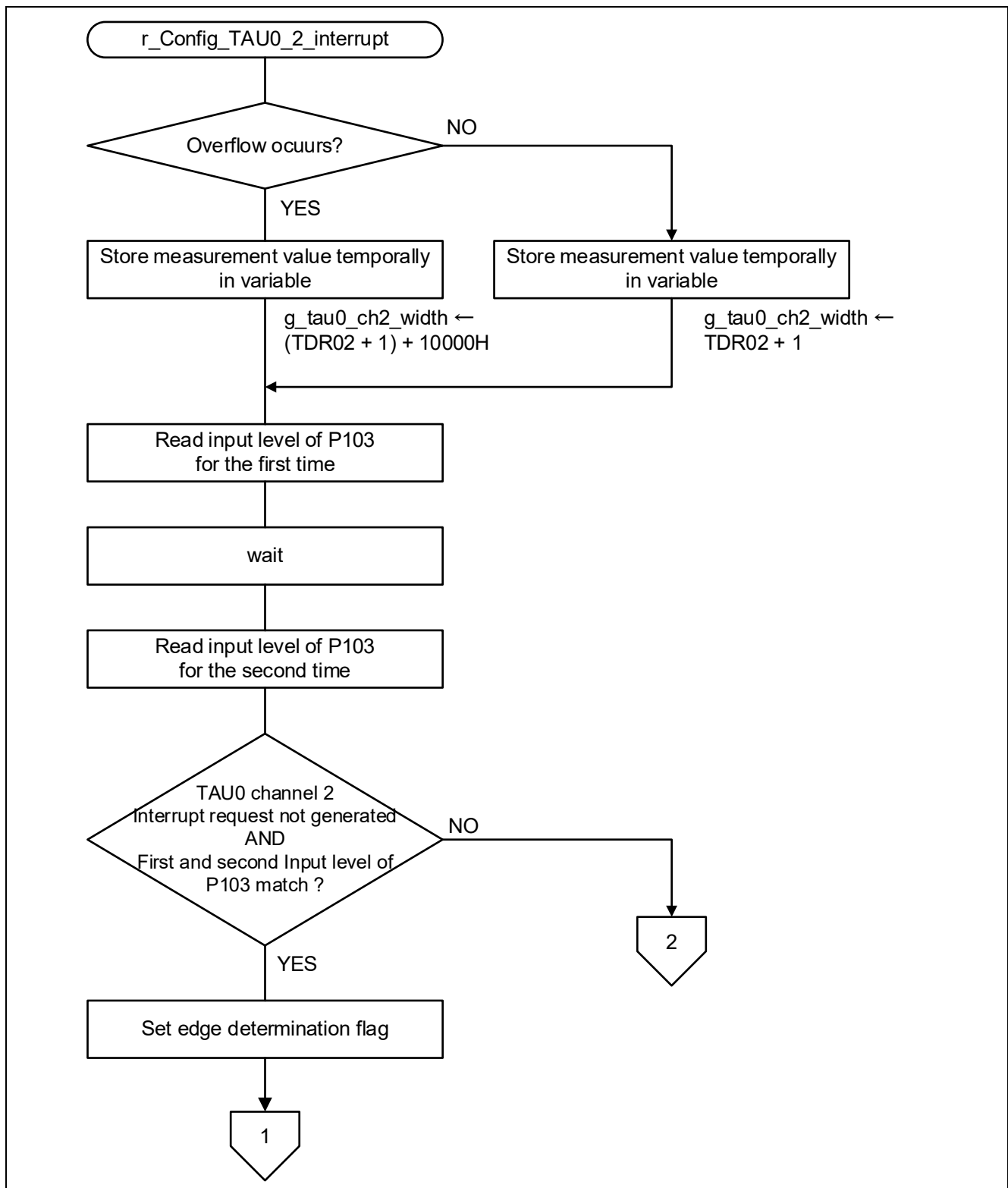


Figure 4.2 TAU0 Channel 2 Capture End Interrupt Processing (1/2)

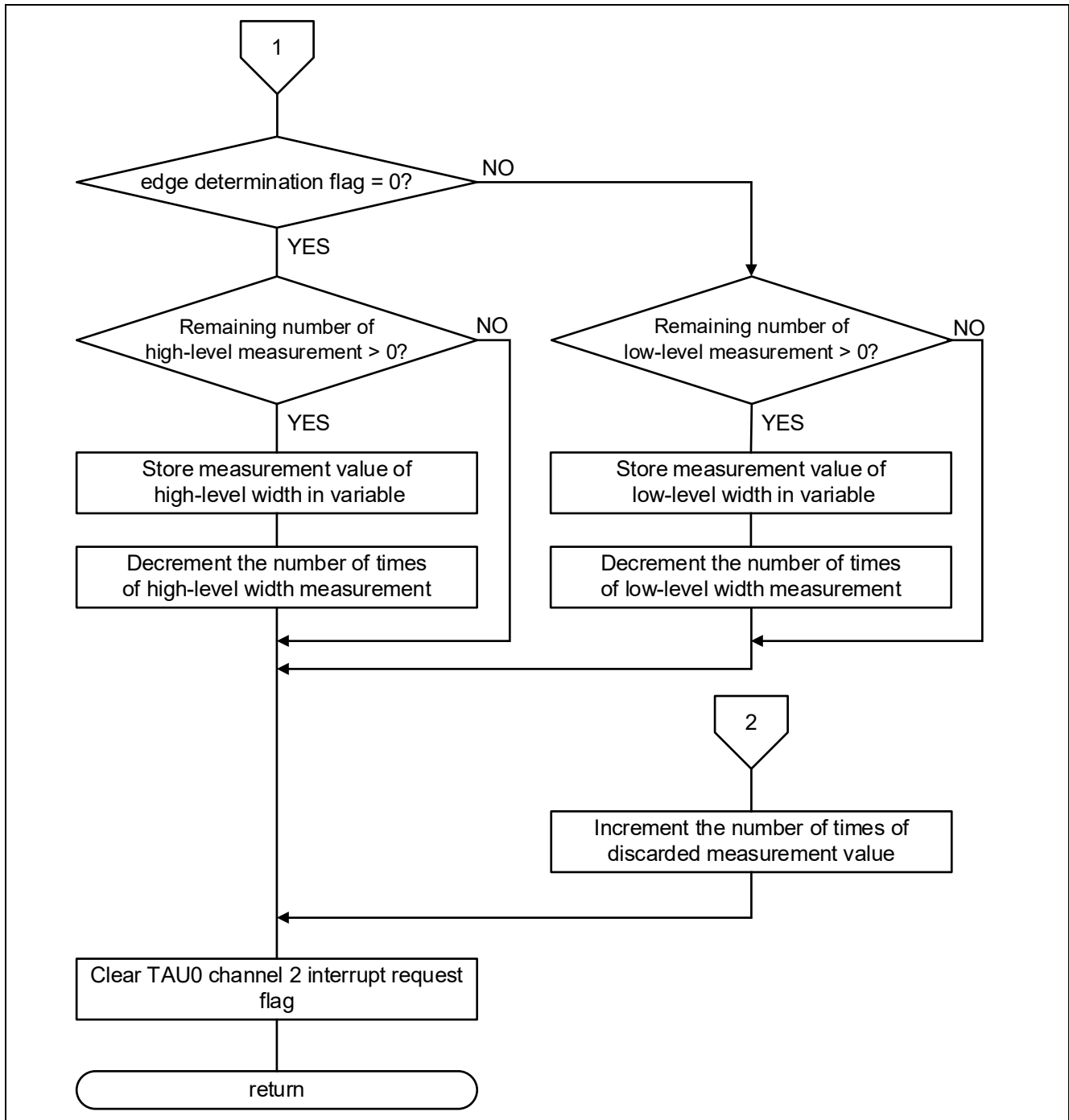


Figure 4.3 TAU0 Channel 0 Capture End Interrupt Processing (2/2)

5. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

6. Reference Documents

RISC-V User's Manual: Hardware (R01UH1036EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.24	—	Initial release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/.