RISC-V

Voltage Detection Circuits

Introduction

This application note explains how to use the three voltage detection circuits (LVDs) incorporated into the RISC-V microcontroller.

Target device

RISC-V

When applying this application note to another model of microcontroller, make the appropriate changes according to the microcontroller specifications and evaluate its operation extensively.

Contents

1. Overview of LVDs

The RISC-V microcontroller incorporates two voltage detection circuits, designated 0 (LVD0) and 1 (LVD1) and 2 (LVD2).

LVD0 compare the power supply voltage (Vcc) with a detection voltage (Vdet0) and generate an internal reset.

LVD1 and LVD2 compare the power supply voltage (Vcc) with a detection voltage (Vdet1 and Vdet2) and generate an internal reset or interrupt request signal.

During supply voltage rise, you must use LVD0 or an external reset signal to maintain a reset state until the power supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics. During supply voltage fall, the microcontroller must either transition to STOP mode or use LVD0 or an external reset signal to enter a reset state before VDD falls below the working voltage range.

1.1 LVD0

1.1.1 Setup method

Use the Option-Setting Memory (0x0000_0404 to 0x0000_0407) to set the operation mode and detection voltage (Vdet0) for LVD0.

1.1.2 Functionality

LVD0 compares the supply voltage (Vcc) with the detection voltage (Vdet0) and generates an internal reset. You can select one of five detection voltages (Vdet0).

LVD0 keeps the microcontroller in reset status until LVD0 detects Vcc ≥ Vdet0 during supply voltage rise. LVD0 generates an internal reset signal if it detects Vcc < Vdet0 at supply voltage fall, and then keeps the microcontroller in reset status until Vcc ≥ Vdet0 is detected.

Note: At supply voltage fall, LVD0 requires a detection delay of 500 µs before detecting Vcc < Vdet0 after the supply voltage (Vcc) falls below the detection voltage (Vdet0). If the detection voltage (Vdet0) is set to the lower limit of the working voltage range, the RISC-V unit will operate outside the working voltage range during the detection delay period. To avoid this issue, consider the amount of supply voltage fall that occurs during the detection delay period and set a detection voltage (Vdet0) such that the RISC-V unit always operates within its working voltage range.

1.2 LVD1

1.2.1 Setup method

LVD1 is inactive when the microcontroller exits reset status. Use the user program to set the operation mode and detection voltage (Vdet1) for LVD1. Operation mode is set with the LVCMPCR register. Detection voltage is set with the LDLVLR register.

The LVCMPCR register cannot be rewritten after the microcontroller exits reset status. Use the following procedure to permit rewriting of the LVCMPCR register and enable LVD1.

To allow the LVCMPCR register to be set from a user program, you must use LVD0 or an external reset signal to keep the microcontroller in reset status until the supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics.

(1) Writing 0xA508 to the PRCR register releases the protection for LVD related registers.
(2) Set registers related to LVD1.
(3) Writing 0xA500 to the PRCR register protects LVD related registers.
(4) LVD1 becomes active after the stabilization time (300us or longer) has elapsed.

1.2.2 Functionality

LVD1 compares the supply voltage (Vcc) to the detection voltage (Vdet1) and generates an internal reset or interrupt request signal. You can select one of sixteen detection voltages (Vdet1).

When LVD1 is activated in reset mode, LVD1 detects Vcc < Vdet1 and generates an internal reset. The reset initializes the voltage detection level register (LVCMPCR) and stops LVD1 operation. If LVD1 is activated while Vcc < Vdet1, then the microcontroller alternates between reset status (CPU stopped) and non-reset status (CPU operational) until Vcc ≥ Vdet1.

When LVD1 is activated in interrupt mode, LVD1 detects Vcc < Vdet1 and generates an interrupt request signal (voltage monitor 1 interrupt).

After the first detection, LVD1 detects Vcc < Vdet1 or Vcc ≥ Vdet1 and generates an interrupt request signal (voltage monitor 1 interrupt).

At power-on, normal operation (CPU operation) begins after the voltage stabilization time (typically T.B.D) and reset processing time have elapsed. Therefore, if normal operation starts while Vcc ≥ Vdet1, the above-described alternation between reset status and non-reset status does not occur, and no interrupt request signal (voltage monitor 1 interrupt) is generated at supply voltage rise. When starting normal operation while Vcc < Vdet1, take the precautionary measures explained in 3.4 Voltage fluctuation during supply voltage rise.

1.3 LVD2

1.3.1 Setup method

LVD2 is inactive when the microcontroller exits reset status. Use the user program to set the operation mode and detection voltage (Vdet2) for LVD2. Operation mode is set with the LVCMPCR register. Detection voltage is set with the LDLVLR register.

The LVCMPCR register cannot be rewritten after the microcontroller exits reset status. Use the following procedure to permit rewriting of the LVCMPCR register and enable LVD2.

To allow the LVCMPCR register to be set from a user program, you must use LVD0 or an external reset signal to keep the microcontroller in reset status until the supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics.

(1) Writing 0xA508 to the PRCR register releases the protection for LVD related registers.
(2) Set registers related to LVD2.
(3) Writing 0xA500 to the PRCR register protects LVD related registers.
(4) LVD2 becomes active after the stabilization time (1200 us or longer) has elapsed.

1.3.2 Functionality

LVD2 compares the supply voltage (Vcc) to the detection voltage (Vdet2) and generates an internal reset or interrupt request signal. You can select one of four detection voltages (Vdet2).

When LVD2 is activated in reset mode, LVD2 detects Vcc < Vdet2 and generates an internal reset. The reset initializes the voltage detection level register (LVCMPCR) and stops LVD2 operation. If LVD2 is activated while Vcc < Vdet2, then the microcontroller alternates between reset status (CPU stopped) and non-reset status (CPU operational) until Vcc ≥ Vdet2.

When LVD2 is activated in interrupt mode, LVD2 detects Vcc < Vdet2 and generates an interrupt request signal (voltage monitor 2 interrupt).

After the first detection, LVD2 detects Vcc < Vdet2 or Vcc ≥ Vdet2 and generates an interrupt request signal (voltage monitor 2 interrupt).

At power-on, normal operation (CPU operation) begins after the voltage stabilization time (typically T.B.D) and reset processing time have elapsed. Therefore, if normal operation starts while Vcc ≥ Vdet2, the above-described alternation between reset status and non-reset status does not occur, and no interrupt request signal (voltage monitor 2 interrupt) is generated at supply voltage rise. When starting normal operation while Vcc < Vdet2, take the precautionary measures explained in 3.4 Voltage fluctuation during supply voltage rise.

2. Selecting the LVD Operation Mode

When storing data at supply voltage fall

Use interrupt mode. Consider the amount of supply voltage fall that occurs during data storage processing and during the detection delay period and set a detection voltage such that the RISC-V unit always operates within its working voltage range.

- LVD1: Interrupt mode Note, LVD2: Interrupt mode (Condition: Vdet1 < Vdet2)
- LVD0: Reset mode, LVD1: Interrupt mode (Condition: Vdet0 < Vdet1)

Note: You must use LVD0 or an external reset signal to maintain a reset state until the supply voltage reaches the working voltage range described in the AC characteristics subcategory of the electrical characteristics. LVD0 can be used to release the initial internal reset after power-on.

When not using external reset

You must set up the LVD in such a way that the RISC-V always operates within the working voltage range. Consider the amount of supply voltage fall that occurs during the detection delay period and set a detection voltage that keeps the RISC-V within the working voltage range. Set the LVD to reset mode. If none of the five detection voltages (Vdet0) for LVD0 are suitable, you can use LVD0 and LVD1 or LVD2 in combination.

- LVD0: Reset mode, LVD1: Off
- LVD0: Reset mode, LVD1: Reset mode (Condition: Vdet0 < Vdet1)

The following settings are prohibited:

- LVD0: Reset mode, LVD1: Interrupt mode (Condition: Vdet0 > Vdet1)
- LVD0: Reset mode, LVD1: Reset mode (Condition: Vdet0 > Vdet1)

3. LVD Operation

This section explains how LVD0 and LVD1 and LVD2 work in combination.

3.1 LVD1: Interrupt mode, LVD2: Interrupt mode

Figure 3.1 shows the operation of the LVDs when LVD1 and LVD2 are both set to interrupt mode with the condition Vdet1 < Vdet2.

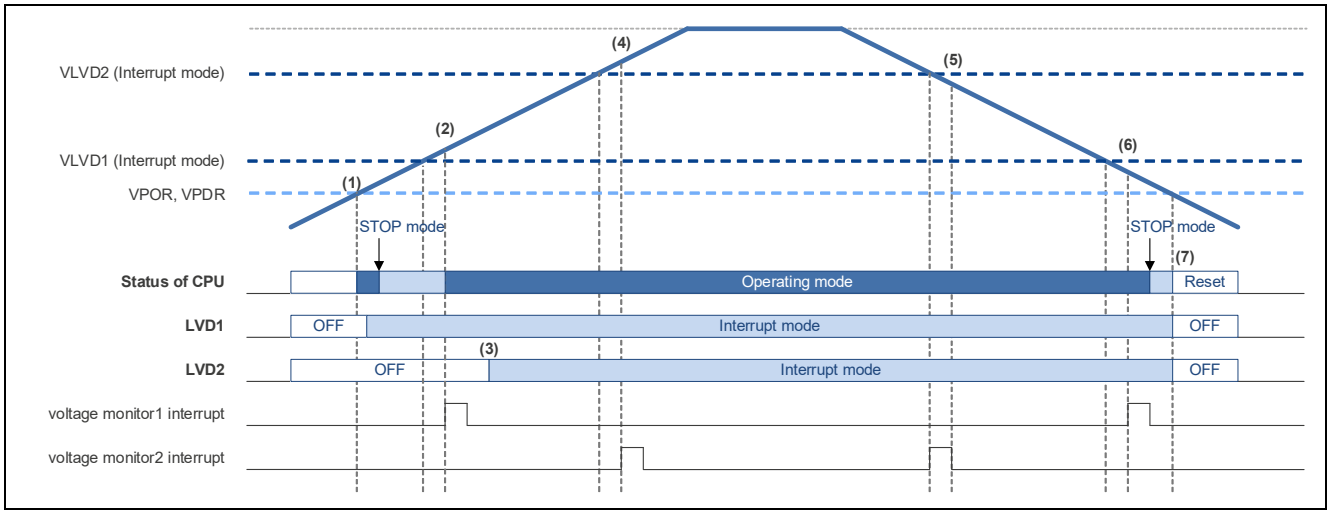

Figure 3.1 LVD operation when LVD0 and LVD1 are in interrupt mode with the condition VLVD0 < VLVD1

(1) LVD1 is activated by a user program.
(2) LVD1 detects Vcc ≥ Vdet1 and issues an interrupt request signal (voltage monitor 1 interrupt).
(3) LVD2 is activated by a user program.
(4) LVD2 detect Vcc ≥ Vdet2 and issues an interrupt request signal (voltage monitor 2 interrupt).
(5) LVD2 detects Vcc < Vdet2 and issues an interrupt request signal (voltage monitor 2 interrupt).
(6) LVD1 detects Vcc < Vdet1 and issues an interrupt request signal (voltage monitor 1 interrupt).
(7) After executing the processing in (6), the CPU enters STOP mode.

3.2 LVD0: Reset mode, LVD1: Interrupt mode

Figure 3.2 shows the operation of the LVDs when LVD0 is set to reset mode and LVD1 is set to interrupt mode with the condition Vdet0 < Vdet1.

Note that you cannot set LVD0 to reset mode and LVD1 to interrupt mode with the condition Vdet0 > Vdet1.

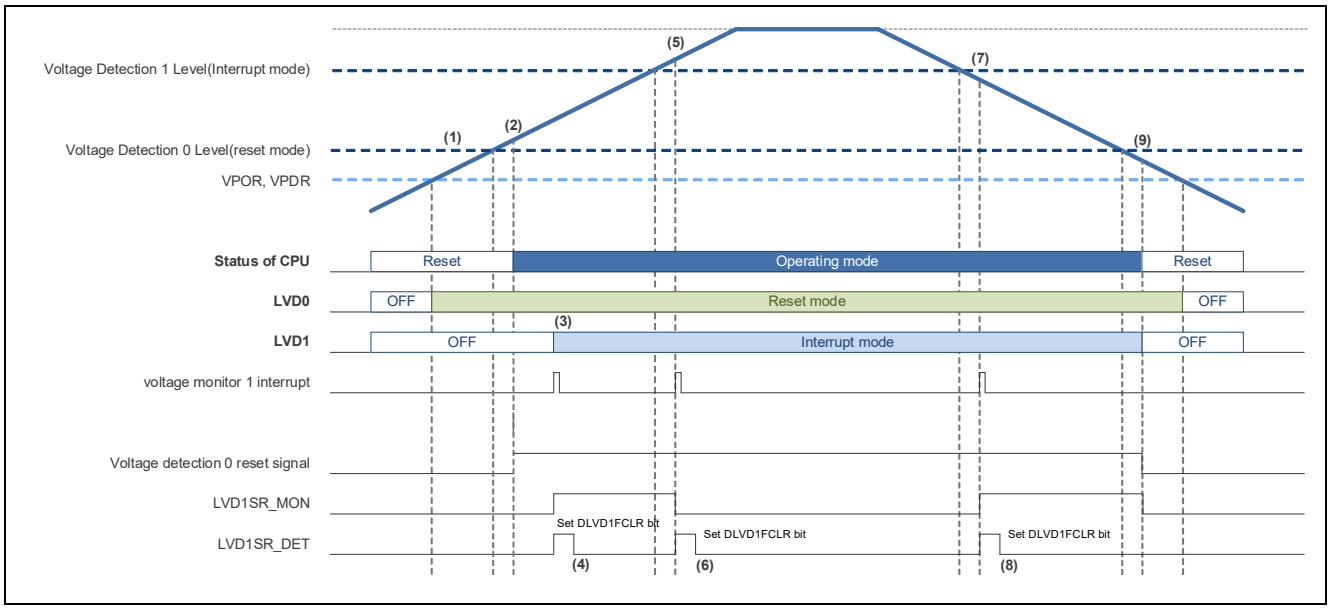

Figure 3.2 LVD operation with LVD0 in reset mode and LVD1 in interrupt mode with the condition Vdet0 < Vdet1

(1) LVD0 keeps the CPU in reset status.
(2) LVD0 detects Vcc ≥ Vdet0 and releases reset status.
(3) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects Vcc < Vdet1, and issues an interrupt request signal (voltage monitor 1 interrupt).
(4) A user program clears the DET flag of the LVD1SR register. The user program continues running as long as Vdet0 ≤ Vcc < Vdet1.
(5) LVD1 detects Vc ≥ Vdet1 and issues an interrupt request signal (voltage monitor 1 interrupt).
(6) A user program clears the DET flag of the LVD1SR register. The user program continues running as long as Vcc ≥ Vdet1.
(7) LVD1 detects Vcc < Vdet1 and issues an interrupt request signal (voltage monitor 1 interrupt).
(8) A user program clears the DET flag of the LVD1SR register. The user program continues running as long as Vdet0 ≤ Vcc < Vdet1.
(9) LVD0 detects Vcc < Vdet0 and generates an internal reset. LVD0 maintains a reset state until Vcc ≥ Vdet0.

Note: If LVD1 is set while Vcc ≥ Vdet1, no interrupt request signal is issued in steps (3) and (5), making steps (4) and (6) unnecessary.

3.3 LVD0: Reset mode, LVD1: Reset mode

Figure 3.3 shows the operation of the LVDs when LVD0 and LVD1 are both set to reset mode with the condition Vdet0 < Vdet1.

Note that you cannot set LVD0 and LVD1 to reset mode with the condition Vdet0 > Vdet1.

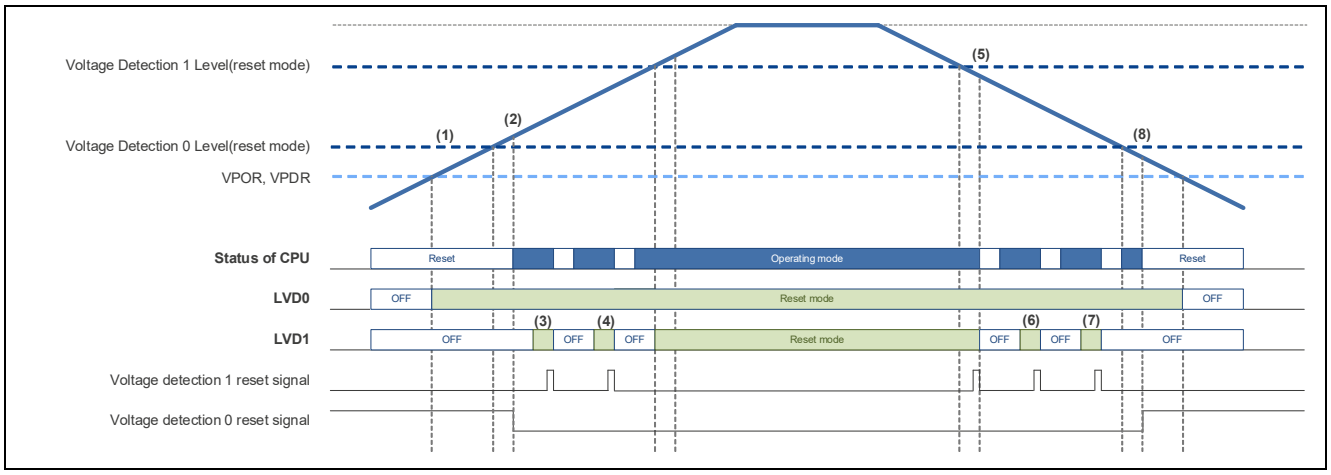

Figure 3.3 LVD operation with LVD0 and LVD1 in reset mode with the condition Vdet0 < Vdet1

(1) LVD0 keeps the CPU in reset status.
(2) LVD0 detects Vcc ≥ Vdet0 and releases reset status.
(3) LVD1 is set to reset mode in the user program and then activate it. When the stabilization time has elapsed, LVD1 becomes active, detects Vcc < Vdet1, and generates an internal reset.
(4) Step (3) repeats until LVD1 detects Vcc ≥ Vdet1.
(5) LVD1 detects Vcc < Vdet1 and generates an internal reset.
(6) LVD1 is activated by a user program. When the stabilization time has elapsed, LVD1 becomes active, detects Vcc < Vdet1, and generates an internal reset.
(7) Step (6) repeats until LVD0 detects Vcc < Vdet0.
(8) LVD0 detects Vcc < Vdet0 and generates an internal reset. LVD0 maintains a reset state until Vcc ≥ Vdet0.

Note: If LVD1 is set while Vcc ≥ Vdet1, no internal reset is generated in step (3). In this case, the processing in step (3) does not repeat in step (4).

3.4 Voltage fluctuation during supply voltage rise

Systems that exhibit a degree of fluctuation in the vicinity of the detection voltages of LVD0 and LVD1 (Vdet0 and Vdet1) might repeatedly enter and exit reset status. By taking the following steps, you can set an arbitrary time that must elapse after exiting reset status before the RISC-V unit begins operation. Measure in advance the time the power supply voltage takes to reach Vcc ≥ Vdet0 or Vcc ≥ Vdet1, and use the results to determine the time until RISC-V operation.

(1) The CPU exits reset mode.
(2) Check the RSTSR0 register to determine the cause of the reset.
    If the cause of the reset is POR or LVD, execute the processing in steps (3) and (4). If the cause of the reset is another internal reset, execute the processing from step (5) onward.
(3) Set the timer array unit to interval timer mode and start the counting process.
(4) Wait until the timer array unit issues an interrupt request signal. If a reset occurs while waiting, return to step (1).
(5) LVD1 is activated by a user program.
(6) Wait until the stabilization wait time of LVD1 (300 us) elapses as in steps (3) and (4).
(7) Start the initialization of ports and peripheral functions.
(8) Run the user program.

4. Reference Documents

RISC-V User's Manual: Hardware (R01UH1036EJ)

The latest versions can be downloaded from the Renesas Electronics website.

Technical update

The latest versions can be downloaded from the Renesas Electronics website.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.24	—	First Edition

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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