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# RL78 Family

R01AN3935EJ0101

Rev.1.01

## Processing Example when the WDT Window Open Period is set to 75%

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### Introduction

This application note describes a processing example when the window open period of the internal watchdog timer (here after WDT) is set to 75%.

### Target devices

RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15

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## 1. WDT Functionality and User Option Bytes to Use

In case of using WDT on the target device, setting of the user option byte (000C0H/020C0H) <sup>Note</sup> is mandatory. The interval interrupt function and related user option bytes used in this application note are described below.

Note: RL78/F12 is set by user option byte (000C0H/010C0H).

### •Interval interrupt

Interval interrupt can be generated when 75% of the overflow time +  $1 / 2 f_{WDT}$  is reached. From the WDTINT bit, user can set the use / non-use of this interval interrupt.

### •Window open period

Window open period can be set by WINDOW1 and WINDOW0 bits.

**Caution:** WDTSBYON bit is needed to set "1" (enables WDT counter during standby mode) to enable the window open period.

### •Overflow time

WDT overflow time which generates WDT reset can be set by WDCS0 to WDCS2 bits.

**Caution:** Do not set  $2^{13}/f_{WDT}$ ,  $2^{14}/f_{WDT}$  and  $2^{16}/f_{WDT}$ , if using interval interrupt in RL78/F13, RL78/F14 and RL78/F15.

### •Counter operation during standby mode

Counter operation (enabled / stop) during standby mode can be set by WDSTBYON bit.

For detail of the user option byte, refer to the user's manual: hardware.

## 2. Processing Example when the WDT Window Open Period is set to 75%

As an example of processing when the window open period is set to 75%, the processing to avoid the window close period and clear the WDT counter in standby mode (intermittent operation) is shown below.

Also, this chapter uses RL78/F13, F14 as examples.

### 2.1 Processing Example when Using the WDT Function

Figure 2-1 shows a processing example that returning from standby mode to normal mode by the WDT interval interrupt and clears the WDT counter (writes “ACH” to the WDTE register).

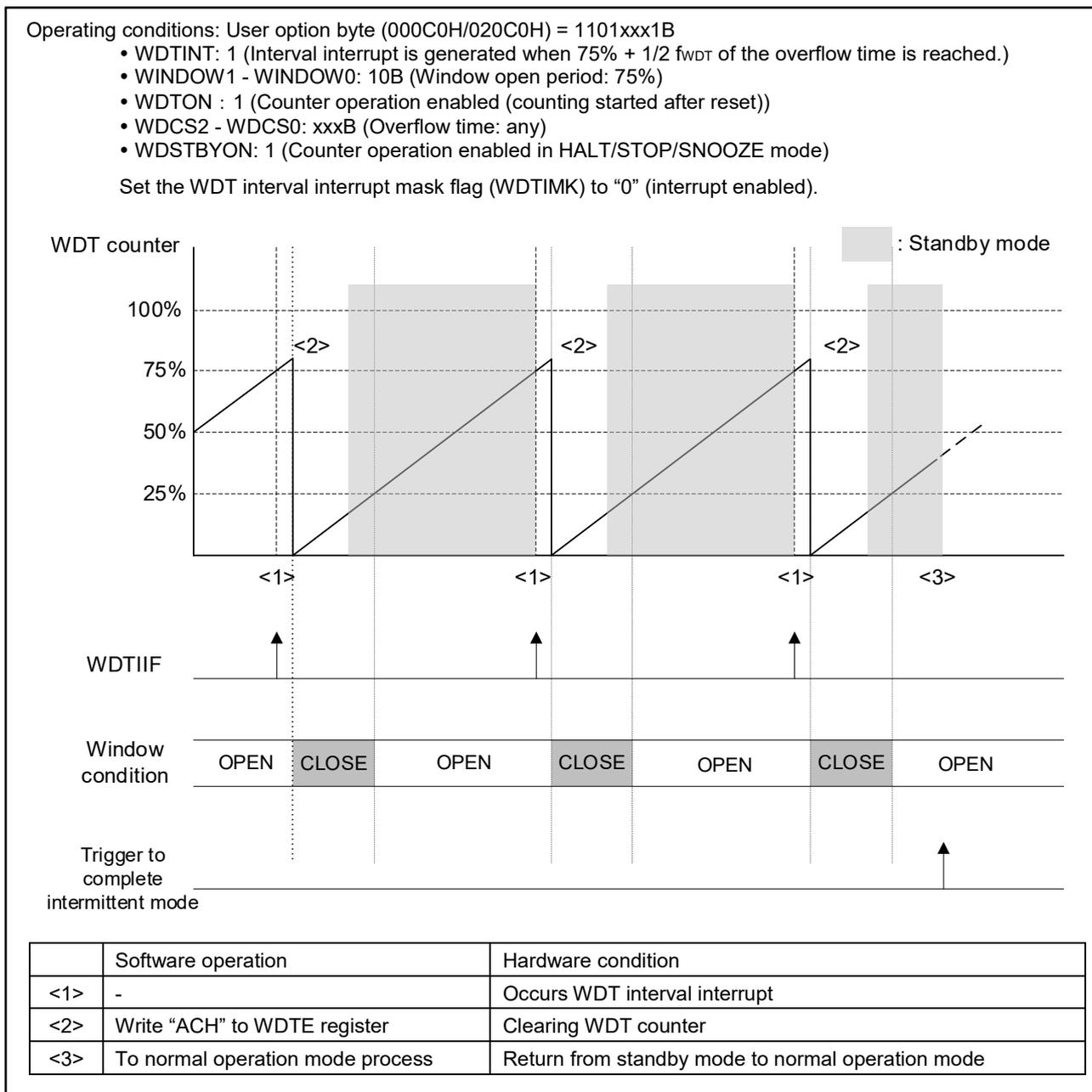


Figure 2-1 Processing Example when Using the WDT Function

## 2.2 Processing Example when Using Timer RJ

Figure 2-2 shows an example for a processing example when using Timer RJ. Uses the timer mode of Timer RJ for cyclic wake-up from standby mode. In the standby mode transition processing and return processing, check the WDT interval interrupt request flag (WDTIIF), and if it is “1” (75% of overflow time + 1/2 f<sub>WDT</sub> reached), the WDT counter is cleared.

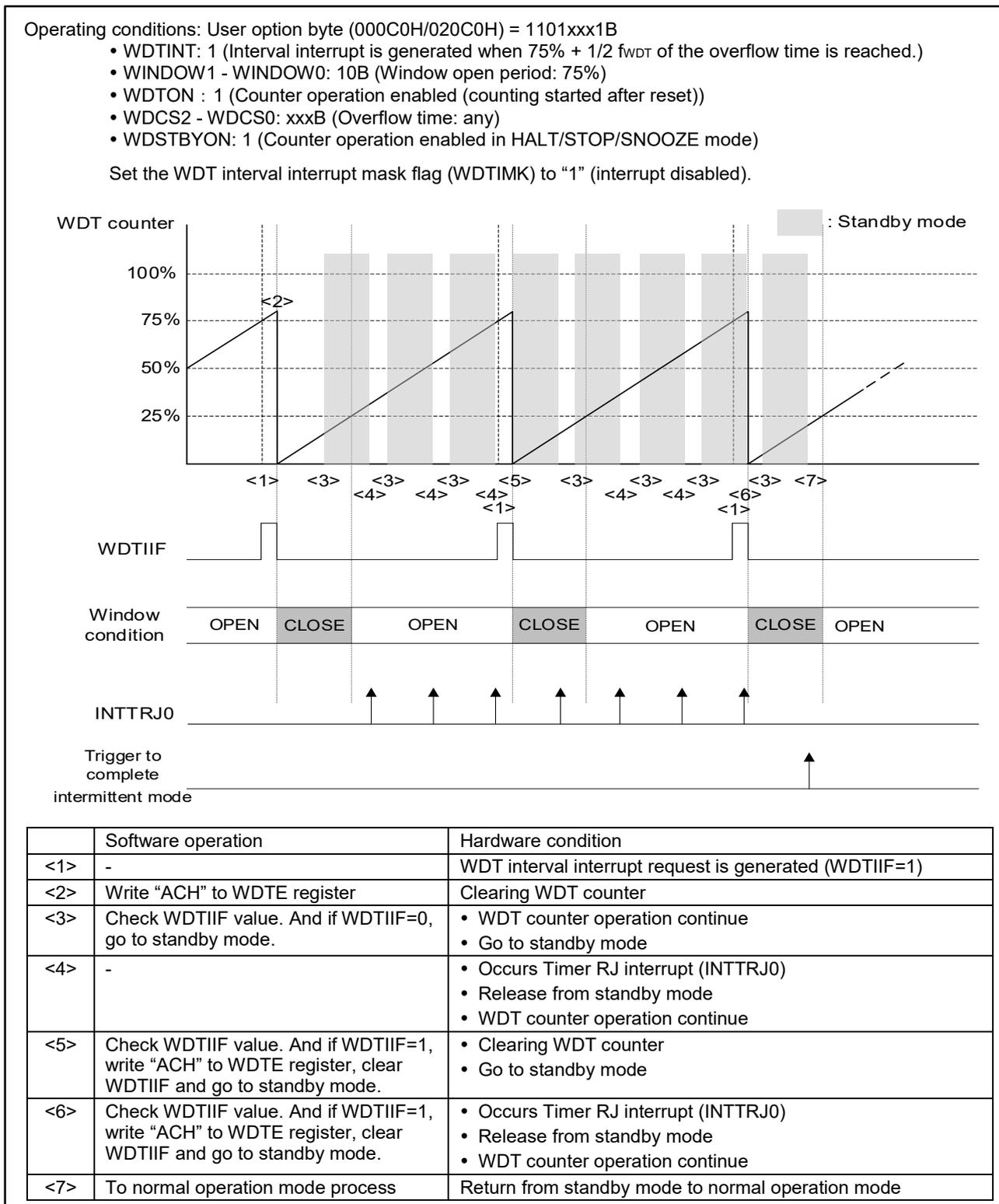


Figure 2-2 Processing Example when Using Timer RJ

### 3. Precaution when Setting the WDT Window Open Period to 75%

Table 3-1 shows the WDT counter clear prohibition period when the window open period is set to 75%. Do not write “ACH” to the WDTE register during the WDT counter clear prohibition period.

**Table 3-1 WDT Counter Clear Prohibition Period**

WDCS2	WDCS1	WDCS0	WDT Overflow Time (In case of $f_{WDT} = 17.25\text{kHz}$ (MAX.))	WDT Counter Clear Prohibition Period <sup>Note</sup>
0	0	0	$2^6/f_{WDT}$ (3.71 ms)	1.85 ms to 2.51 ms
0	0	1	$2^7/f_{WDT}$ (7.42 ms)	3.71 ms to 5.02 ms
0	1	0	$2^8/f_{WDT}$ (14.84 ms)	7.42 ms to 10.04 ms
0	1	1	$2^9/f_{WDT}$ (29.68 ms)	14.84 ms to 20.08 ms
1	0	0	$2^{11}/f_{WDT}$ (118.72 ms)	56.36 ms to 80.32 ms
1	0	1	$2^{13}/f_{WDT}$ (474.89 ms)	237.44 ms to 321.26 ms
1	1	0	$2^{14}/f_{WDT}$ (949.79 ms)	474.89 ms to 642.51 ms
1	1	1	$2^{16}/f_{WDT}$ (3799.18 ms)	1899.59 ms to 2570.04 ms

Note: This is the value when 75% is set for the window open period. And the oscillation accuracy of the WDT operating clock (low-speed on-chip oscillator) is included.

#### 4. References

Documents referenced in this application note are shown below. When referring to these documents, make sure to obtain the latest version of each document from Renesas Electronics website.

- RL78/ F12 User's Manual: Hardware Rev. 1.10
- RL78/ F13, F14 User's Manual: Hardware Rev. 2.10
- RL78/ F15 User's Manual: Hardware Rev. 1.00
- RL78/ D1A User's Manual: Hardware Rev. 1.10

### Revision History

Rev.	Date	Description	
		Page	Summary
1.01	Sep. 30, 2021	-	First edition issued

# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

## 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

## 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

## 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

## 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

## 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

## 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

## 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

## 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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