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April 1st, 2010
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SH7080 Group

SCIF serial data transmission and reception functions in the clock synchronous mode

Introduction

This application note describes the clock synchronous serial data transmission and reception functions that use the transmit-FIFO data-empty interrupt sources and receive-data-full interrupt sources of the SCIF (Serial Communications Interface with FIFO).

This application note is for your reference in the design of user software.

Target Device

SH7085

Contents

1. Specification.....	2
2. Applicable Conditions	2
3. Description of Functions Used	3
4. Principles of Operation.....	6
5. Description of Software.....	8
6. Flowchart.....	14

1. Specification

This sample task uses the clock synchronous serial transfer function with FIFO to transmit and receive 256 bytes of data. Communications are handled as full-duplex by using the loop-back test function of the SCIF, in which the serial transmit pin (TXD3) and the serial receive pin (RXD3) are internally connected. Figure 1 shows the operation in this sample task.

- The communications format has a fixed data length of 8 bits.
- The transmission trigger number is set to 8, and 256 bytes of data are transmitted by using the transmit-FIFO data-empty interrupt source. Executing the transmission-interrupt processing routine once writes 8 bytes of data for transmission to the transmit-FIFO data register (SCFTDR).
- The reception trigger number is set to 8, and 256 bytes of data are received by using the receive data-full interrupt source. A single execution of the reception-interrupt processing routine reads 8 bytes of received data from the receive FIFO data register (SCFRDR).

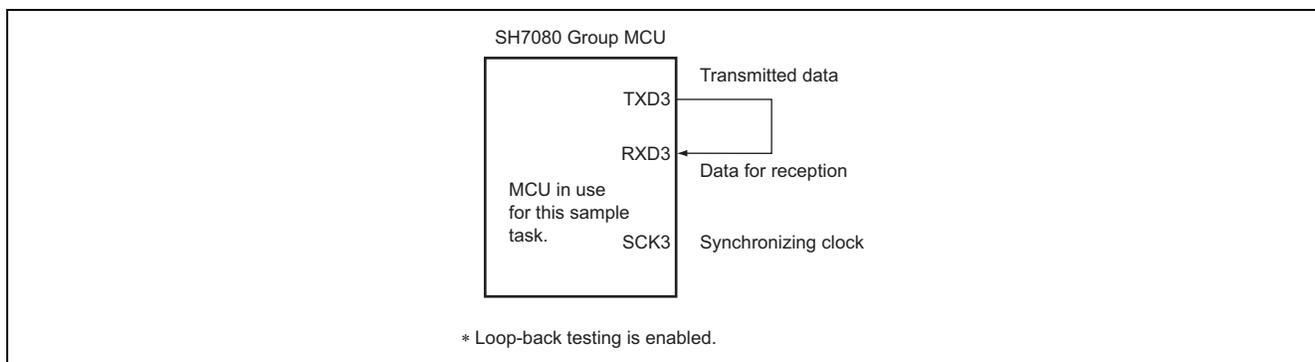


Figure 1 SCIF Serial Data Transmission and Reception in the Clock Synchronous Mode

2. Applicable Conditions

- Microcontroller: SH7085 (R5F7085)
- Operating frequencies: Internal clock 80 MHz
 - : Bus clock 40 MHz
 - : Peripheral clock 40 MHz
 - : MTU2 clock 40 MHz
 - : MTU2S clock 80 MHz
- C compiler : Renesas Technology V.8.00.04

3. Description of Functions Used

This sample application uses the transmit-FIFO data-empty interrupt source of the SCIF (Serial Communications Interface with FIFO) to transmit serial data in the clock synchronous mode. In the SCIF clock synchronous mode, data is transmitted in synchronization with the clock pulse. When the internal clock is selected, the synchronizing clock signal is output through the SCK pin. When the external clock signal is selected, the synchronizing clock signal is input through the SCK pin. A block diagram of the SCIF is given as figure 2.

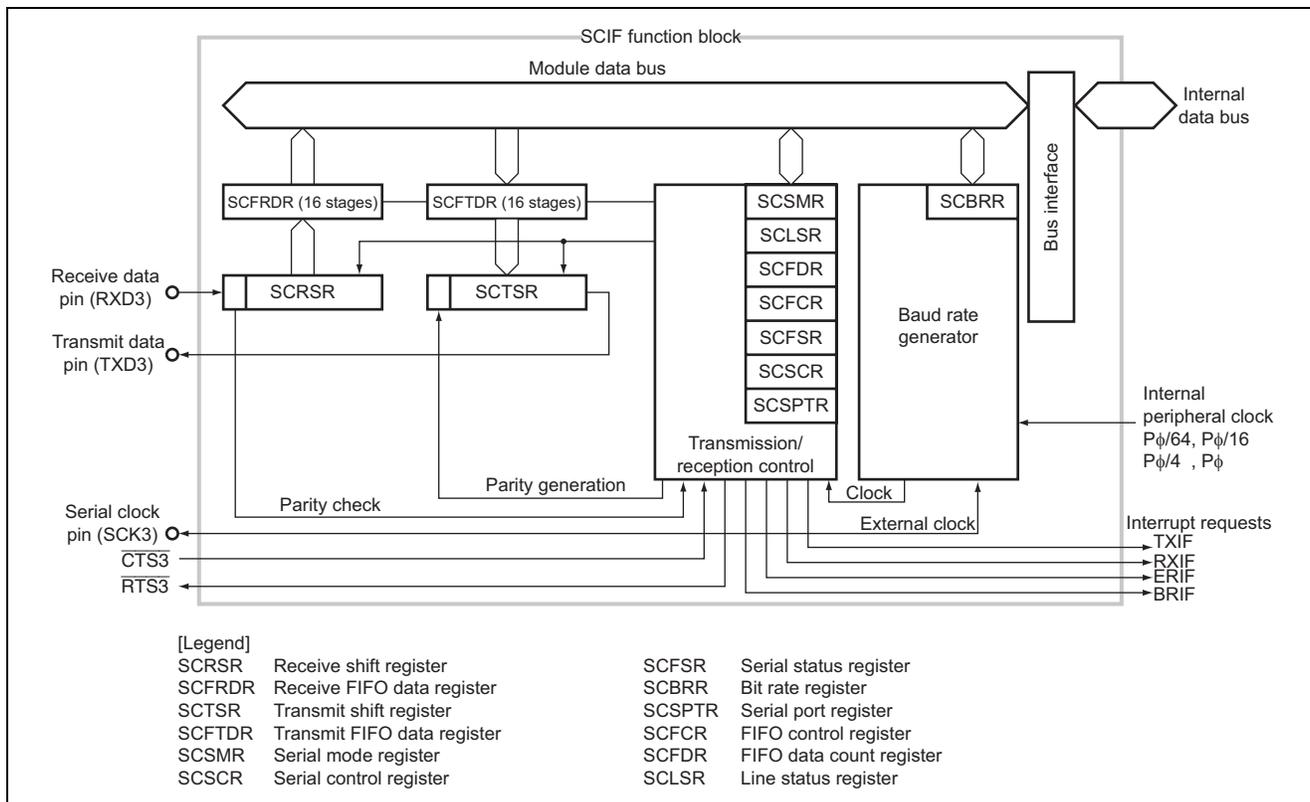


Figure 2 Block Diagram of the SCIF (Serial Communications Interface with FIFO)

- Provision of one 16-stage FIFO register each for transmission and reception enables efficient, high-speed serial communications.
- Serial data transfer proceeds in synchronization with the clock pulses. The SCIF provides a way to communicate with other LSI circuits that have clock synchronous communications functionality.
- The Receive Shift Register (SCRSR) is used to receive serial data. The SCIF places the serial data input from the RDX pin in SCRSR in the order of reception, starting with the LSB (bit 0), and converts the data to parallel data. When 1 byte of data has been received, the data is automatically transferred to the Receive FIFO Data Register (SCFRDR). The CPU cannot directly transfer data to or from SCRSR.
- The Receive FIFO Data Register (SCFRDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold received serial data. After 1 byte of data has been received, the received serial data is transferred from the Receive Shift Register (SCRSR) to SCFRDR for storage, completing reception. Successive reception operations can proceed in this way until 16 bytes of data have been stored in the register. The CPU can read data from SCFRDR, but it cannot write data to SCFRDR. If a read from the Receive FIFO Data Register is attempted when there is no received data in the register, the value read is undefined. After the register has been filled with received data, any subsequently received serial data is lost.
- The Transmit Shift Register (SCTSR) is used to transmit serial data. The SCIF transfers data for transmission from the Transmit FIFO Data Register (SCFTDR) to SCTSR, and then performs serial data transmission by sending the data to the TXD pin in order starting with the LSB (bit 0). When 1 byte of data has been transmitted, the next byte of data for transmission is automatically transferred from SCFTDR to SCTSR to start transmission. The CPU cannot directly transfer data to or from SCTSR.
- The Transmit FIFO Data Register (SCFTDR) is a 16-stage FIFO register (each stage is 8 bits) used to hold the data that is to be transmitted serially. When the SCIF detects that the Transmit Shift Register (SCTSR) is empty, the SCIF starts serial transmission by transferring the data for transmission that has been written in SCFTDR to SCTSR. Serial transmission will proceed until SCFTDR is empty. The CPU can continue to write data to SCFTDR with any timing until SCFTDR becomes full of data for transmission (16 bytes), after which no more data can be written. If an attempt is made to write more data, the data is ignored.
- The Serial Mode Register (SCSMR) is a 16-bit register used to set the SCIF serial communications format and select the clock source for the baud rate generator. The CPU can read data from and write data to SCSMR at any time.
- The Serial Control Register (SCSCR) is a 16-bit register used to enable or disable SCIF transmission, reception, and interrupt requests, and to select the clock source for transmission and reception. The CPU can read data from and write data to SCSCR at any time.
- The Serial Status Register (SCFSR) is a 16-bit register. The upper 8 bits indicate the number of reception errors in the data in the Receive FIFO Data Register, and the lower 8 bits consist of status flags indicating the SCIF operating state. The CPU can read data from and write data to SCFSR at any time. However, 1 cannot be written to the ER, TEND, TDFE, BRK, RDF, and DR status flags. Before these flags can be cleared to 0, they must first be read as 1. The FER and PER flags are read-only flags, and data cannot be written to them.
- The Bit Rate Register (SCBRR) is an 8-bit register that, together with the baud rate generator clock source selection by the CKS1 and CKS0 bits of the Serial Mode Register (SCSMR), sets the bit rate for serial transmission and reception. The CPU can read data from and write data to SCBRR at any time. SCBRR is initialized to H'FF by a power-on reset.
- The FIFO Control Register (SCFCR) is a 16-bit register that resets the number of data and sets the trigger data numbers for the Transmit FIFO Data Register and the Receive FIFO Data Register. The register also contains a loop-back test enable bit. The CPU can read data from and write data to SCFCR at any time.

- The FIFO Data Count Register (SCFDR) is a 16-bit register that indicates the number of data bytes stored in the Transmission FIFO Data Register (SCFTDR) and in the Receive FIFO Data Register (SCFRDR). The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicate the number of receive data bytes in SCFRDR. The CPU can read data from SCFDR at any time.
- The Line Status Register (SCLSR) is a 16-bit register that the CPU can read from and write to at any time. However, 1 cannot be written to the ORER status flag. Before the ORER status flag can be cleared, it must first be read as 1.

4. Principles of Operation

The settings for communications functions in this sample task are described in table 1. The principles of operation for this sample task are illustrated in figure 3.

Table 1 Settings for communications functions in this sample task

Communication format	Function settings
Communication mode	Clock synchronous mode
Interrupts	Transmit-FIFO data-empty interrupt (TXIF) Receive data full interrupt (RXIF) Receive error interrupt (ERIF)
Communication rate	100 Kbps
Data length	8 bits
Bit order	LSB first
Synchronizing clock	Internal clock; SCK pin as synchronizing clock output
FIFO data trigger numbers	Transmission: 8 Reception: 8
Loop-back test function	Enabled (TXD3 and RXD3 pins are internally connected.)

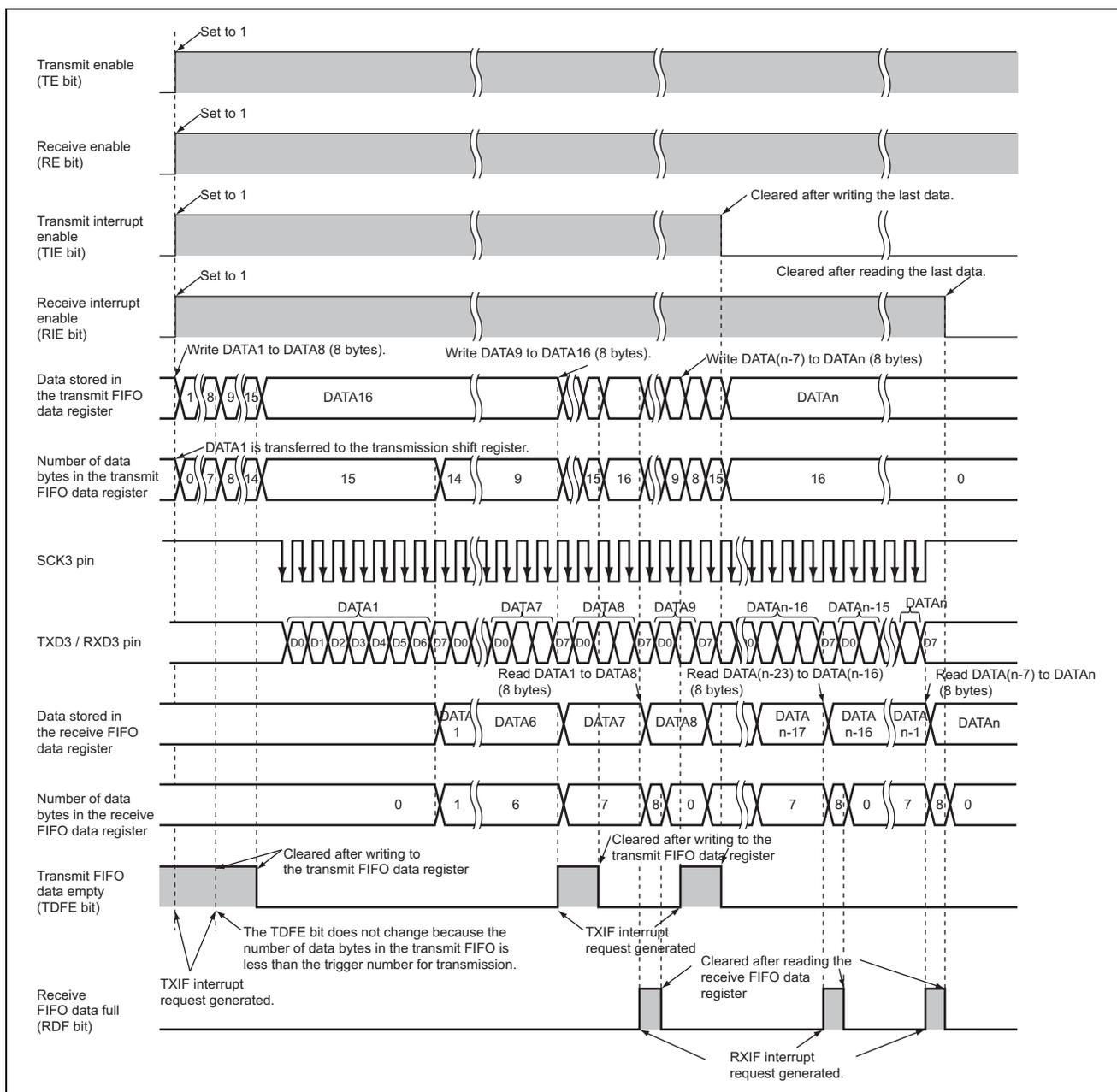


Figure 3 Principles of Operation

5. Description of Software

5.1 Description of Modules Used

The modules of this sample task are described in table 2.

Table 2 Description of Module

Module Name	Label Name	Description
Main routine	main()	Makes initial settings for the SCIF and enables transmission.
SCIF initial settings	io_init_scif()	Processing to make initial settings for transmission/reception by the SCIF in the clock synchronous mode
SCIF transmit-FIFO data-empty interrupt routine	int_scif_txif()	Handles SCIF transmit-FIFO data-empty interrupts.
SCIF receive data-full interrupt routine	int_scif_rxif()	Handles SCIF receive data-full interrupts.
SCIF reception-error interrupt routine	int_scif_erif()	Handles SCIF reception-error interrupts.

5.2 Variables Used

The variables used in this sample task are described in table 3.

Table 3 Variables Used

Variables, Label Name	Description	Used In
unsigned int DataNum	Amount of data to be transmitted/received	int_scif_txif()
unsigned int SndCnt	Transmission counter	main(), int_scif_txif()
unsigned char SndData[256]	Buffer for storage of data for transmission	main(), int_scif_txif()
unsigned int TXIFCnt	Transmit-FIFO data-empty interrupt counter	main(), int_scif_txif()
unsigned int RcvCnt	Reception counter	main(), int_scif_rxif()
unsigned char RcvData[256]	Received-data storage buffer	main(), int_scif_rxif()
unsigned int RXIFCnt	Receive data-full interrupt counter	main(), int_scif_rxif()
unsigned int ERCnt	Reception error interrupt counter	main(), int_scif_erif()

5.3 Setting the Registers

This section describes the setting of registers used in this sample task. Note that the settings shown below are used in the sample task and are not initial values.

5.3.1 Register for Setting the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)

The Frequency Control Register specifies the division ratio of the operating frequency.

Setting: H'0241

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	IFC[2:0]	000	Division ratio of the internal clock (I ϕ) frequency 000: $\times 1$, 80 MHz when the input clock is 10 MHz
11 to 9	BFC[2:0]	001	Division ratio of the bus clock (B ϕ) frequency 001: $\times 1/2$, 40 MHz when the input clock is 10 MHz
8 to 6	PFC[2:0]	001	Division ratio of the peripheral clock (P ϕ) frequency 001: $\times 1/2$, 40 MHz when the input clock is 10 MHz
5 to 3	MIFC[2:0]	000	Division ratio of the MTU2S clock (MI ϕ) frequency 000: $\times 1$, 80 MHz when the input clock is 10 MHz
2 to 0	MPFC[2-0]	001	Division ratio of the MTU2 clock (MP ϕ) frequency 001: $\times 1/2$, 40 MHz when the input clock is 10 MHz

5.3.2 Register for Setting the Low Power Consumption Mode

- Standby Control Register 3 (STBCR3)

This register controls the operation of each module in the low power consumption mode.

Setting: H'BF

Bit	Bit Name	Setting	Function
7	MSTP15	1	1: Stops clock supply to I ² C2 module.
6	MSTP14	0	0: SCIF in operation.
5	MSTP13	1	1: Stops clock supply to SCI_2 module.
4	MSTP12	1	1: Stops clock supply to SCI_1 module.
3	MSTP11	1	1: Stops clock supply to SCI_0 module.
2	MSTP10	1	1: Stops clock supply to the SSU module.
1 to 0	—	11	Reserved

5.3.3 Settings for Serial Communications with FIFO

- Serial Control Register (SCSCR)

This register enables and disables transmission, reception, and interrupt requests, and selects the clock source for transmission and reception.

Setting: H'00F0

Bit	Bit Name	Setting	Function
15 to 8	—	0000 0000	Reserved
7	TIE	1	0: Disables transmit-FIFO data-empty interrupt (TXIF) requests. 1: Enables transmit-FIFO data-empty interrupt (TXIF) requests.
6	RIE	1	0: Disables receive-data-full interrupt (RXIF) requests, reception error interrupt (ERIF) requests, and break interrupt (BRIF) requests. 1: Enables receive-data-full interrupt (RXIF) requests, reception error interrupt (ERIF) requests, and break interrupt (BRIF) requests.
5	TE	1	0: Disables transmission. 1: Enables transmission.
4	RE	1	0: Disables reception. 1: Enables reception.
3	REIE	0	0: Disables reception error interrupt (ERIF) requests and break interrupt (BRIF) requests.
2	—	0	Reserved
1 to 0	CKE[1:0]	00	00: The internal clock; the SCK pin functions as the output for the synchronizing clock signal

- FIFO Control Register

This register resets the data count and sets the trigger data numbers for the Transmit FIFO Data Register and the Receive FIFO Data Register.

Setting: H'0081

Bit	Bit Name	Setting	Function
15 to 11	—	00000	Reserved
10 to 8	RSTRG[2:0]	000	000: $\overline{\text{RTS}}$ output active trigger. Invalid because modem signals are not allowed.
7 to 6	RTRG[1:0]	10	10: Receive FIFO data trigger number = 8
5 to 4	TTRG[1:0]	00	00: Transmit FIFO data trigger number = 8
3	MCE	0	0: Disables modem signals.
2	TFRST	0	0: Disables resetting of the Transmit FIFO Data Register. 1: Enables resetting of the Transmit FIFO Data Register.
1	RFRST	0	0: Disables resetting of the Receive FIFO Data Register. 1: Enables resetting of the Receive FIFO Data Register.
0	LOOP	1	0: Disables loop-back testing. 1: Enables loop-back testing.

- Serial Status Register (SCFSR)

The upper 8 bits of this register indicate the number of errors in reception, and the lower 8 bits indicate the operating state of the SCIF.

Setting: H'0000

Bit	Bit Name	Setting	Function
15 to 12	PER[3:0]	0000	Number of parity errors
11 to 8	FER[3:0]	0000	Number of framing errors
7	ER	0	Reception error
6	TEND	0	0: Transmission is in progress. 1: Transmission has ended.
5	TDFE	0	0: The number of data items for transmission written to SCFTDR is greater than the specified trigger number for transmission. 1: The number of data items for transmission written to SCFTDR is less than the specified trigger number for transmission.
4	BRK	0	0: No break signal
3	FER	0	0: No framing error
2	PER	0	0: No parity error
1	RDF	0	0: Fewer data items have been received in SCFRDR than the specified trigger number for reception.
0	DR	0	0: Reception is in progress, or there is no received data left in SCFRDR after normal reception.

- Serial Mode Register (SCSMR)

This register sets the transfer format and selects the clock source for the baud rate generator.

Setting: H'0080

Bit	Bit Name	Setting	Function
15 to 8	—	0000 0000	Reserved
7	C/A	1	0: Asynchronous mode 1: Clock synchronous mode
6	CHR	0	0: 8-bit data
5	PE	0	0: Disables parity bit addition and checking.
4	O/E	0	0: Ignores the O/E bit specification because PE = 0.
3	STOP	0	0: 1 stop bit
2	—	0	Reserved
1 to 0	CKS[1:0]	00	00: P _φ clock

- Bit Rate Register (SCBRR)

This register sets the bit rate for serial transmission and reception.

Setting: H'0063

Bit	Bit Name	Setting	Function
7 to 0	—	0110 0011	Bit rate for serial transmission/reception

5.3.4 Settings for Pin Function Controller (PFC)

- Port E I/O register L (PEIORL)

This register selects the input directions for the pins of port E.

Setting: H'0060

Bit	Bit Name	Setting	Function
15	PE15IOR	0	0: PE15 input
14	PE14IOR	0	0: PE14 input
13	PE13IOR	0	0: PE13 input
12	PE12IOR	0	0: PE12 input
11	PE11IOR	0	0: PE11 input, RXD3
10	PE10IOR	0	0: PE10 input
9	PE9IOR	0	0: PE9 input
8	PE8IOR	0	0: PE8 input
7	PE7IOR	0	0: PE7 input
6	PE6IOR	1	1: PE6 output, SCK3
5	PE5IOR	1	1: PE5 output, TXD3
4	PE4IOR	0	0: PE4 input
3	PE3IOR	0	0: PE3 input
2	PE2IOR	0	0: PE2 input
1	PE1IOR	0	0: PE1 input
0	PE0IOR	0	0: PE0 input

- Port E Control Register L3 (PECRL3)

This register selects the functions of port E pins with multiplexed functions.

Setting: H'3000

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	PE11MD[2:0]	011	011: RXD3 input (SCIF)
11	—	0	Reserved
10 to 8	PE10MD[2:0]	000	000: PE10 input/output (port)
7	—	0	Reserved
6 to 4	PE9MD[2:0]	000	000: PE9 input/output (port)
3	—	0	Reserved
2 to 0	PE8MD[2:0]	000	000: PE8 input/output (port)

- Port E Control Register L2 (PECRL2)

This register selects the functions of port E pins with multiplexed functions.

Setting: H'0220

Bit	Bit Name	Setting	Function
15	—	0	Reserved
14 to 12	PE7MD[2:0]	000	011: PE7 input/output (port)
11	—	0	Reserved
10 to 8	PE6MD[2:0]	010	000: SCK3 input/output (port)
7	—	0	Reserved
6 to 4	PE5MD[2:0]	010	010: TXD3 output (port)
3	—	0	Reserved
2 to 0	PE4MD[2:0]	000	000: PE4 input/output (port)

5.3.5 Settings for interrupt controller (INTC)

- Interrupt priority register L (IPRL)

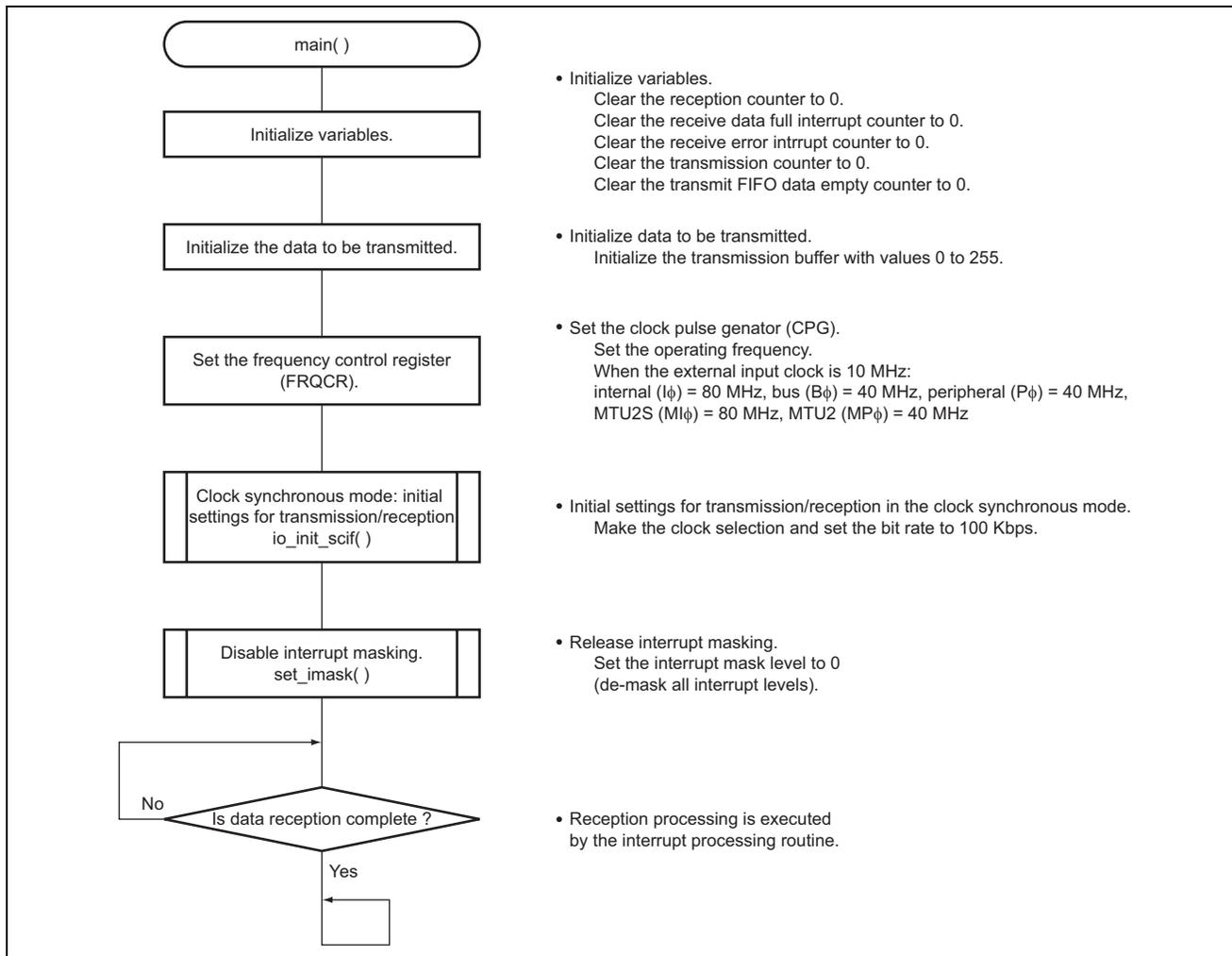
This register determines the priority levels of the corresponding interrupt requests.

Setting: H'000F

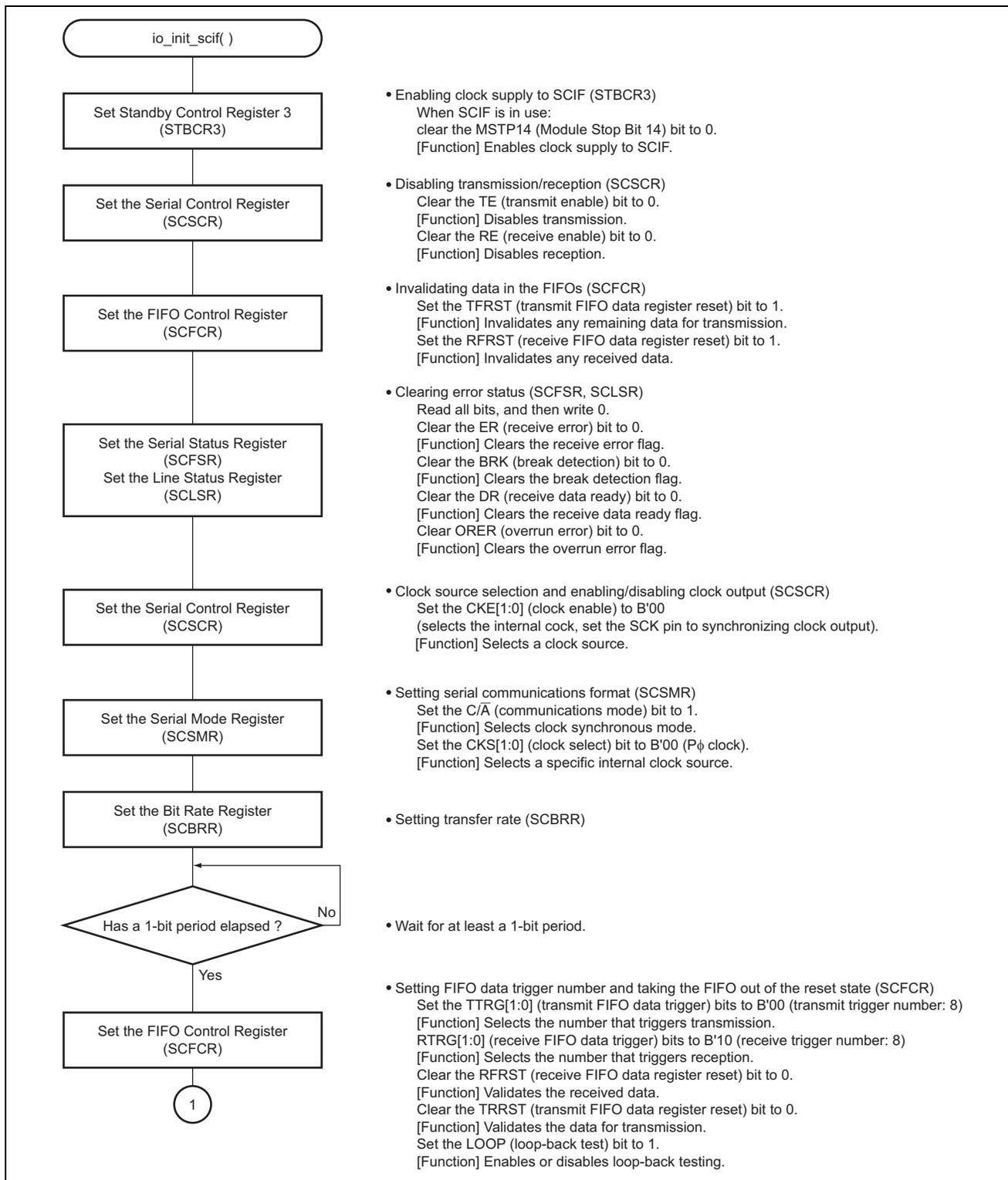
Bit	Bit Name	Setting	Function
15 to 12	IPR[15:12]	0000	Priority level 0
11 to 8	IPR[11:8]	0000	Priority level 0
7 to 4	IPR[7:4]	0000	Priority level 0
3 to 0	IPR[3:0]	1111	Priority level 15, SCIF interrupts

6. Flowchart

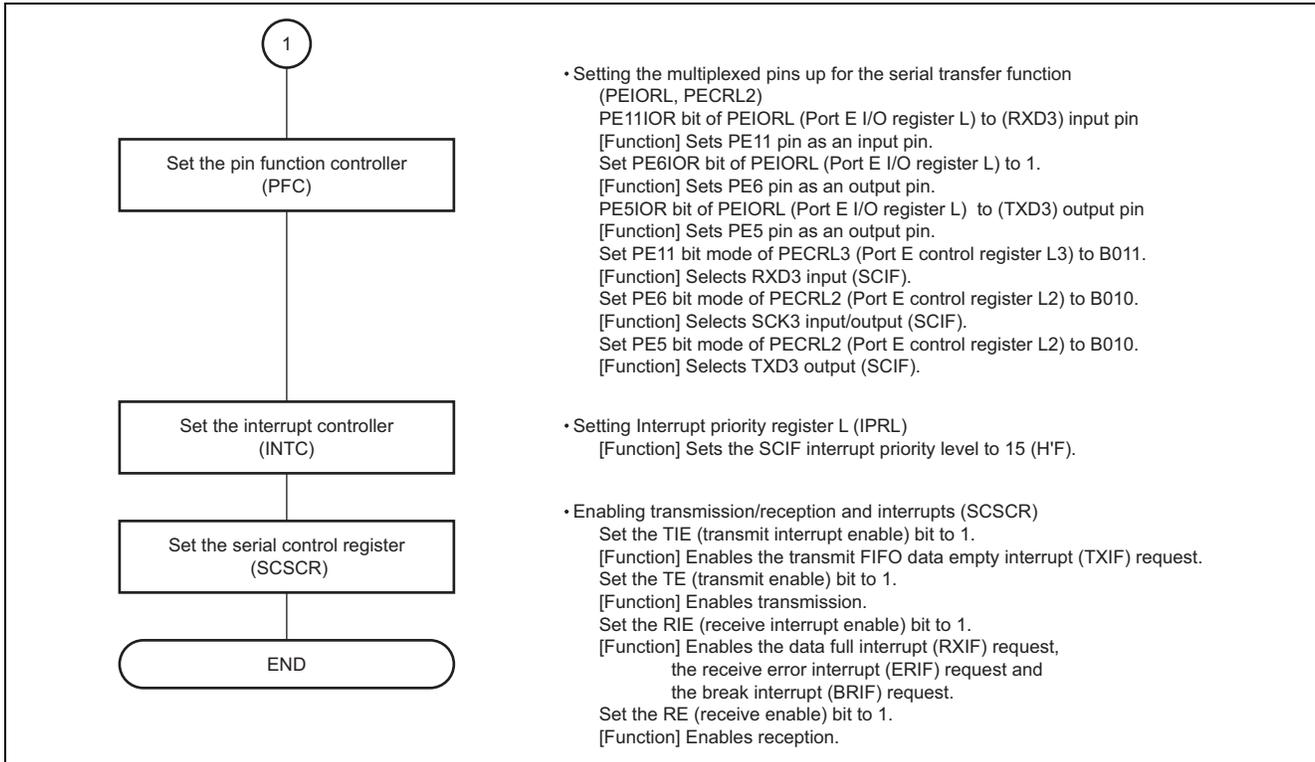
6.1 Main routine



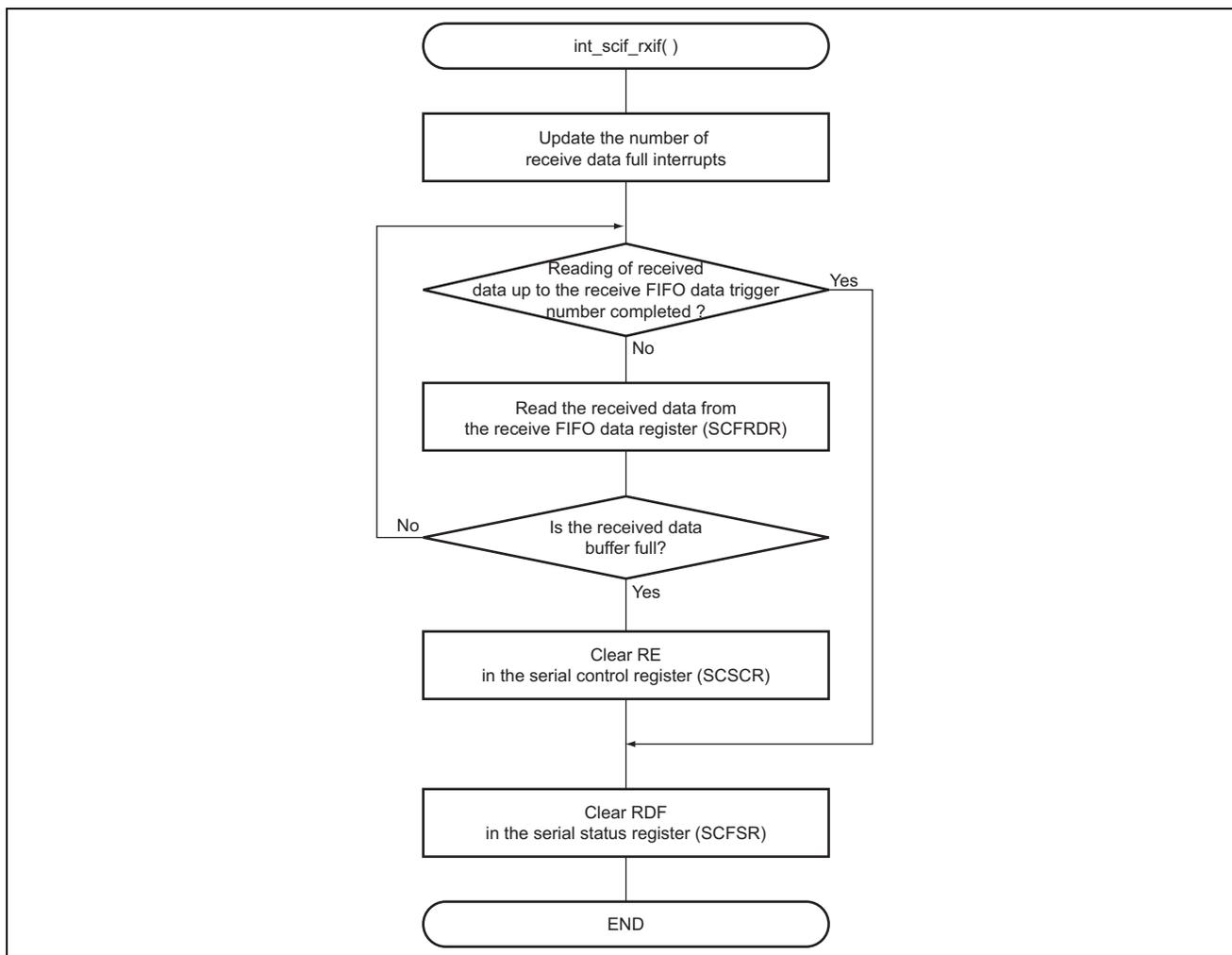
6.2 SCIF transmission/reception initial setting routine in the clock synchronous mode



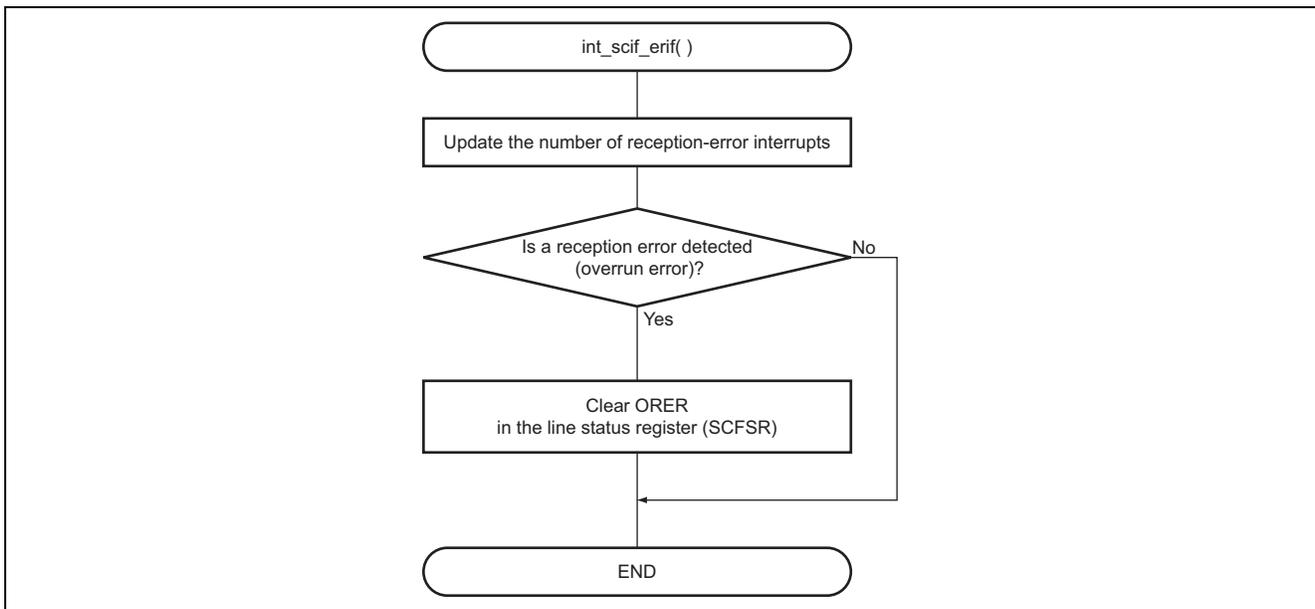
- Enabling clock supply to SCIF (STBCR3)
When SCIF is in use:
clear the MSTP14 (Module Stop Bit 14) bit to 0.
[Function] Enables clock supply to SCIF.
- Disabling transmission/reception (SCSCR)
Clear the TE (transmit enable) bit to 0.
[Function] Disables transmission.
Clear the RE (receive enable) bit to 0.
[Function] Disables reception.
- Invalidating data in the FIFOs (SCFCR)
Set the TFRST (transmit FIFO data register reset) bit to 1.
[Function] Invalidates any remaining data for transmission.
Set the RFRST (receive FIFO data register reset) bit to 1.
[Function] Invalidates any received data.
- Clearing error status (SCFSR, SCLSR)
Read all bits, and then write 0.
Clear the ER (receive error) bit to 0.
[Function] Clears the receive error flag.
Clear the BRK (break detection) bit to 0.
[Function] Clears the break detection flag.
Clear the DR (receive data ready) bit to 0.
[Function] Clears the receive data ready flag.
Clear ORER (overrun error) bit to 0.
[Function] Clears the overrun error flag.
- Clock source selection and enabling/disabling clock output (SCSCR)
Set the CKE[1:0] (clock enable) to B'00
(selects the internal clock, set the SCK pin to synchronizing clock output).
[Function] Selects a clock source.
- Setting serial communications format (SCSMR)
Set the C/A (communications mode) bit to 1.
[Function] Selects clock synchronous mode.
Set the CKS[1:0] (clock select) bit to B'00 (P_φ clock).
[Function] Selects a specific internal clock source.
- Setting transfer rate (SCBRR)
- Wait for at least a 1-bit period.
- Setting FIFO data trigger number and taking the FIFO out of the reset state (SCFCR)
Set the TTRG[1:0] (transmit FIFO data trigger) bits to B'00 (transmit trigger number: 8)
[Function] Selects the number that triggers transmission.
RTRG[1:0] (receive FIFO data trigger) bits to B'10 (receive trigger number: 8)
[Function] Selects the number that triggers reception.
Clear the RFRST (receive FIFO data register reset) bit to 0.
[Function] Validates the received data.
Clear the TRRST (transmit FIFO data register reset) bit to 0.
[Function] Validates the data for transmission.
Set the LOOP (loop-back test) bit to 1.
[Function] Enables or disables loop-back testing.



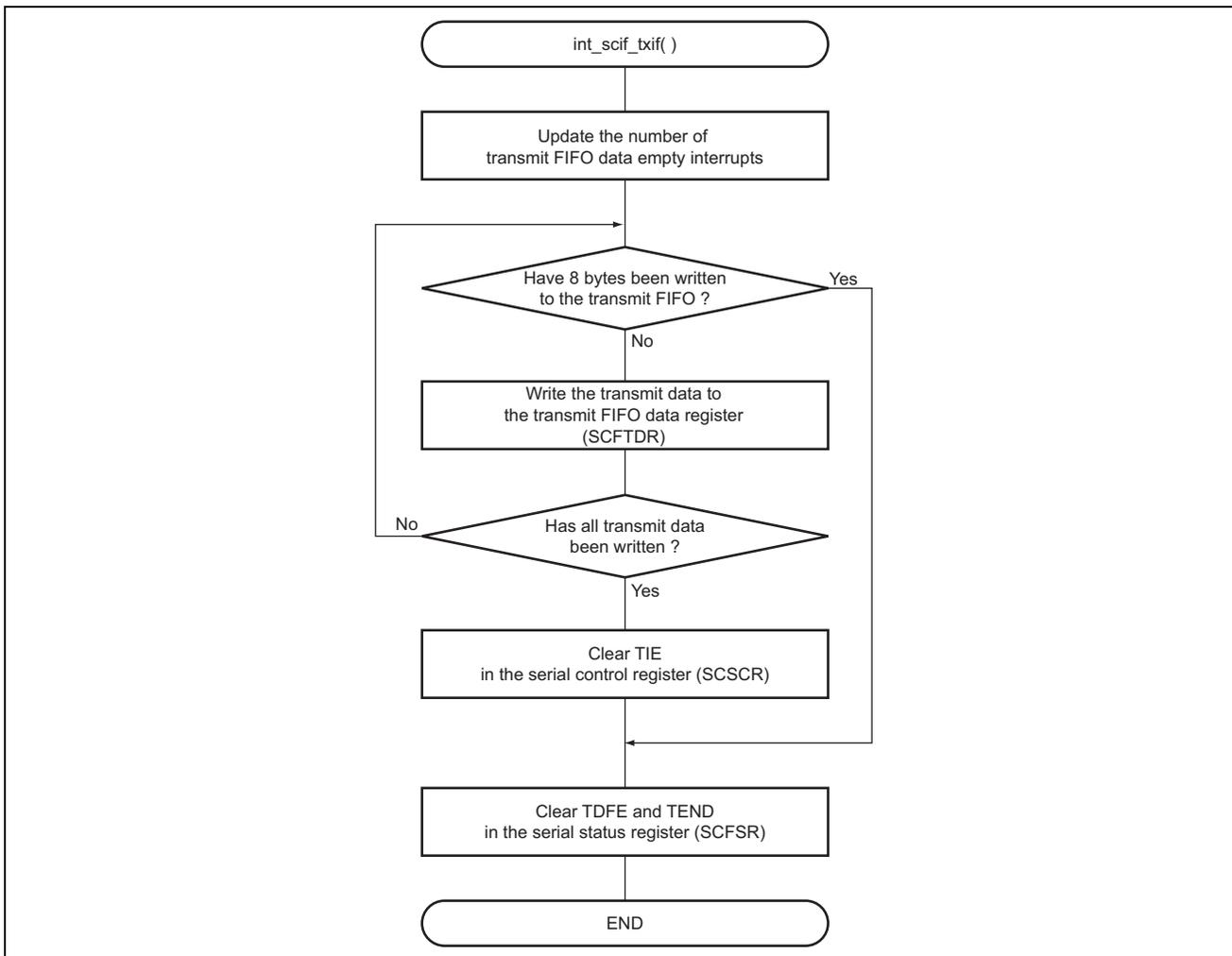
6.3 SCIF receive-data-full interrupt routine



6.4 SCIF reception error interrupt routine



6.5 SCIF transmit-FIFO data-empty interrupt routine



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