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SH7145 Group

Interrupt Level Setting and Modification by Interrupt Controller

Introduction

Interrupts of different levels are generated by specifying interrupt levels via the interrupt controller (INTC) of the SH7145F.

Target Device

SH7145F

Contents

1. Specifications

Interrupts of different levels are generated by specifying interrupt levels via the interrupt controller (INTC) of the SH7145F.

In this sample task, two LEDs are lit alternately by generating a compare-match interrupt at regular intervals using the compare-match timer. In addition, while the IRQ0 input switch is closed, the flickering of LDEs is stopped by an external interrupt (IRQ0).

Figure 1 shows the connections between the LEDs and the $\overline{\text{IRQ0}}$ input switch.

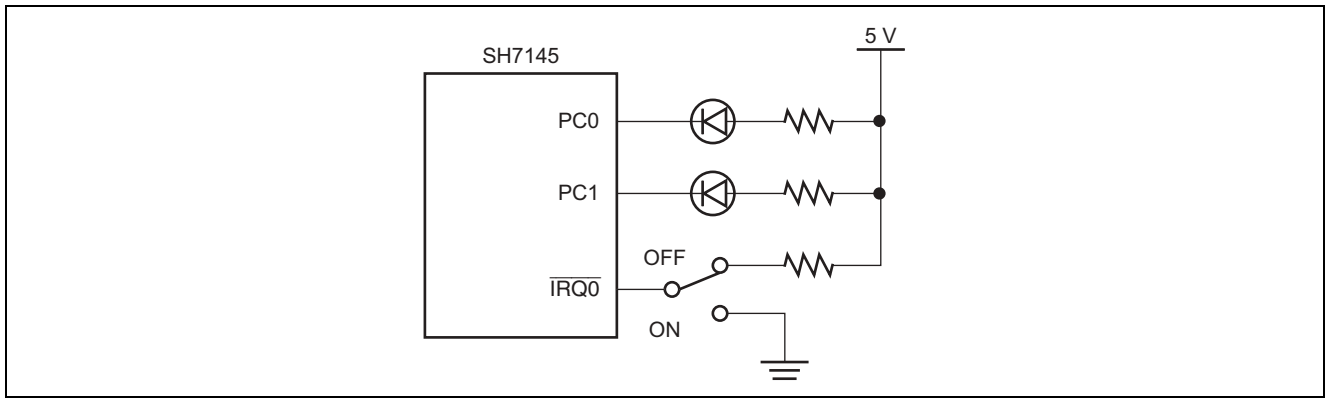


Figure 1 Connection between the LEDs and the $\overline{\text{IRQ0}}$ Input Switch

2. Description of Functions

In this sample task, the interrupt levels of the external interrupt (IRQ0) and compare-match timer interrupt (CMT0) are specified by the interrupt controller (INTC).

2.1 Interrupt Controller (INTC)

Figure 2 shows the block diagram of the interrupt controller. The function of the interrupt controller (INTC) is described below.

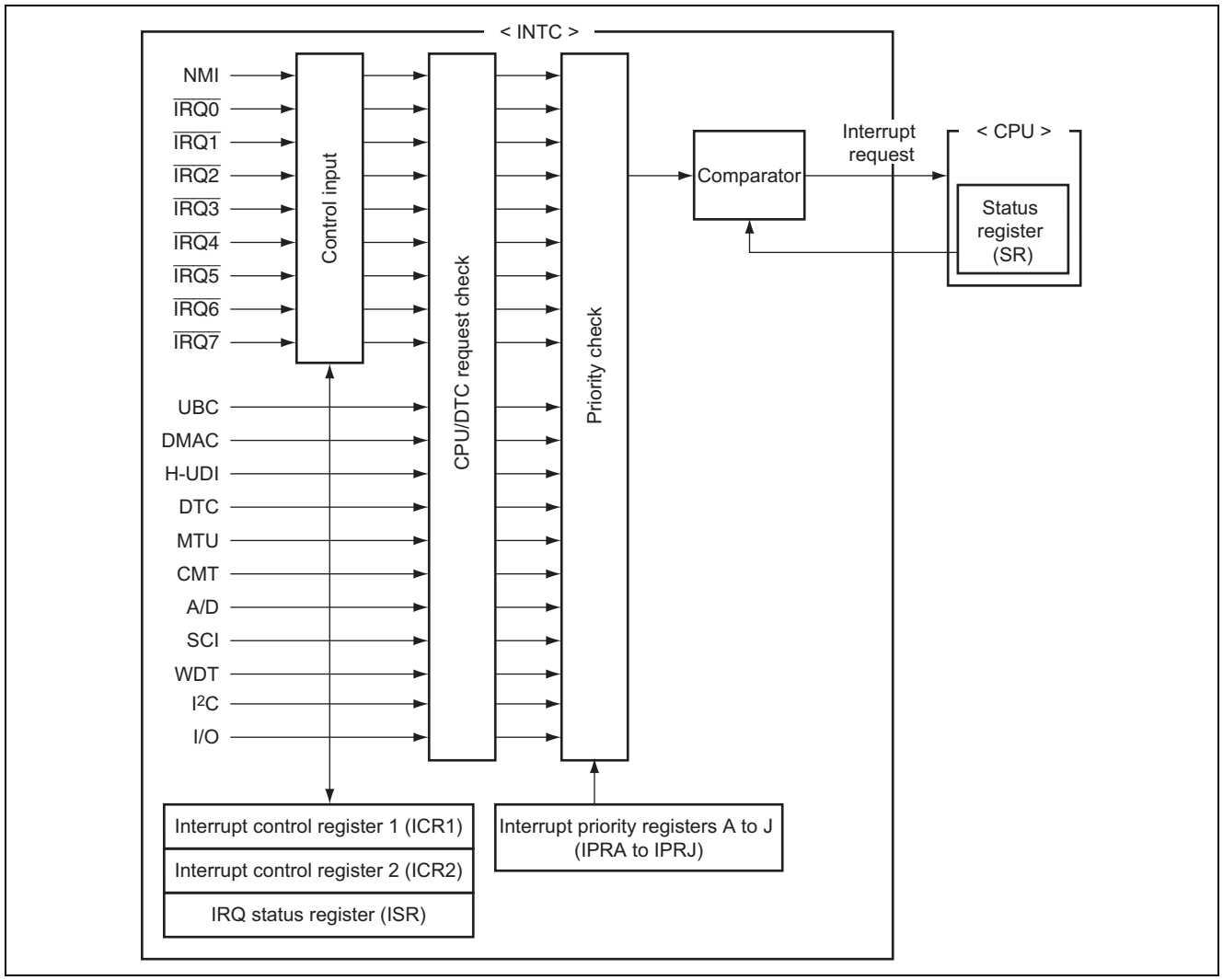


Figure 2 Block Diagram of the Interrupt Controller (INTC)

- The interrupt controller (INTC) sets and checks the interrupt levels, and also controls the interrupt requests to the CPU.
- The interrupt control register 1 (ICR1) specifies the input signal detection mode of the external interrupt input pins (NMI and $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$) and indicates the input signal level on the NMI pin.
- The interrupt control register 2 (ICR2) specifies the $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$ edge detection mode.
- The IRQ status register (ISR) indicates the $\overline{\text{IRQ0}}$ to $\overline{\text{IRQ7}}$ interrupt request statuses.
- The interrupt priority registers A to J (IPRA to IPRJ) specify the levels of interrupts other than NMI.

2.2 Compare-Match Timer (CMT0)

The CMT module channel 0 (ch0) generates an interrupt at specified intervals.

Figure 3 shows a block diagram of the CMT module channel 0 (ch0). Its functions are described below.

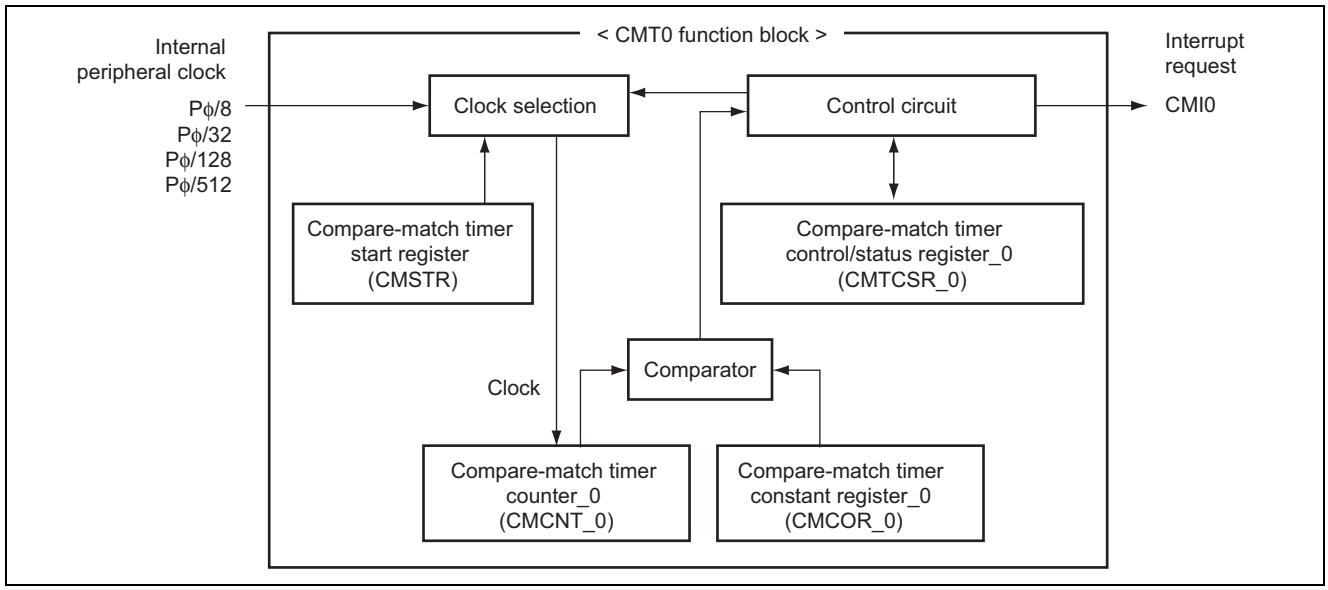


Figure 3 CMT (Channel 0) Block Diagram

- The CMT incorporates a 16-bit counter and can generate interrupts at specified intervals.
- A clock generated by dividing the internal peripheral clock Pϕ can be selected as the input clock. The CMT increments on the selected clock.
- The compare-match timer start register (CMSTR) starts or stops the counting.
- The compare-match timer control/status register (CMCSR_0) indicates a compare-match occurrence, sets up the interrupts, and selects the clock for counting.
- The compare-match timer counter (CMCNT_0) is an up-counter for the generation of an interrupt request on a compare-match between the CMCNT_0 and CMCOR_0 registers.
- The compare-match timer constant register (CMCOR_0) sets the period of compare-match.

3. Principles of Operation

In this sample task, the interrupt controller is configured to detect an interrupt when a low level is input to the $\overline{\text{IRQ0}}$ pin. When a low level is input to $\overline{\text{IRQ0}}$, an external interrupt is requested continuously and a compare-match interrupt cannot be accepted according to the interrupt level settings.

Figure 4 shows the timing of the compare-match interrupt generation by CMT and the external $\overline{\text{IRQ0}}$ interrupt. Table 1 shows the software and hardware processing for the operation shown in figure 4.

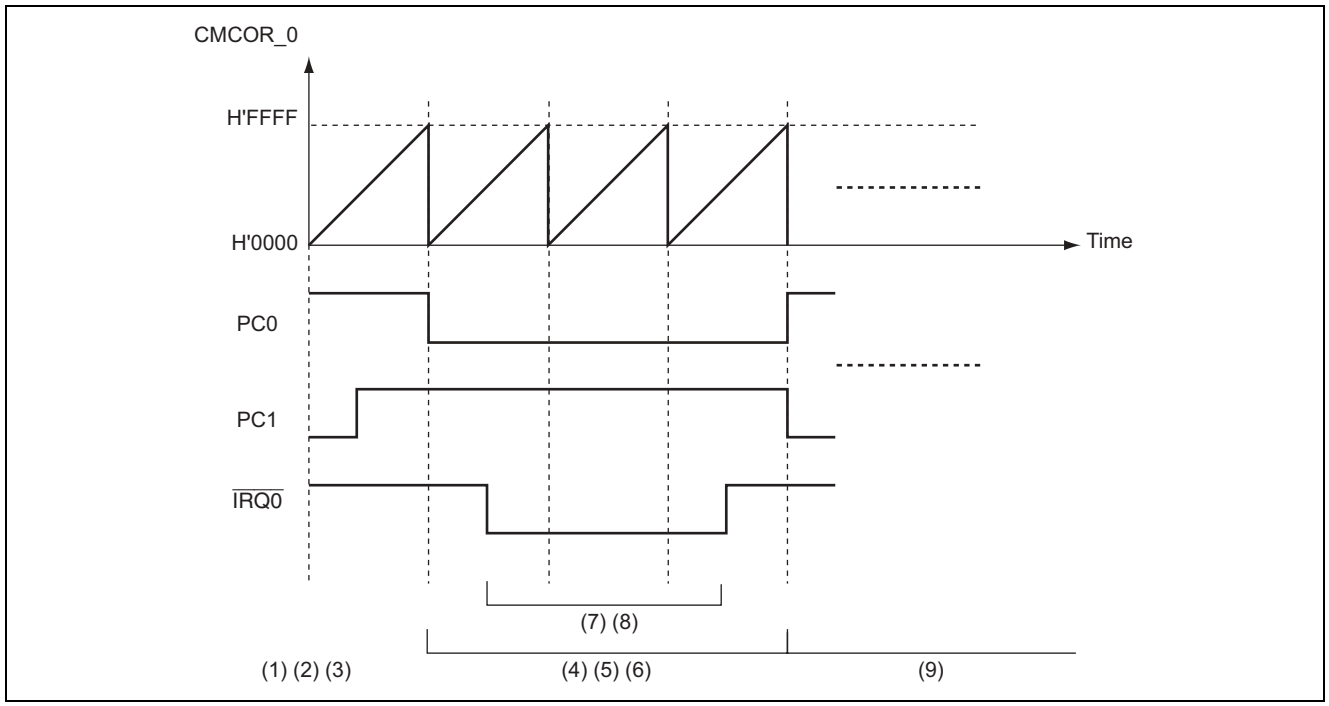


Figure 4 Interrupt Generation Timing

Table 1 Software and Hardware Processing

No.	Software Processing	Hardware Processing
(1)	Set the PC0 and PC1 output levels in PCDR.	—
(2)	Set the interrupt cycle in CMCOR_0.	—
(3)	Set the STR0 bit in CMSTR to 1.	Start counting by CMT0.
(4)	—	Set the CMF flag (a compare-match interrupt is generated).
(5)	Clear the CMF flag to 0.	Start counting by CMT0.
(6)	Invert the PC0 and PC1 output levels by PCDR.	—
(7)	—	Detect the IRQ0 interrupt request.
(8)	—	Mask the compare-match interrupt request while the IRQ0 interrupt request is detected.
(9)	Repeat steps (1) to (8) above.	Repeat steps (1) to (8) above.

4. Description of Software

4.1 Modules

Table 2 shows the modules used in this sample task.

Table 2 Description of Modules

Module Name	Label Name	Function
Main routine	main	Sets up CMT0, sets interrupt levels, and selects the pin functions.
$\overline{\text{IRQ0}}$ interrupt routine	irq_int	Performs no operation.
CMT0 interrupt routine	cmt_int	Inverts the signal levels output from the PC0 and PC1 pins.

4.2 Internal Registers

Tables 3 and 4 describe the internal registers used in this sample task. Note that the settings in these tables indicate the values set in this sample task and not the initial values.

Table 3 Description of Internal Registers (1)

Register Name	Bit	Bit Name	Setting Value	Function
IPRA			H'F000	Interrupt priority register A
	15 to 12	IPR15	1	Specify the IRQ0 interrupt request priority.
		IPR14	1	
		IPR13	1	
		IPR12	1	
IPRG			H'00A0	Interrupt priority register G
	7 to 4	IPR7	1	Specify the IRQ0 interrupt request priority.
		IPR6	0	
		IPR5	1	
		IPR4	0	
ICR1			H'00	Interrupt control register 1
	7	IRQ0S	0	IRQ0 sense select When IRQ0S = 0, an interrupt request is detected if a low level is input to the $\overline{\text{IRQ0}}$ pin.
MSTCR2				Module standby control register 2
	12	MSTP12	0	CMT standby control bit When MSTP12 = 0, the standby state of CMT is cancelled.
CMSTR			H'01	Compare-match timer start register
	15 to 2	—	0	Reserved bits
	1	STR1	0	Count start 1 When STR1 = 0, the CMCNT_1 stops counting.
	0	STR0	1	Count start 0 When STR0 = 1, the CMCNT_0 starts counting.
CMCNT_0			—	Compare-match timer counter_0 Up-counter used to generate an interrupt request.
CMCOR_0			H'FFFF	Compare-match timer constant register Used to set the period of compare-match with CMCNT_0.

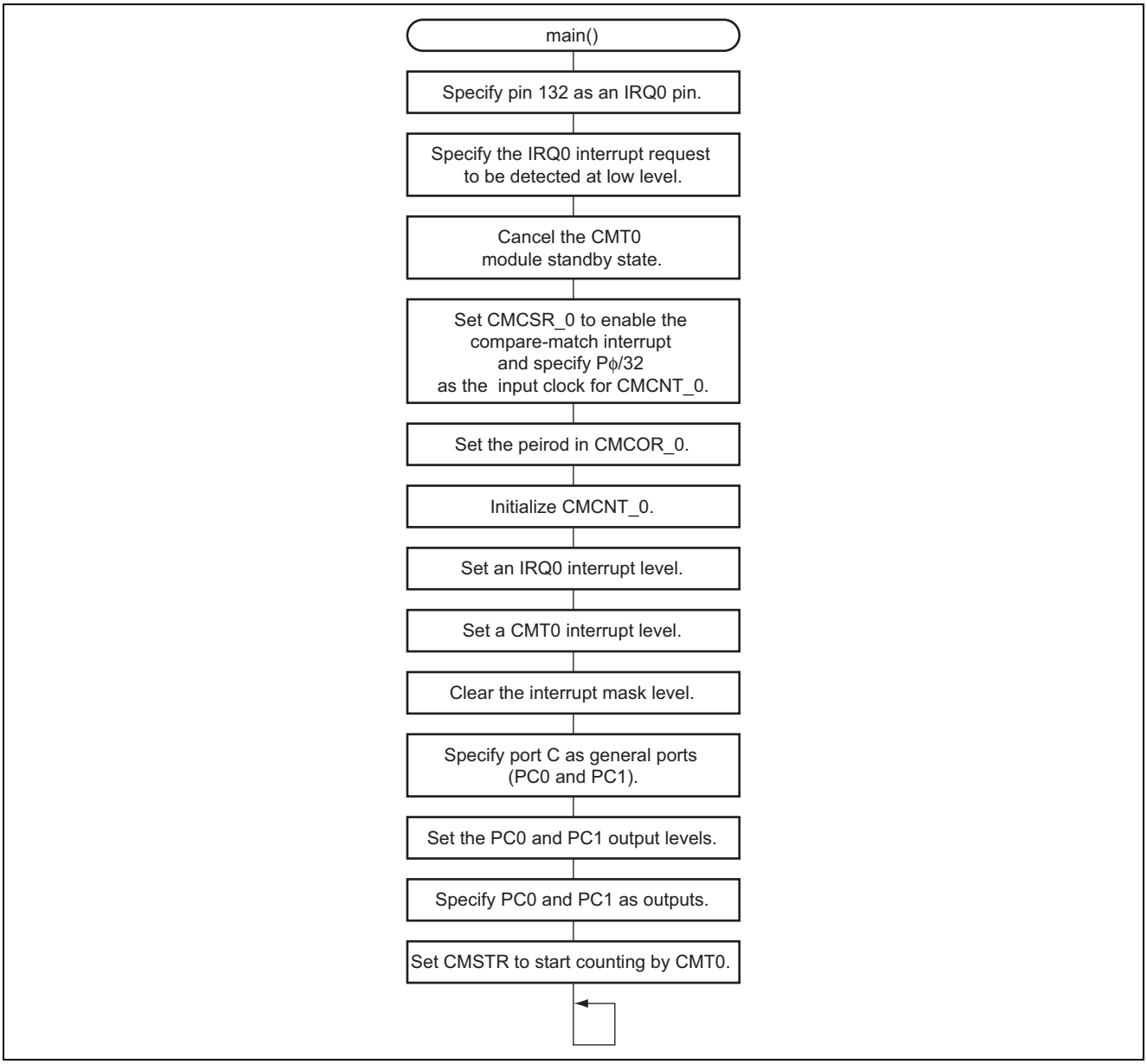
Table 4 Description of Internal Registers (2)

Register Name	Bit	Bit Name	Setting Value	Function
CMCSR_0				Compare-match timer control/status register_0
	15 to 8	—	0	Reserved bits
	7	CMF	*1	Compare-match flag When CMF = 1, the CMCNT matches the CMCOR.
	6	CMIE	1	Compare-match interrupt enable Enables or disables the compare-match interrupt. When CMIE = 1, the compare-match interrupt is enabled.
	5 to 2	—	0	Reserved bits
	1, 0	CKS1 CKS0	0 1	CMCNT_0 input clock selection In this sample task, ϕP/32 is selected.
PCIOR			H'03	Port C I/O register Specifies input/output of the port C pins.
	1	PC1IOR	1	When PC1IOR = 1, PC1 functions as an output pin.
	0	PC0IOR	1	When PC0IOR = 1, PC0 functions as an output pin.
PCDR				Port C data register
	1	PC1DR	*2	When PC1 functions as a general output pin, the value of PC1DR is output.
	0	PC0DR	*2	When PC0 functions as a general output pin, the value of PC0DR is output.

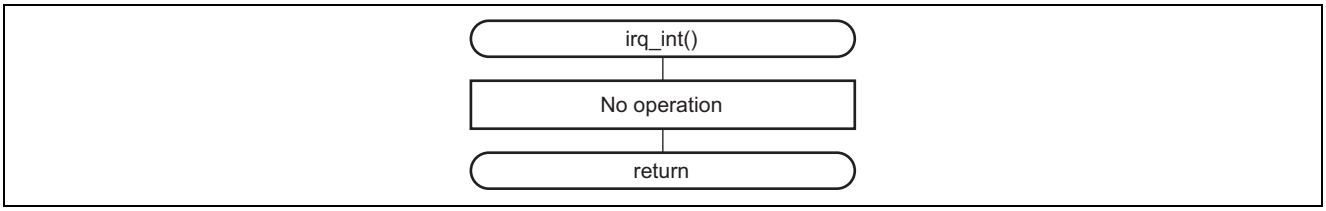
Notes: 1. Only "0" can be written to this bit. This bit is automatically set to 1 by hardware.
2. The value is changed by software every time a compare-match interrupt occurs.

5. Flowchart

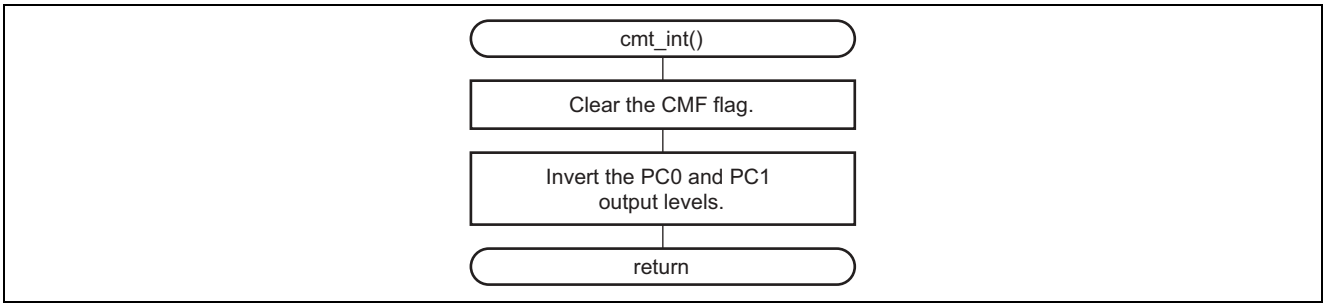
5.1 Main Routine



5.2 $\overline{\text{IRQ0}}$ Interrupt Routine



5.3 Compare-Match Interrupt Routine



6. Program Listing

```
/***********************************************************************************************/
/* SH7145F Application Note                                                                    */
/*                                                                                             */
/* Function                                                                                    */
/*    :INTC(IRQ0,CMT0)                                                                         */
/*                                                                                             */
/* External input clock         :12.5MHz                                                       */
/* Internal CPU clock           :50MHz                                                         */
/* Internal peripheral clock    :25MHz                                                         */
/*                                                                                             */
/* Written        :2003/10      Rev.1.0                                                        */
/***********************************************************************************************/

#include "iodefine.h"
#include <machine.h>

/***********************************************************************************************/
/*  Function Define                                                                            */
/***********************************************************************************************/
void main(void);

void irq_int(void);
void cmt_int(void);
void dummy_f(void);

/***********************************************************************************************/
/*  Main Program                                                                               */
/***********************************************************************************************/
void main(void)
{
    P_PORTA.PACRL2.BIT.PA2MD = 3;                   /* Set pin function (IRQ0: 132pin)          */
    P_INTC.ICR1.BIT.IRQ0S = 0;                      /* Set IRQ0 interrupt mode                  */

    P_STBY.MSTCR2.BIT.MSTP12 = 0;                   /* Disable CMT0 standby mode                */

    P_CMT.CMCSR_0.WORD = 0x0041;                    /* Initialize CMCSR_0                       */
            // [15-8]  = 0
            // [7]CMF  = 0
            // [6]CMIE = 1     : CMT0 interrupt enable
            // [5-2]   = 0
            // [1]CKS1 = 0
            // [0]CKS0 = 1     : Count clock P phi/32
    P_CMT.CMCOR_0 = 0xFFFF;                         /* Set CMCOR_0                              */
    P_CMT.CMCNT_0 = 0;                              /* Initialize CMCNT_0                       */

    P_INTC.IPRA.BIT.IRQ0 = 0xF;                     /* Interruption level of IRQ0               */
    P_INTC.IPRG.BIT.CMT0 = 0xA;                     /* Interruption level of CMT0               */
    set_imask(0);
```

```
    P_PORTC.PCCR.WORD &= 0xFFFC;                    /* Set function PC0,PC1                    */
    P_PORTC.PCDR.BIT.PC0DR = 0;                     /* PC0 -> H                                */
    P_PORTC.PCIOR.WORD |= 0x0003;                   /* PortC output                            */

    P_CMT.CMSTR.BIT.STR = 1;                        /* Count start                             */

    while(1);                                       /* LOOP                                    */
}

/****************************************************************************************************/
/*  Interruption Program                                                                            */
/****************************************************************************************************/
/****************************************************************************************************/
/*  IRQ0 Interruption Program                                                                       */
/****************************************************************************************************/
#pragma interrupt(irq_int)
void irq_int(void)
{
                                                    /* No operation                            */
}

/****************************************************************************************************/
/*  CMT0 Interruption Program                                                                       */
/****************************************************************************************************/
#pragma interrupt(cmt_int)
void cmt_int(void)
{
    P_CMT.CMCSR_0.BIT.CMF = 0;                      /* CMF clear                               */

    P_PORTC.PCDR.WORD = ~P_PORTC.PCDR.WORD;         /* Output reversal                         */
}

/****************************************************************************************************/
/*  Other Interruption Program                                                                      */
/****************************************************************************************************/
#pragma interrupt(dummy_f)
void dummy_f(void)
{
    /* Other Interrupt */
}
```

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Sep.16.04	—	First edition issued

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