
SH7268/SH7269 Group

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Feb. 03, 2012

I²C Bus Interface 3

Master Transmission and Reception

Using Clocked Synchronous Serial Format

Abstract

This application note gives information for using the clocked synchronous serial format included in the I²C bus interface 3 (hereinafter called IIC3) in the SH7269.

Products

SH7268/SH7269 Group (hereinafter called as "SH7269")

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

Contents

1. Specifications	3
2. Operation Confirmation Conditions	4
3. Reference Application Note	4
4. Hardware	5
4.1 Hardware Configuration	5
4.2 Used Pins and the Pin Functions	5
5. Software	6
5.1 Operation Overview	6
5.2 File Composition	7
5.3 Constants	8
5.4 Variables	8
5.5 Functions	8
5.6 Function Specifications	9
5.7 Flowchart	11
5.7.1 Main Processing	11
5.7.2 IIC3 Initialization	12
5.7.3 Data Reception Processing	13
5.7.4 Data Transmission Processing	14
6. Sample Code	15
7. Reference Documents	15

1. Specifications

Set the SH7269 to the master device for the clocked synchronous serial communications to transmit/receive data. The IIC3 clock synchronous serial format function is used for the serial communication. The clock signal (SCK) outputs the possible maximum frequency, 757.5kHz (when P0 is 33.33MHz). Interrupts are unavailable. The IIC3 has only one data signal (at the SDA pin), therefore data are transferred in half-duplex communications.

Table 1.1 shows the peripheral function and its application. Figure 1.1 shows the outline of the operation.

Table 1.1 Peripheral Functions and Their Applications

Peripheral Function	Application
I ² C bus interface 3	Clock synchronous serial communication (in the master device)

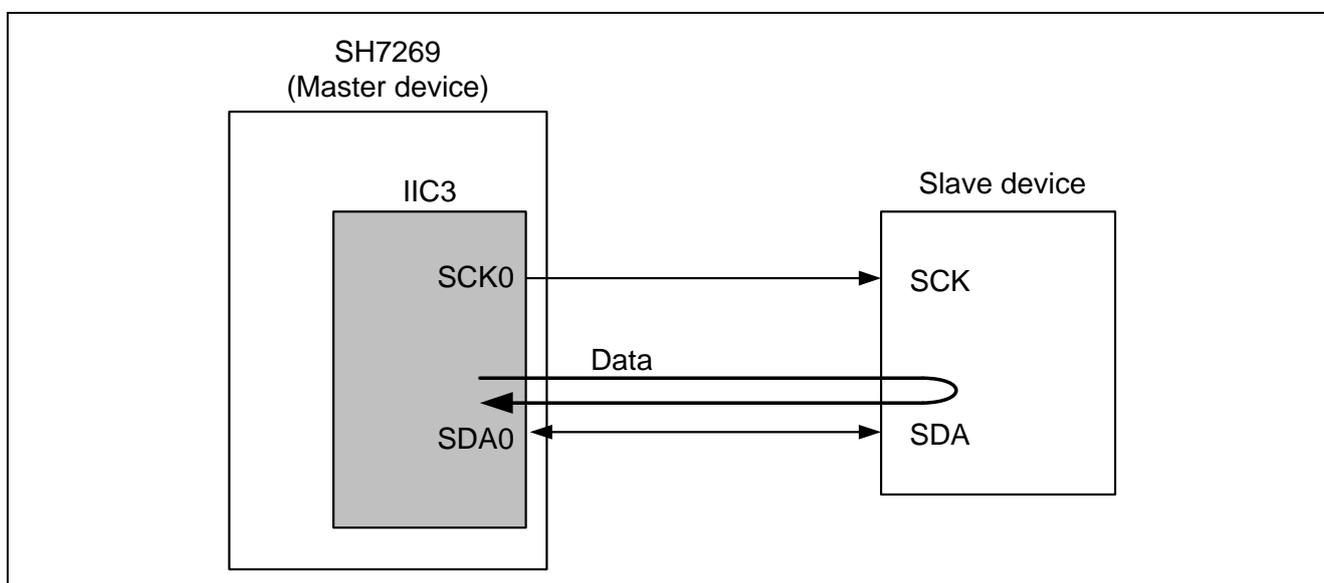


Figure 1.1 Operation Outline

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	SH7269
Operating frequency	<ul style="list-style-type: none"> • CPU internal clock (Iϕ): 266.67MHz • Internal clock (Bϕ): 133.33MHz • Peripheral clock 1 (P1ϕ): 66.67MHz • Peripheral clock 0 (P0ϕ): 33.33MHz • SCK clock: 757.5kHz
Operating voltage	<ul style="list-style-type: none"> • PVcc: 3.3V • Vcc: 1.25V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Ver.4.07.00
C compiler	Renesas Electronics Corporation SuperH RISC engine FamilyC/C++ Compiler Package Ver.9.03 Release02
	Compiler option -cpu=sh2afpu -fpu=single -include="\$(WORKSPDIR)\inc" -object="\$(CONFIGDIR)\\$(FILELEAF).obj" -debug -gbr=auto -chgincpath -errorpath -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1 -nologo
Operation Mode	Boot mode (booting from the memory with 16-bit bus width connected to the CS0 space)
Sample code version	1.00
Board used	Renesas Electronics Corporation SH7269 CPU Board (R0K572690C000BR)
Device used	Renesas Electronics Corporation Slave device (in clocked synchronous serial communications) Model: R5S72643

3. Reference Application Note

For additional information associated with this document, refer to the following application note.

- SH7262/SH7264 Group Example of Initialization (document No.: REJ06B0847)

4. Hardware

4.1 Hardware Configuration

Figure 4.1 shows the configuration for SH7269 connecting a slave device using the IIC3.

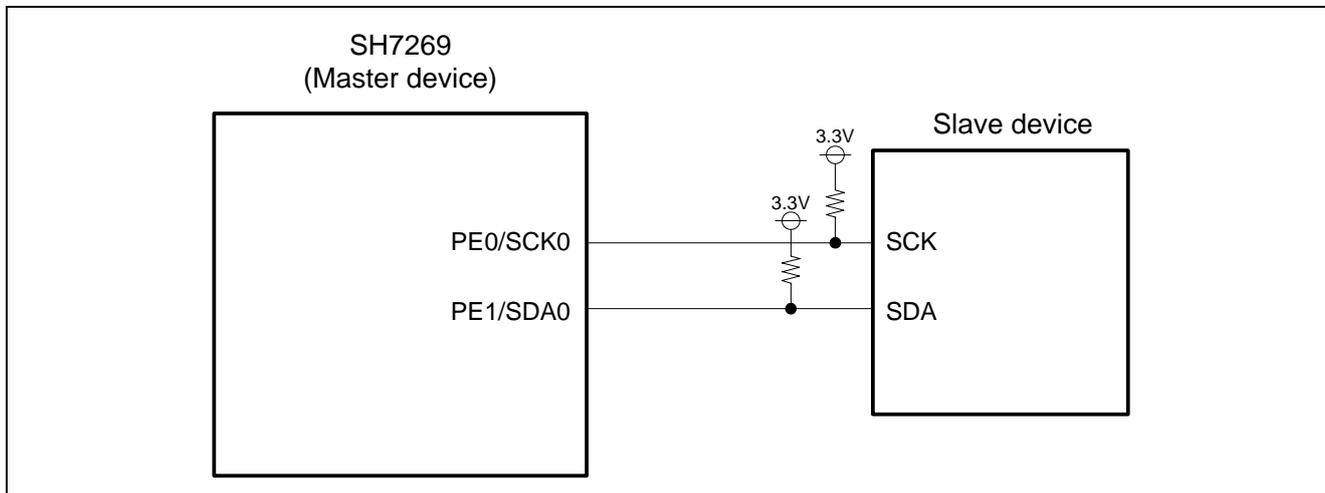


Figure 4.1 Configuration with Slave Device with IIC3

4.2 Used Pins and the Pin Functions

Table 4.1 Used Pins and Their Functions

Pin name	Input/output	Function
PE0/SCK0	Output	Clock output in the clocked synchronous serial communications
PE1/SDA0	Output/Input	Data input/output in the clocked synchronous serial communications

5. Software

5.1 Operation Overview

Figure 5.1 shows the communication sequence with a slave device.

In the sample code, master transmission/reception is carried out by setting the IIC3 to the clocked synchronous serial format. A transmission for ten-byte test data is carried out, which is followed by a reception for ten-byte test data. Continuously, transmission and reception repeat in alternate shift.

Set the slave side to data reception enabled before transmitting data on the master side.

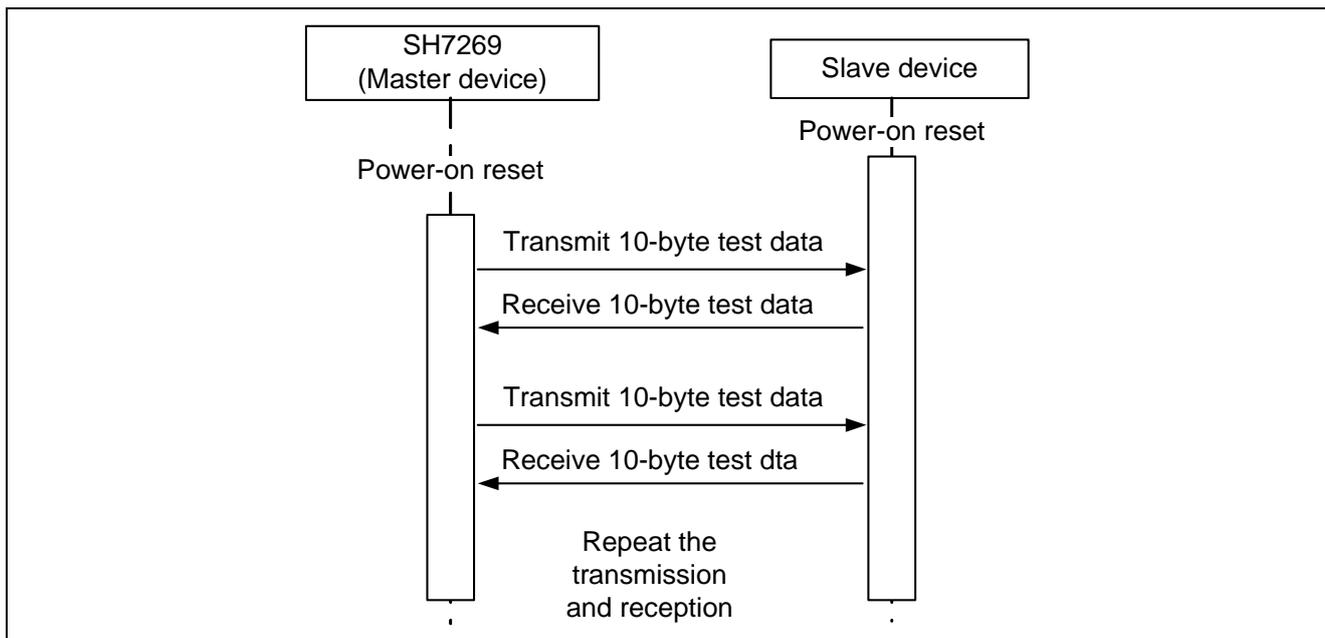


Figure 5.1 Communication Sequence with Salve Device

5.2 File Composition

Table 5.1 lists the files used in the sample code. Files generated by the integrated development environment should not be listed in this table.

Table 5.1 File Composition

File Name	Outline	Remarks
main.c	Main function	
iic3.c	Control transfers using the IIC3 clocked synchronous serial format	Supporting both the master mode and the slave mode (specified by the argument, io_iic3_clksync_init function)
iic3.h	iic3.c interface definition	

5.3 Constants

Table 5.2 and Table 5.3 show the constants and enumeration constants used in the sample code.

Table 5.2 Constants

Constant Name	Setting Value	Description
IIC3_MEMSIZE	10	Transmit buffer size in bytes

Table 5.3 Enumeration Constants

Form	Constant	Setting Value	Description
ecode_t	E_ERR	-1	Return value indicating an end-in-error
	E_OK	0	Return value indicating a normal end
device_t	IIC3_MASTER	0	Master device
	IIC3_SLAVE	1	Slave device

5.4 Variables

Table 5.4 lists the static-type variables used in the sample code.

Table 5.4 Static-Type Variables

Form	Constant	Description	Functions used
static uint8_t	rx_buf[IIC3_MEMSIZE]	Receive buffer	main.c
static uint8_t	mst_test_data[IIC3_MEMSIZE]	Master transmit data	main.c
static device_t	device_mode	Operation mode: master mode or slave mode	iic3.c

5.5 Functions

Table 5.5 lists the functions used in the sample code.

Table 5.5 Functions

Function	Description
main	Main processing
io_iic3_clksync_init	Initialize the IIC3 using the clocked synchronous serial format
io_iic3_clksync_rx	IIC3 reception using the clocked synchronous serial format
io_iic3_clksync_tx	IIC3 transmission using the clocked synchronous serial format

5.6 Function Specifications

The following tables list the sample code function specifications.

main

Outline	Main function
Header	iic3.h
Declaration	void main(void);
Description	Sets the clocked synchronous serial format to the IIC3 and carries out master transmission/reception. Then transmits 10-byte test data. 10-byte test data reception follows. Afterwards, the transmission and reception repeats in alternate shift.
Argument	None
Returned value	None

io_iic3_clksync_init

Outline	Initializes the IIC3 using the clocked synchronous serial format
Header	iic3.h, iodef.h
Declaration	ecode_t io_iic3_clksync_init (device_t mode);
Description	Initializes the IIC3. Configure the basic setting to carry out the transfer processing using the clocked synchronous serial format. Set IIC3_MASTER to the argument <i>mode</i> for transferring in master mode. Set IIC3_SLAVE for transferring in slave mode.
Argument	device_t mode : Operation mode to set (master mode or slave mode)
Returned value	E_OK: Normal end

io_iic3_clksync_rx

Outline	Receives the IIC3 data using the clocked synchronous serial format
Header	iic3.h, iodef.h
Declaration	ecode_t io_iic3_clksync_rx(uint8_t *buf, int32_t size);
Description	Receives data using the IIC3 clocked synchronous serial format. When the variable <i>device_mode</i> is IIC3_MASTER, receives the data in master mode, and when the variable is IIC3_SLAVE, receives the data in slave mode. The SCL pin outputs a clock when master reception is selected. The receive data is stored in the area for the byte counts specified by the argument <i>size</i> in the address specified by the argument <i>buf</i> . The processing ends when completing transferring all the data.
Argument	uint8_t *buf : Start address in the receive data int32_t size : Received byte count
Returned value	E_OK: Normal end

`io_iic3_clksync_tx`

Outline	Transmits IIC3 using the clocked synchronous serial format
Header	iic3.h, iodef.h
Declaration	<code>ecode_t io_iic3_clksync_tx(uint8_t *buf, int32_t size);</code>
Description	Transmits data using IIC3 clocked synchronous serial format. When the variable <code>device_mode</code> is <code>IIC3_MASTER</code> , carries out master transmission, and when the variable is <code>IIC3_SLAVE</code> , carries out slave transmission. The SCL pin outputs a clock when master transmission is selected. The data is used for transmit data for byte counts specified by the argument <code>size</code> from the address specified by the argument <code>buf</code> . The processing ends when completing transferring all the data..
Argument	<code>uint8_t *buf</code> : Start address in the receive data <code>int32_t size</code> : Received byte count
Returned value	<code>E_OK</code> : Normal end

5.7 Flowchart

5.7.1 Main Processing

Figure 5.2 shows the procedure of the main processing.

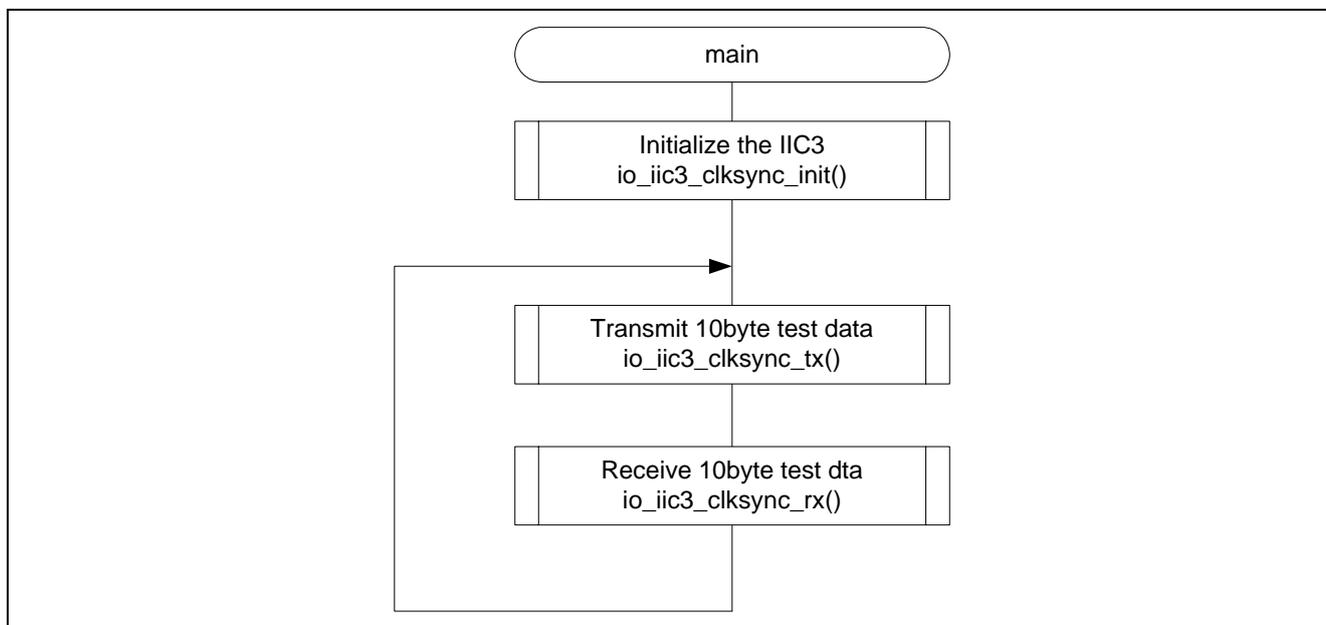


Figure 5.2 Main Processing

5.7.2 IIC3 Initialization

Figure 5.3 shows the procedure of initializing the IIC3.

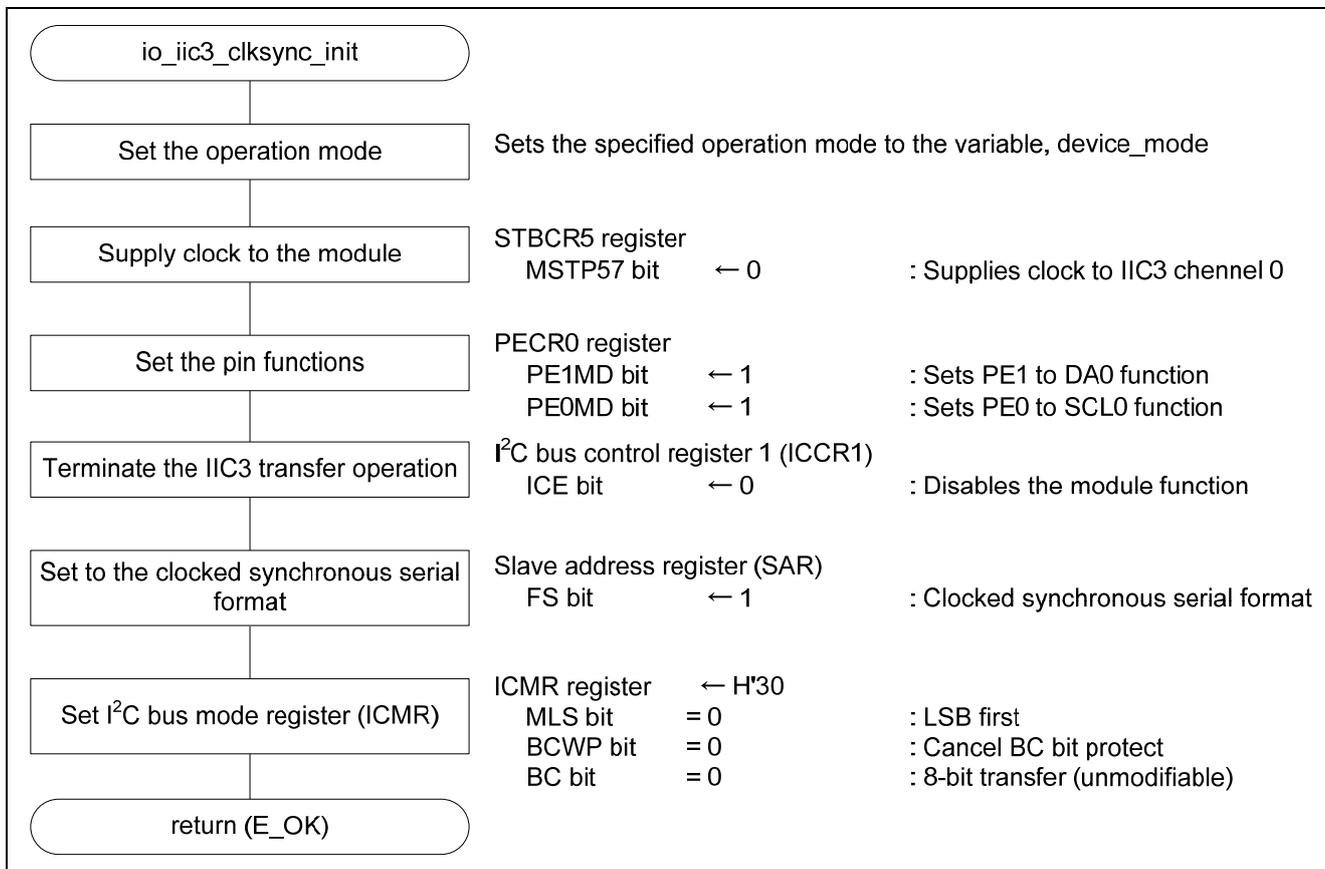


Figure 5.3 IIC3 Initialization

5.7.3 Data Reception Processing

Figure 5.4 shows the procedure for data reception.

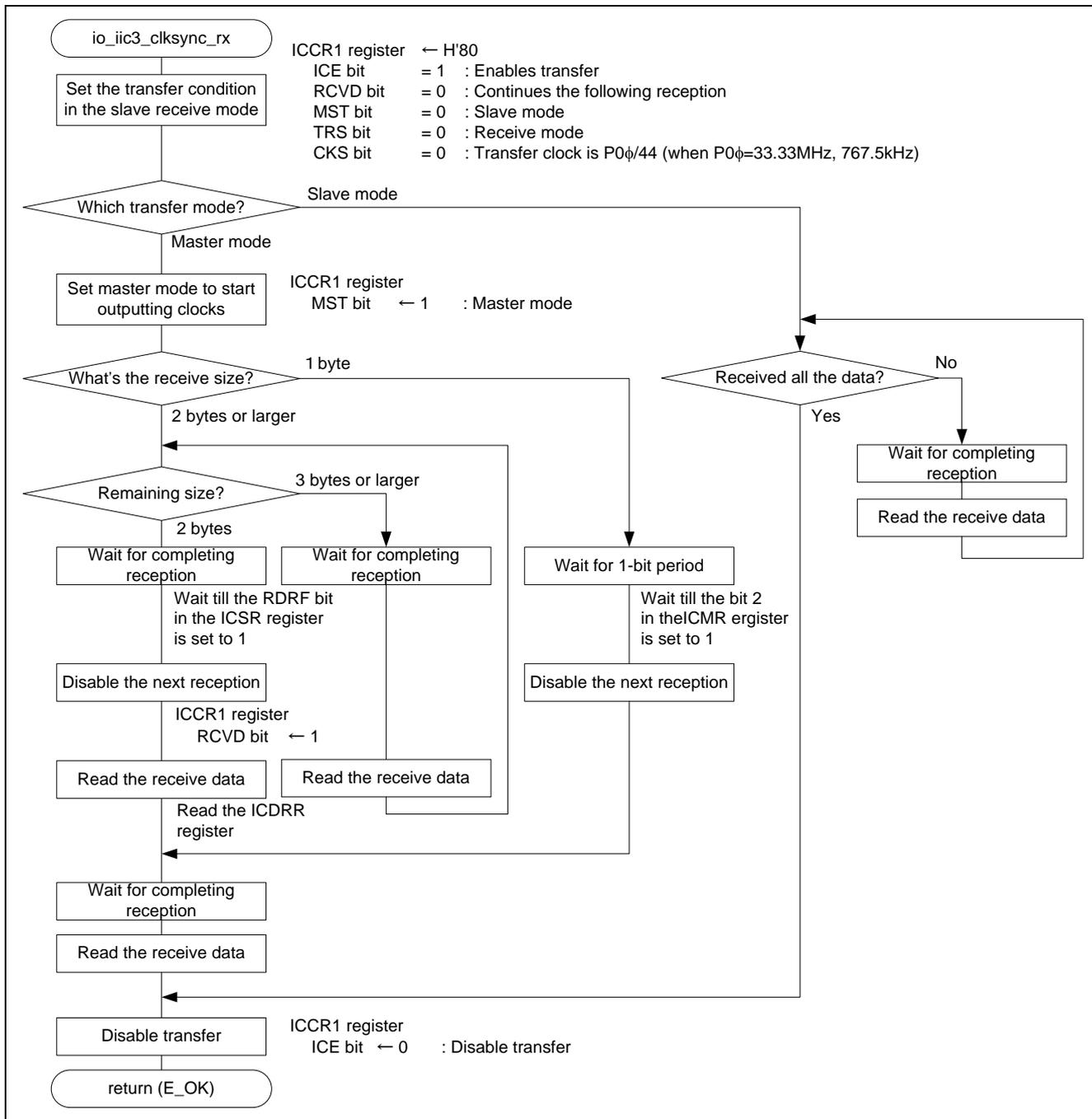


Figure 5.4 Data Reception

5.7.4 Data Transmission Processing

Figure 5.5 shows the procedure of data transmission.

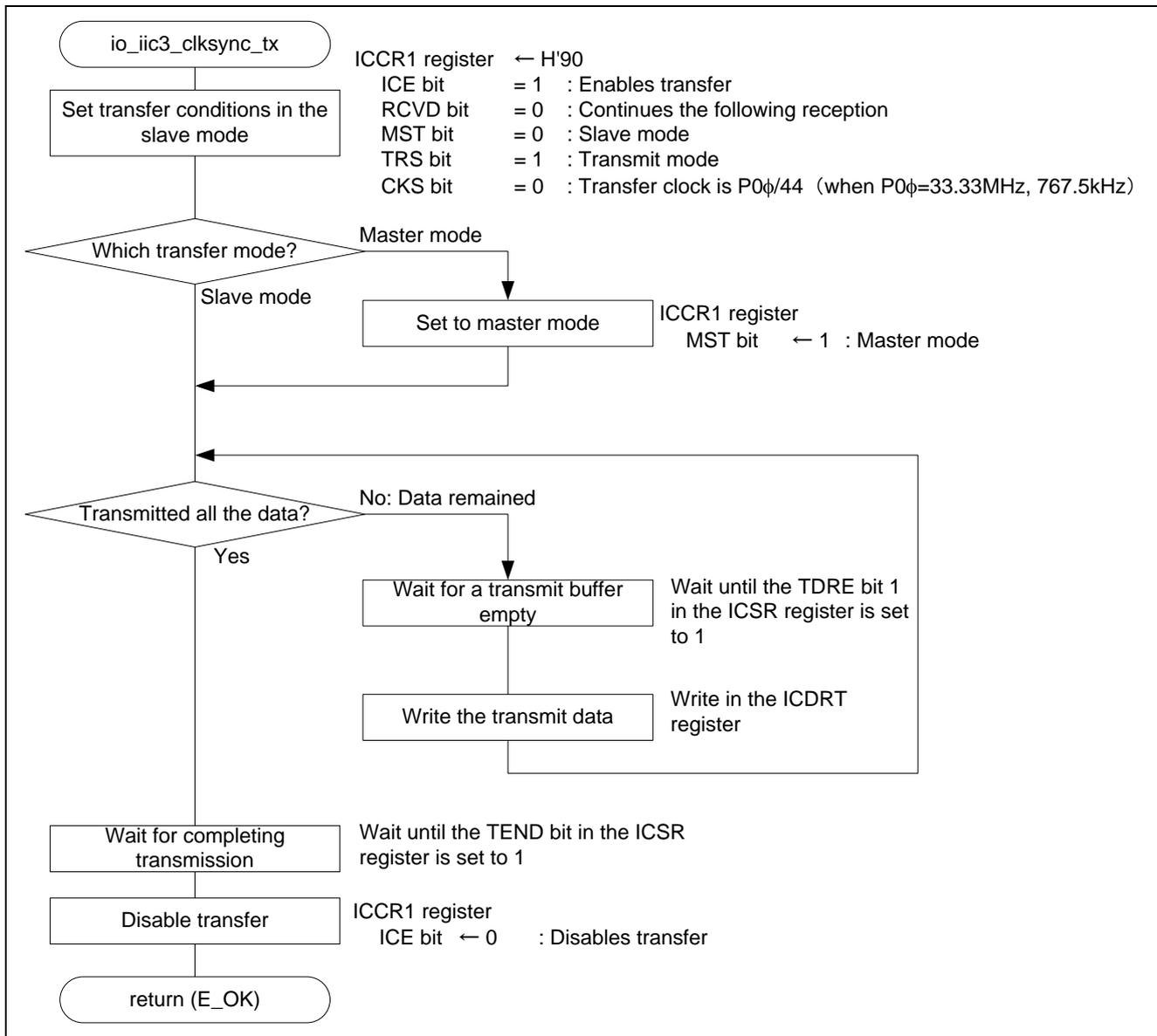


Figure 5.5 Data Transmission

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

Hardware Manual

SH7268 Group, SH7269 Group User's Manual: Hardware Rev.1.00

The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

Development Tool Manual

SuperH RISC Engine Family C/C++ Compiler, Assembler, Optimizing Linkage Editor

Complier Package V.9.04 User's Manual Rev.1.01

The latest version can be downloaded from the Renesas Electronics website.

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Revision History	SH7268/SH7269 Group Application Note for IIC Bus Interface3 (Master Transmission and Reception Using Clocked Synchronous Serial Format)
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Rev.	Date	Description	
		Page	Summary
1.00	Feb. 03, 2012	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable.

When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different type number, confirm that the change will not lead to problems.

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