
R32C/100 Series

Timer A Operation Using a Two-phase Pulse Signal, Free-running Count Function,
Quadrupled Processing, and Z-phase Input in Event Counter Mode

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Abstract

This document describes timer A operation using two-phase pulse signal processing, free-running count function, quadrupled processing, and Z-phase input in event counter mode with the R32C/100 Series.

Products

MCUs: R32C/116 Group, R32C/117 Group, and R32C/118 Group

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

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1. Specifications

When using the event counter mode of timer A3, the timer counts a two-phase pulse signal applied to pins TA3IN and TA3OUT using quadrupled processing. A Z-phase input signal applied to the INT2 pin resets the timer counter.

Table 1.1 lists the Peripheral Function and Its Application. Figure 1.1 and Figure 1.2 show the Overview of Quadrupled Processing and Counter Reset Timing, respectively.

Table 1.1 Peripheral Function and Its Application

Peripheral Function	Application
Timer A (timer A3)	Counts a two-phase pulse signal applied to pins TA3IN and TA3OUT

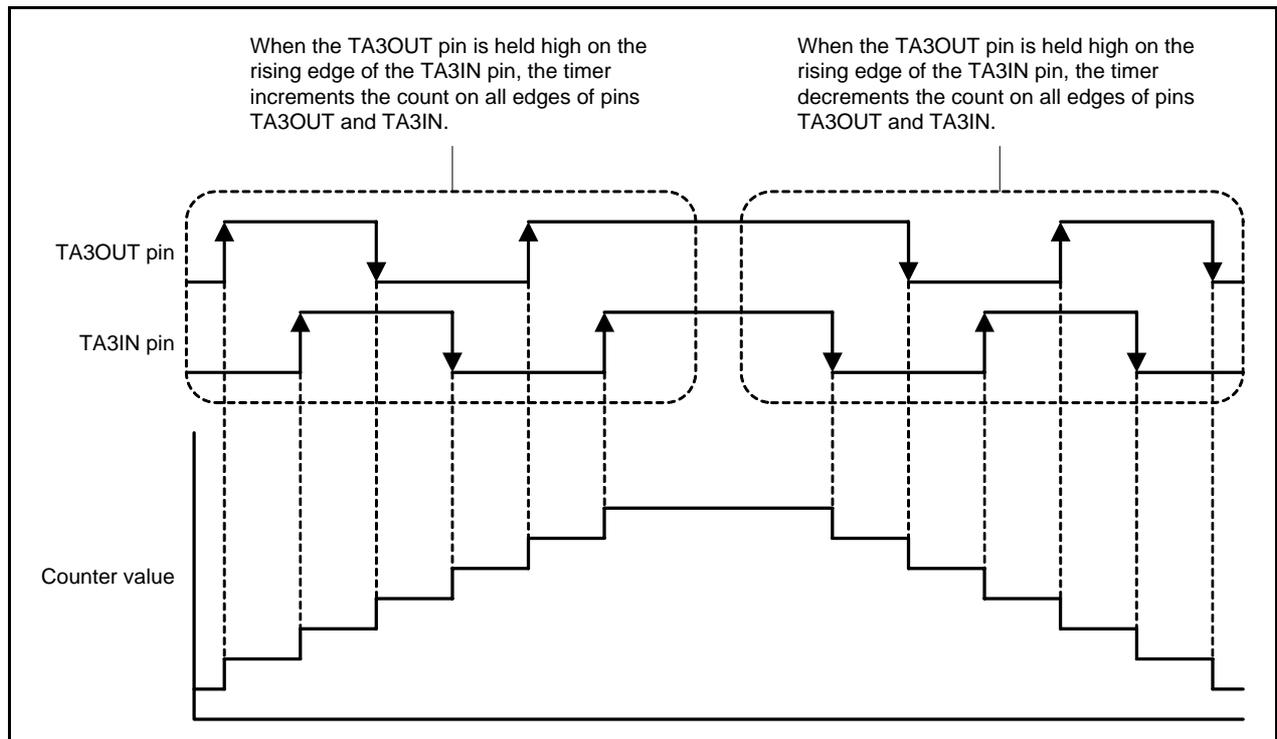


Figure 1.1 Overview of Quadrupled Processing

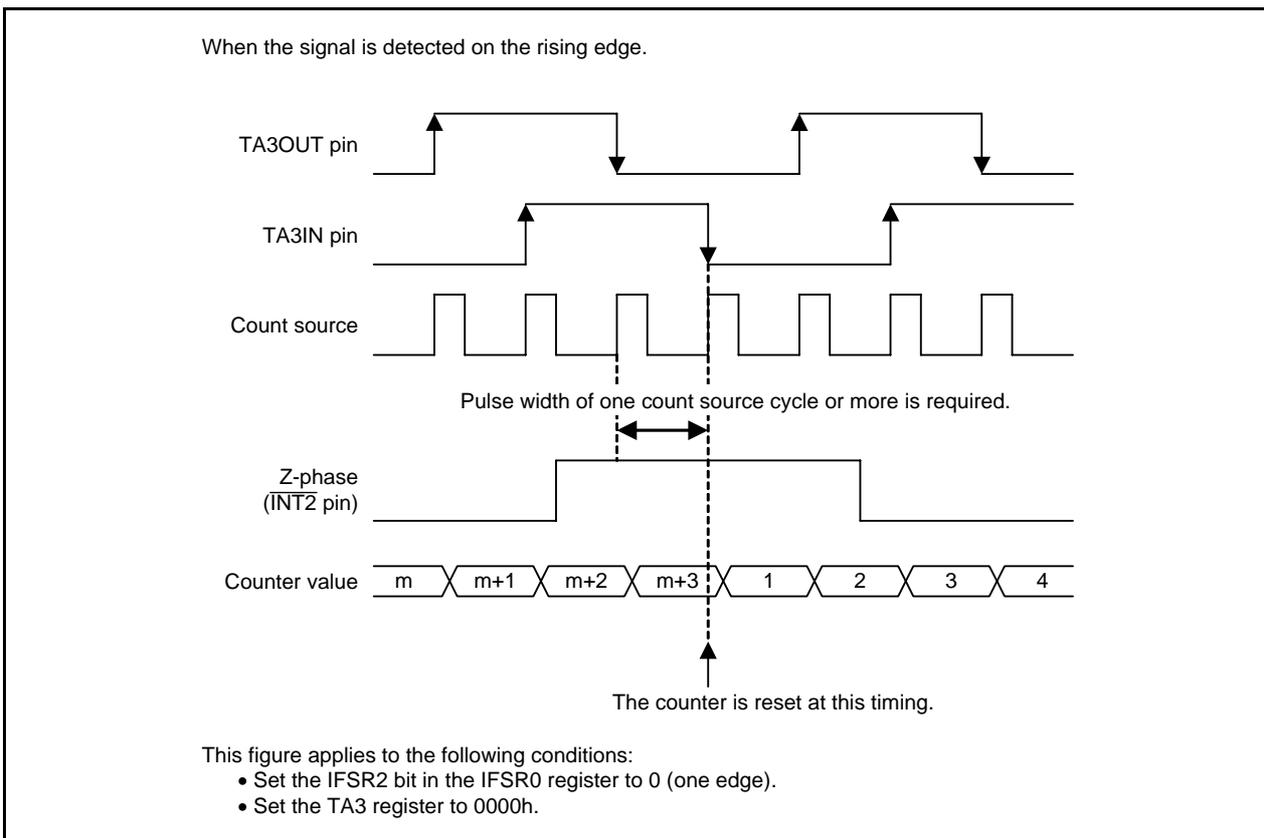


Figure 1.2 Counter Reset Timing

2. Operation Confirmation Conditions

The sample code accompanying this application note has been run and confirmed under the conditions below.

Table 2.1 Operation Confirmation Conditions

Item	Contents
MCU used	R5F64189DFD (R32C/118 Group)
Operating frequencies	Main clock: 16 MHz PLL clock: 100 MHz Base clock: 50 MHz CPU clock: 50 MHz Peripheral bus clock: 25 MHz Peripheral function clock source: 25 MHz
Operating voltage	5 V
Integrated development environment	Renesas Electronics Corporation High-performance Embedded Workshop Version 4.07
C compiler	Renesas Electronics Corporation R32C/100 Series C Compiler V.1.02 Release 01 Compile options -D __STACKSIZE__=0X300 -D __ISTACKSIZE__=0X300 -DVECTOR_ADR=0x0FFFFFFBDC -c -finfo -dir "\$(CONFIGDIR)" (Default setting is used in the integrated development environment.)
Operating mode	Single-chip mode
Sample code version	Version 1.00
Board used	Renesas Starter Kit for R32C/118 (product name: R0K564189S000BE)

3. Reference Application Note

The application note associated with this application note is listed below. Refer to the following application note for additional information.

- R32C/100 Series Configuring PLL Mode (REJ05B1221-0100)

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P7_6/TA3OUT	Input	Two-phase pulse input of timer A3
P7_7/TA3IN	Input	Two-phase pulse input of timer A3
P8_4/ $\overline{\text{INT2}}$	Input	Z-phase pulse input of timer A3 (counter reset)

5. Software

5.1 Operation Overview

The timer A3 counter counts a two-phase pulse signal applied to pins TA3IN and TA3OUT. A Z-phase input signal resets the counter during a count operation.

(1) Timer A3 initial settings

Table 5.1 and Table 5.2 list the Timer A3 Settings and $\overline{\text{INT2}}$ Pin Setting, respectively.

Table 5.1 Timer A3 Settings

Item	Contents
Two-phase pulse processing operation	Quadrupled processing operation
Counter reset by Z-phase input signal	Enabled
Count operation type	Free-running

Table 5.2 $\overline{\text{INT2}}$ Pin Setting

Item	Contents
Polarity select	Rising edge

(2) Timer A3 count starts

Set the timer A3 count start bit in the count start register to 1 (start counter). Even if the counter overflows or underflows, it continues counting without reloading the value in the reload register.

(3) Timer A3 counter reset

The counter is reset at the initial count source input after a Z-phase input is detected.

Figure 5.1 shows the Operation Timing.

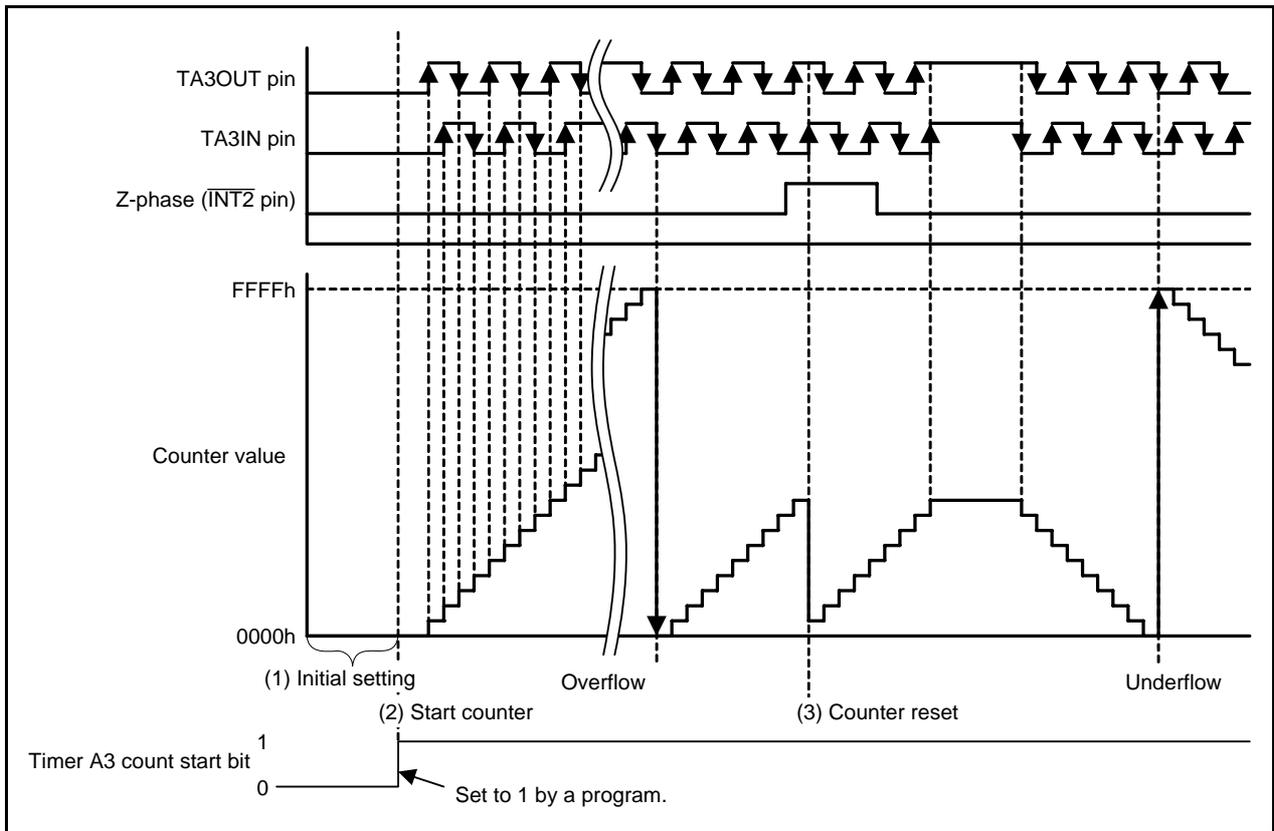


Figure 5.1 Operation Timing

5.2 Flowcharts

5.2.1 Main Processing

Figure 5.2 and Figure 5.3 show Main Processing (1) and Main Processing (2), respectively.

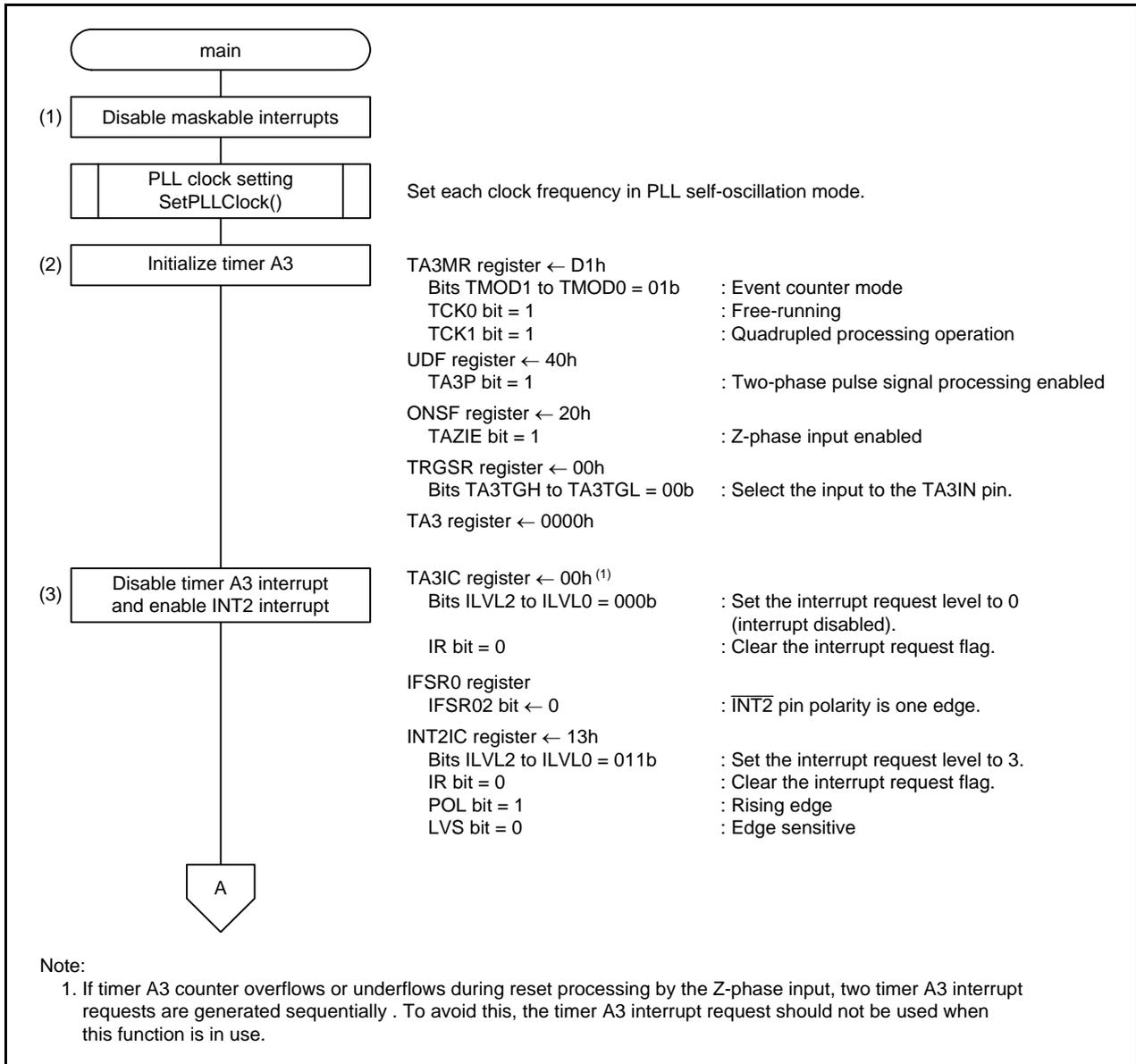


Figure 5.2 Main Processing (1)

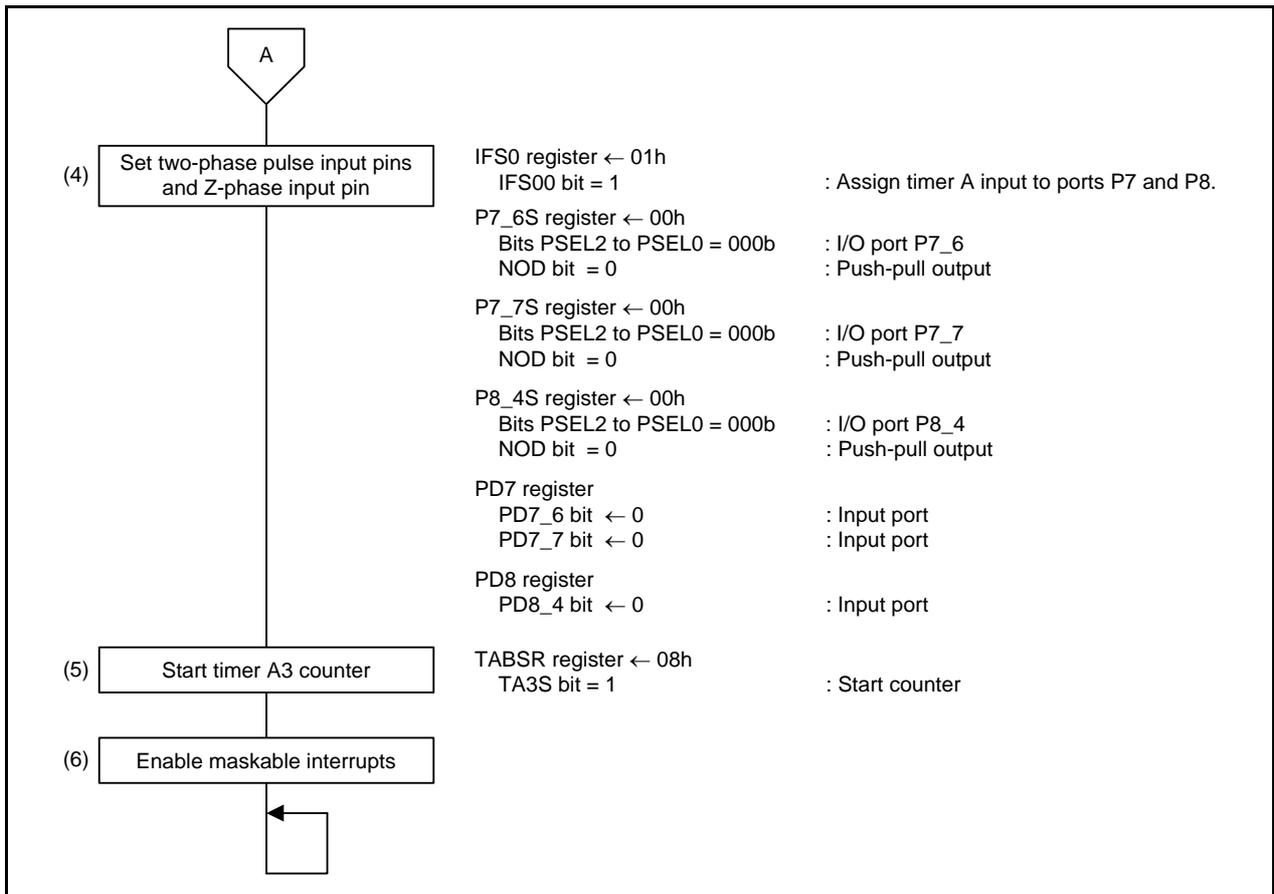


Figure 5.3 Main Processing (2)

6. Sample Code

Sample code can be downloaded from the Renesas Electronics website.

7. Reference Documents

R32C/116 Group User's Manual: Hardware Rev.1.10

R32C/117 Group User's Manual: Hardware Rev.1.10

R32C/118 Group User's Manual: Hardware Rev.1.10

The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Electronics website.

C Compiler Manual

R32C/100 Series C Compiler Package V.1.02

C Compiler User's Manual Rev.2.00

The latest version can be downloaded from the Renesas Electronics website.

8. Website and Support

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<http://www.renesas.com/>

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Revision History	R32C/100 Series Timer A Operation Using a Two-phase Pulse Signal, Free-running Count Function, Quadrupled Processing, and Z-phase Input in Event Counter Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Jan. 14, 2011	—	First edition issued

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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