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## R8C/25 Group

### Timer RE in Output Compare Mode

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#### 1. Abstract

This document describes how to set up and use timer RE in output compare mode in the R8C/25 Group.

#### 2. Introduction

The application example described in this document is applied to the following MCU and parameter(s):

- MCU: R8C/25 Group
- XIN clock: 20 MHz

This program can be used with other R8C/Tiny Series which have the same special function registers (SFRs) as the R8C/25 Group. Check the manual for any additions and modifications to functions. Careful evaluation is recommended before using this application note.

### 3. Descriptions of Applications

#### 3.1 Timer RE

Timer RE has 4-bit and 8-bit counters. Timer RE has the following two modes:

- Real-time clock mode      Generate a 1-second signal from f<sub>C4</sub> and counts seconds, minutes, hours, and days of the week.
- Output compare mode      Count a count source and detect compare matches.

#### 3.2 Output Compare Mode

In output compare mode, the internal count source divided by 2 is counted using the 4-bit or 8-bit counter and the compare value match is detected with the 8-bit counter. Figure 3.1 shows a Block Diagram of Output Compare Mode and Table 3.1 lists the Output Compare Mode Specifications. Figures 3.2 to 3.6 show the Registers Associated with Output Compare Mode, and Figure 3.7 shows the Operation in Output Compare Mode.

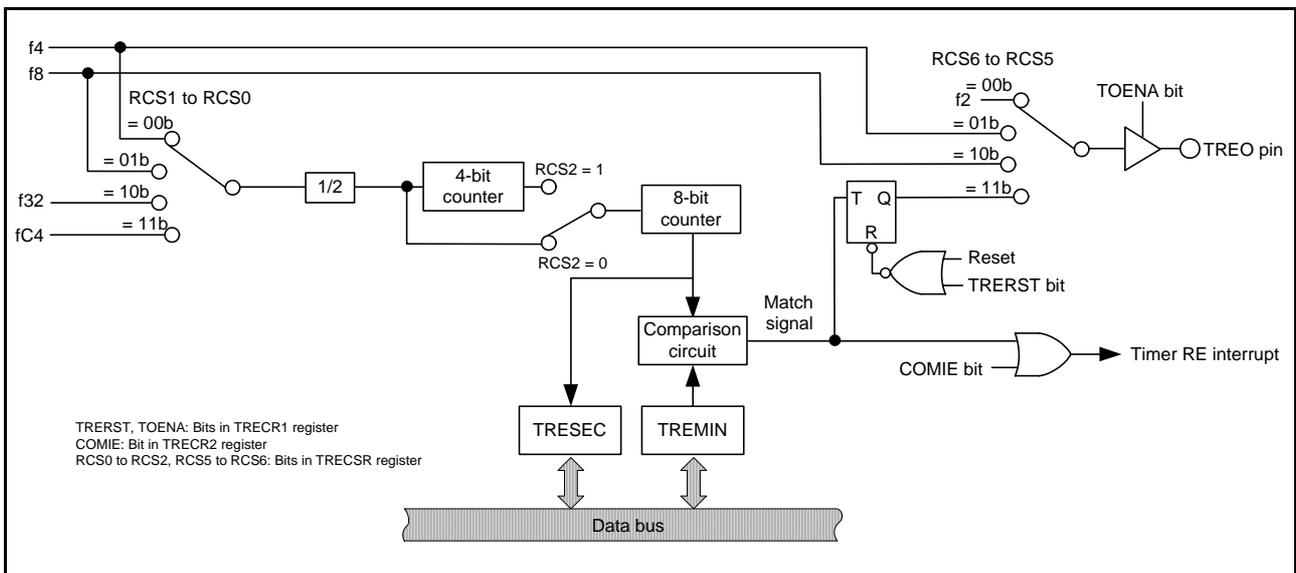


Figure 3.1 Block Diagram of Output Compare Mode

**Table 3.1 Output Compare Mode Specifications**

Item	Specification
Count sources	f4, f8, f32, fC4
Count operations	<ul style="list-style-type: none"> <li>• Increment</li> <li>• When the 8-bit counter content matches the TREMIN register content, the value returns to 00h and the count continues. The count value is held while the count stops.</li> </ul>
Count period	<ul style="list-style-type: none"> <li>• When RCS2 = 0 (4-bit counter is not used)  <math>1/f_i \times 2 \times (n+1)</math></li> <li>• When RCS2 = 1 (4-bit counter is used)  <math>1/f_i \times 32 \times (n+1)</math></li> </ul> f <sub>i</sub> : Frequency of count source n: Setting value of TREMIN register
Count start condition	1 (count starts) is written to the TSTART bit in the TRECR1 register.
Count stop condition	0 (count stops) is written to the TSTART bit in the TRECR1 register.
Interrupt request generation timing	When the 8-bit counter content matches the TREMIN register content.
TREO pin function	Select any one of the following: <ul style="list-style-type: none"> <li>• Programmable I/O ports</li> <li>• Output f2, f4, or f8</li> <li>• Compare output</li> </ul>
Read from timer	When reading the TRESEC register, the 8-bit counter value can be read. When reading the TREMIN register, the compare value can be read.
Write to timer	Writing to the TRESEC register is disabled. When bits TSTART and TCSTF in the TRECR1 register are set to 0 (timer stops), writing to the TREMIN register is enabled.
Select functions	<ul style="list-style-type: none"> <li>• Select use of 4-bit counter</li> <li>• Compare output function</li> </ul> Every time the 8-bit counter value matches the TREMIN register value, TREO output polarity is reversed. The TREO pin outputs "L" after reset is deasserted and the timer RE is reset by the TRERST bit in the TRECR1 register. The output level is held by setting the TSTART bit to 0 (count stops).

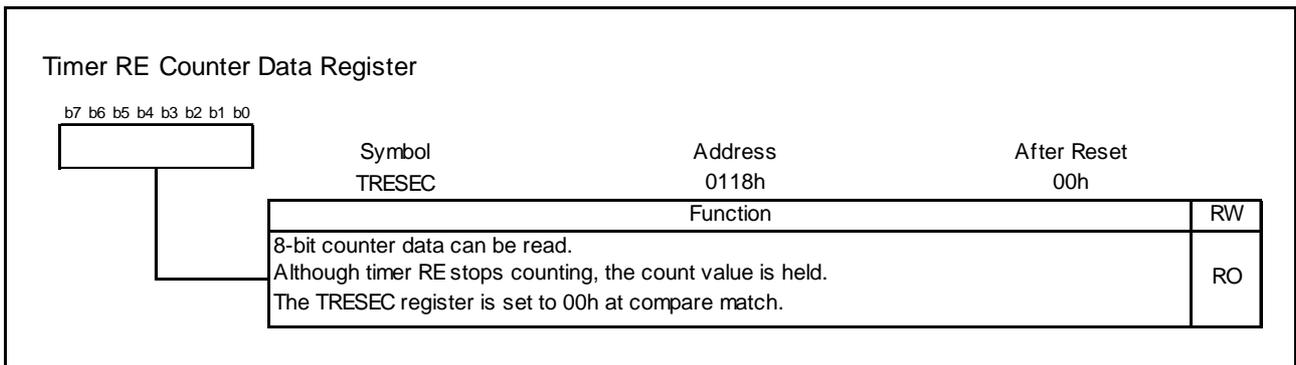


Figure 3.2 TRESEC Register in Output Compare Mode

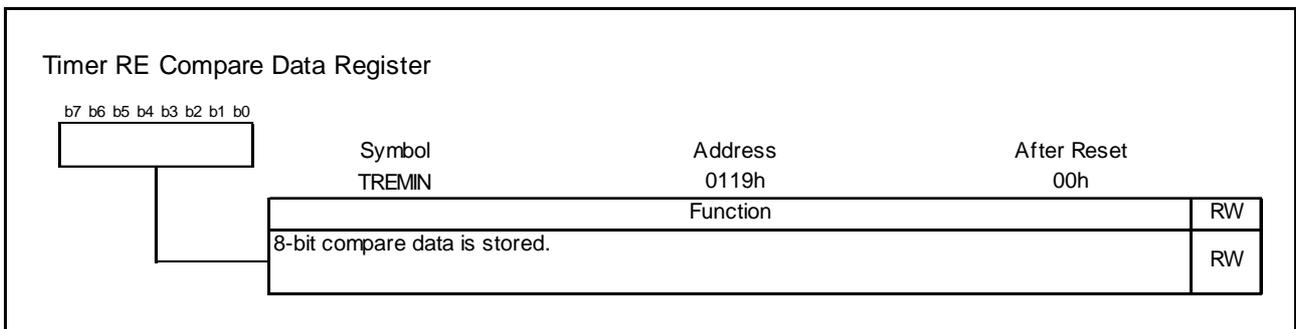


Figure 3.3 TREMIN Register in Output Compare Mode

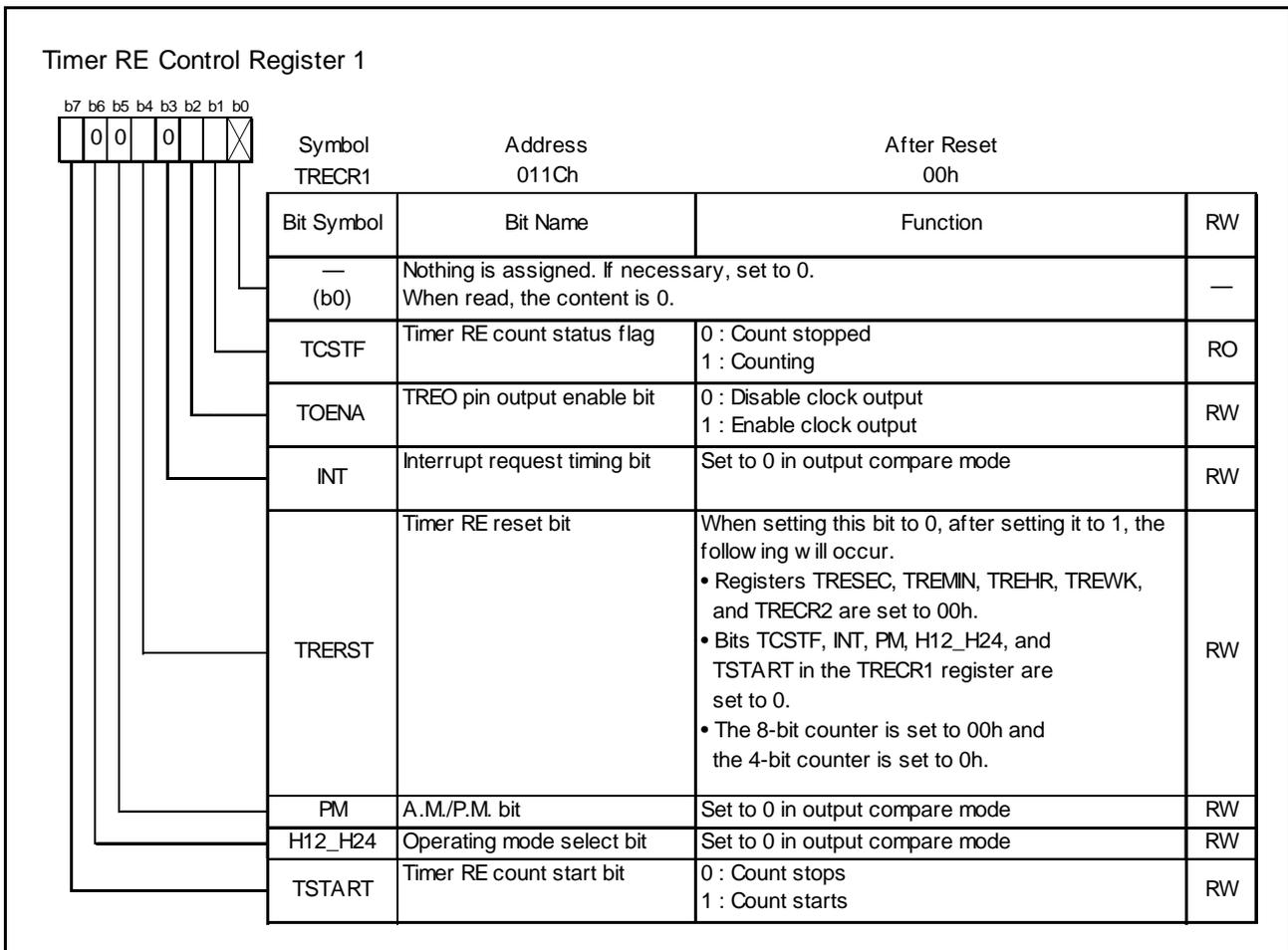


Figure 3.4 TREC1 Register in Output Compare Mode

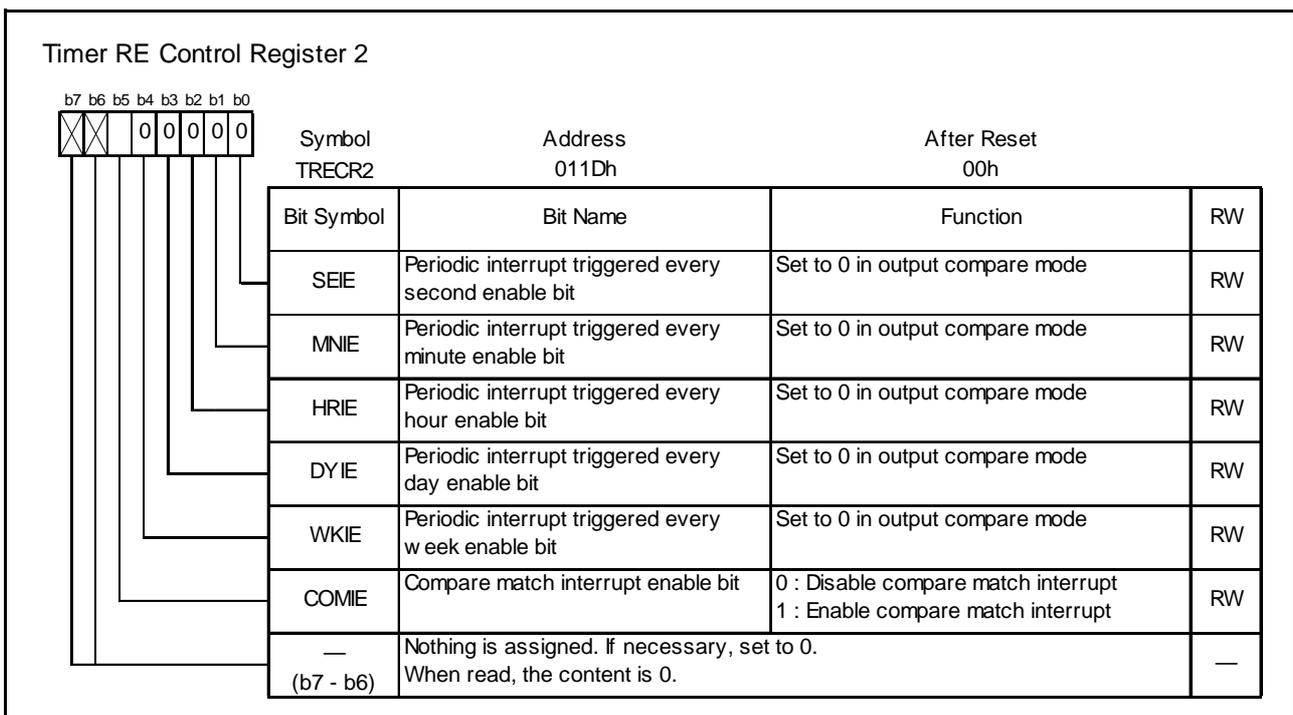


Figure 3.5 TREC2 Register in Output Compare Mode

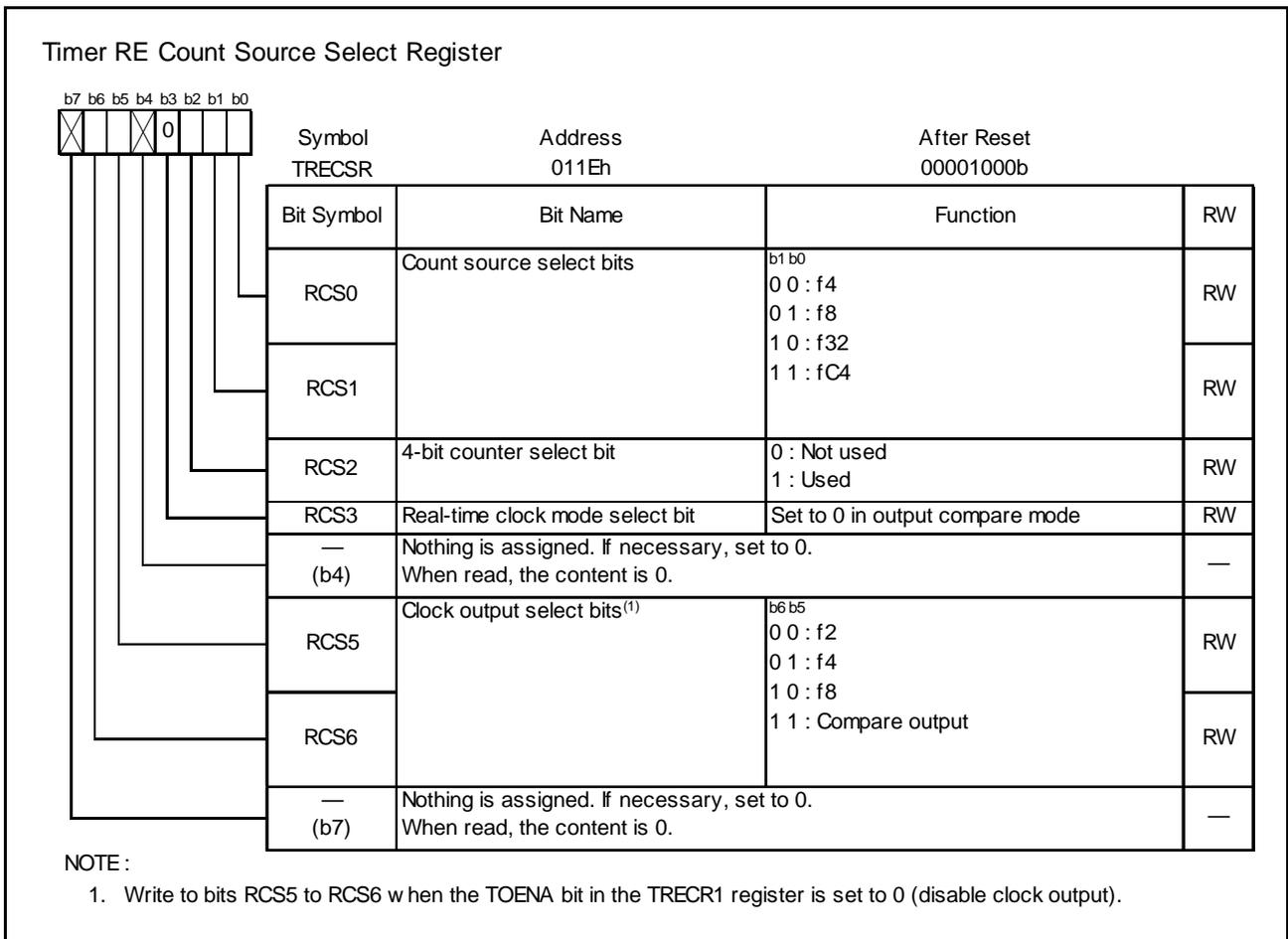


Figure 3.6 TRECSR Register in Output Compare Mode

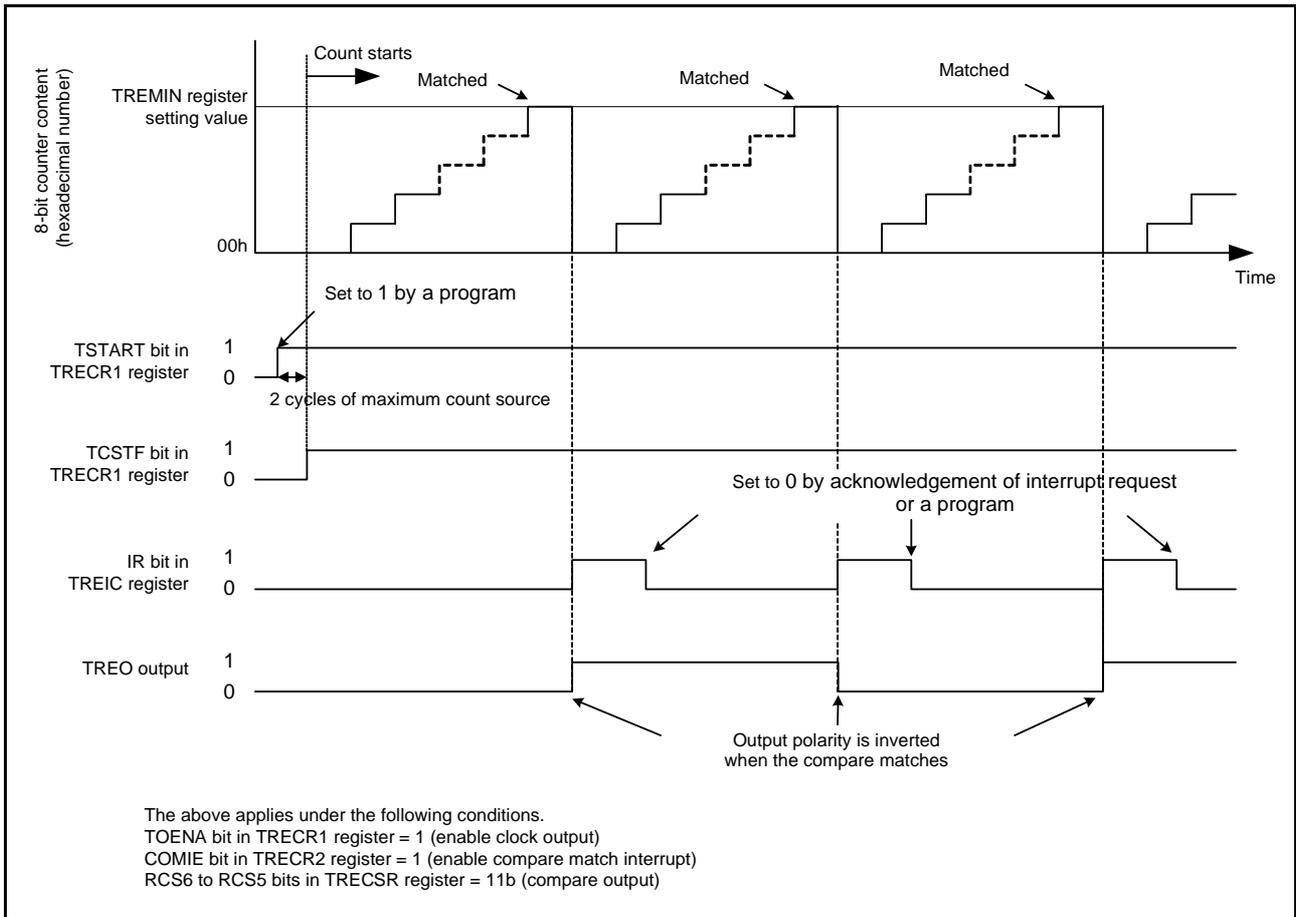


Figure 3.7 Operation in Output Compare Mode

### 3.3 Notes on Timer RE

#### 3.3.1 Starting and Stopping Count

Timer RE has the TSTART bit for instructing the count to start or stop, and the TCSTF bit which indicates count start or stop. Bits TSTART and TCSTF are in the TREC1 register.

Timer RE starts counting and the TCSTF bit is set to 1 (count starts) when the TSTART bit is set to 1 (count starts). It takes up to two cycles of the count source until the TCSTF bit is set to 1 after setting the TSTART bit to 1. During this time, do not access registers associated with timer RE<sup>(1)</sup> other than the TCSTF bit.

Also, timer RE stops counting when setting the TSTART bit to 0 (count stops) and the TCSTF bit is set to 0 (count stops). It takes the time for up to two cycles of the count source until the TCSTF bit is set to 0 after setting the TSTART bit to 0. During this time, do not access registers associated with timer RE other than the TCSTF bit.

NOTE:

1. Registers associated with timer RE: TRESEC, TREMIN, TREHR, TREWK, TREC1, TREC2, and TRECSR.

#### 3.3.2 Register Setting

Write to the following registers or bits when timer RE is stopped:

- Registers TRESEC, TREMIN, TREHR, TREWK, and TREC2
- Bits H12\_H24, PM, and INT in TREC1 register
- Bits RCS0 to RCS3 in TRECSR register

Timer RE is stopped when bits TSTART and TCSTF in the TREC1 register are set to 0 (timer RE stopped).

Also, set all above-mentioned registers and bits (immediately before timer RE count starts) before setting the TREC2 register.

4. Program Outline

Every time a compare match is detected, the TREO output polarity is reversed. The output width for “H” period and “L” period is set to 100 μs.

$$100 \mu s = 20 \text{ MHz} \times f8 \times (4\text{-bit counter is not used}) \times (\text{TREMIN} + 1) \\ = 50 \text{ ns} \times 8 \times 2 \times 125$$

Figure 4.1 shows an Assigned Pin.

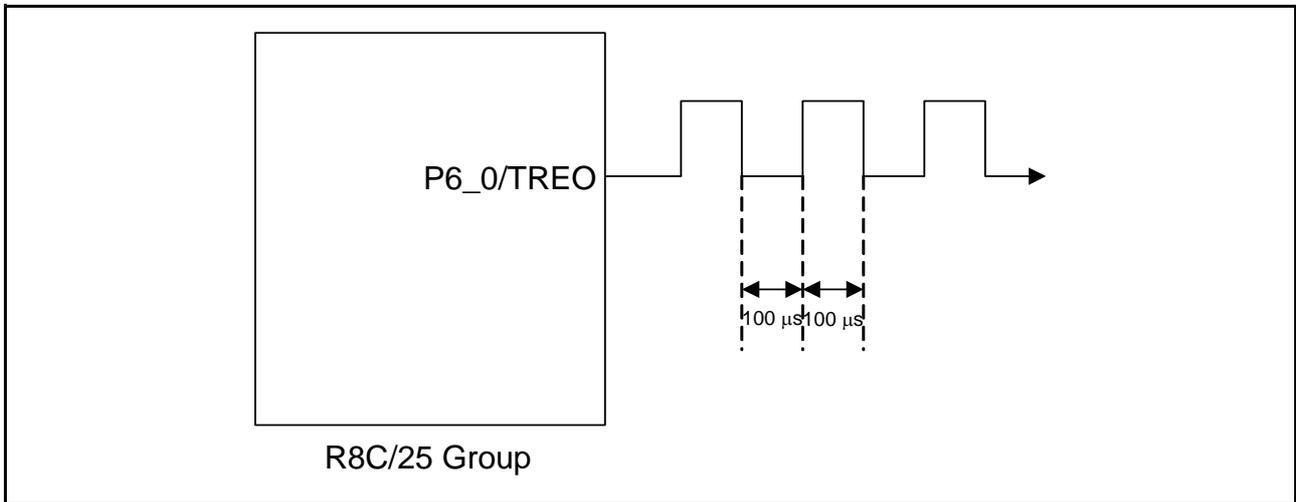


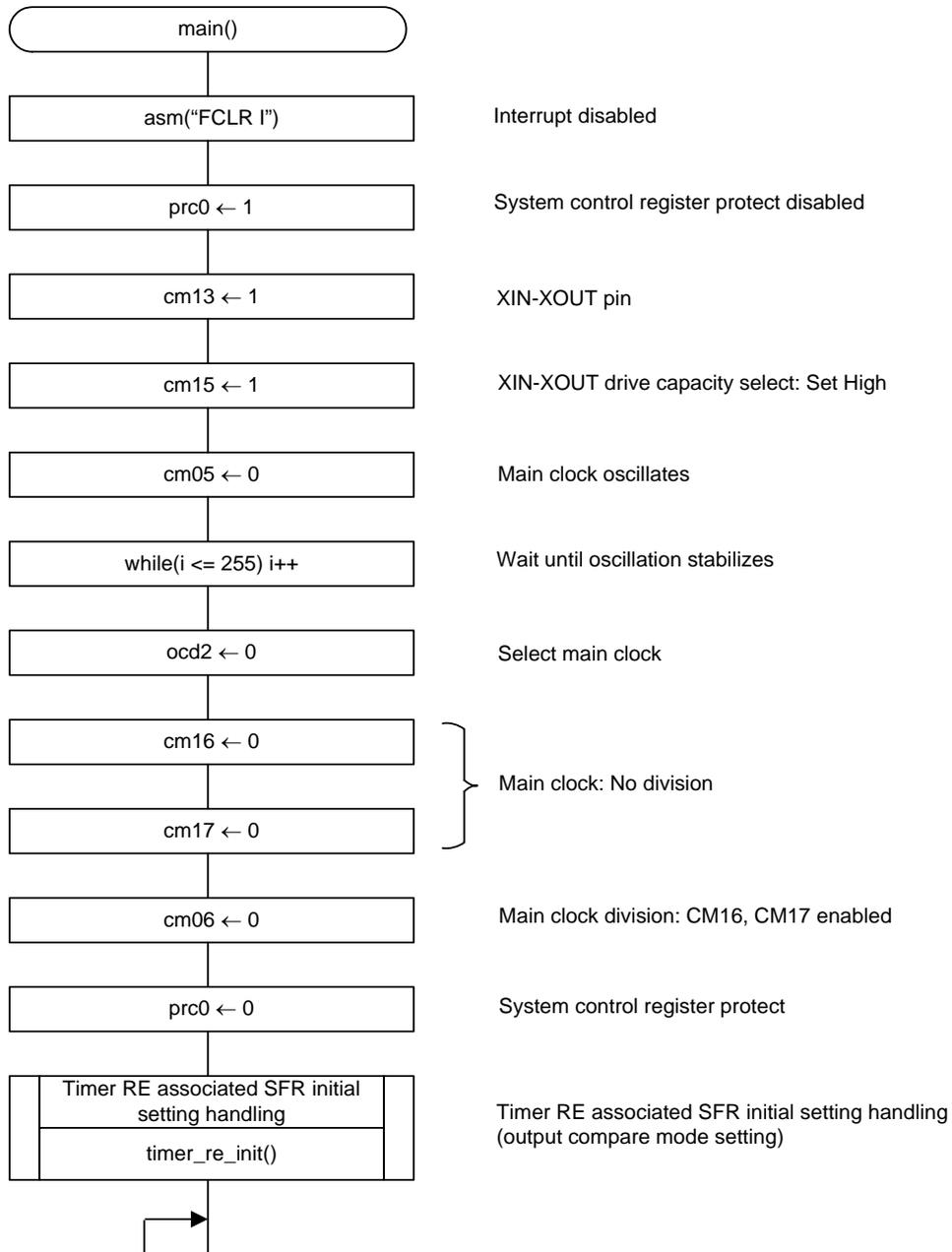
Figure 4.1 Assigned Pin

4.1 Function Table

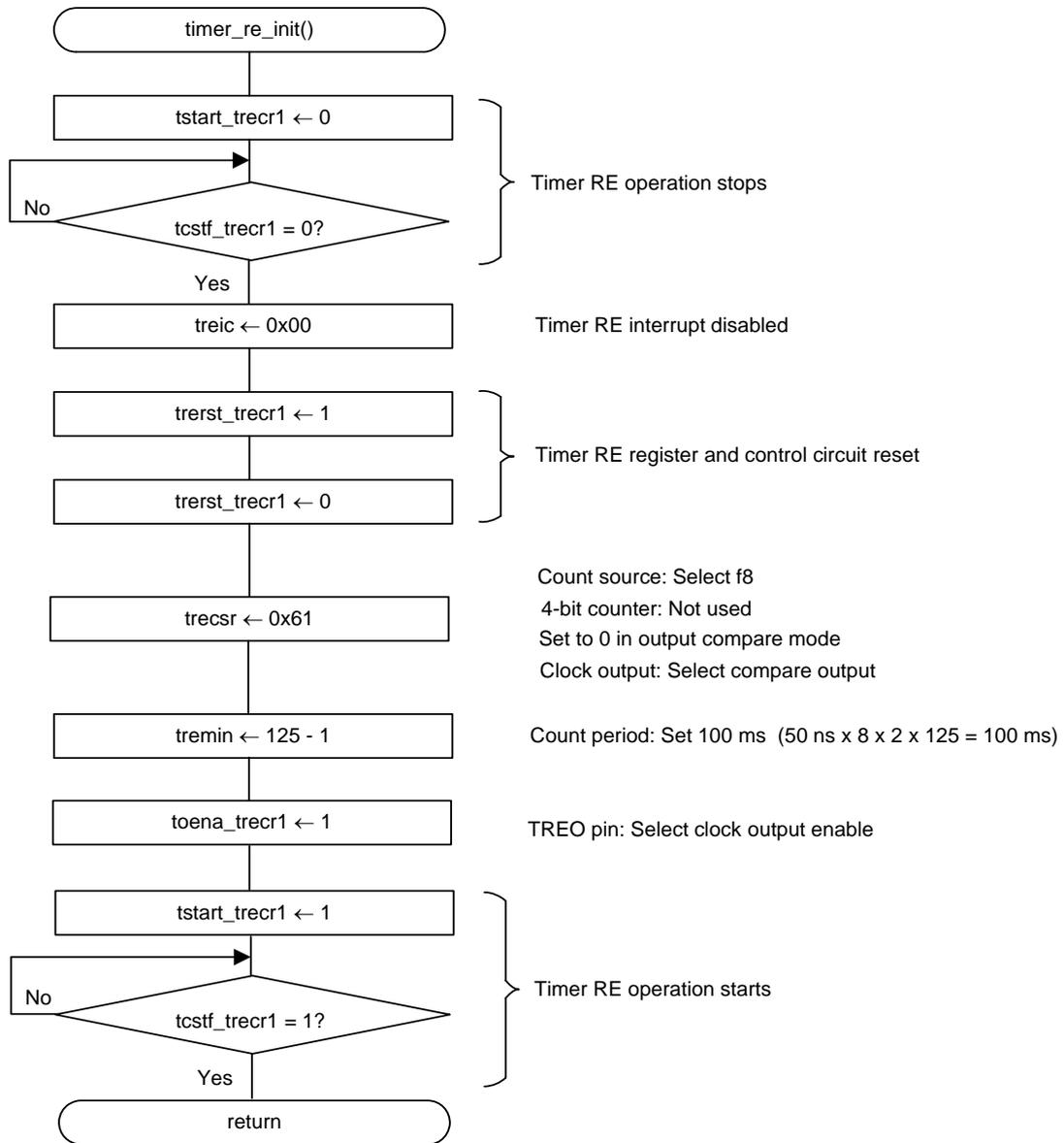
Declaration	void timer_re_init (void)		
Outline	Timer RE associated SFR initial setting		
Argument	Argument name		Meaning
	None		
Variable used (global)	Variable name		Contents used
	None		
Returned value	Type	Value	Meaning
	None		
Function	Timer RE associated SFR register settings are initialized.		

4.2 Flow Chart

4.2.1 Main Function



4.2.2 Timer RE Associated SFR Initial Setting



## 5. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website.  
To download, click “Application Notes” in the left-hand side menu on the R8C/Tiny Series page.

## 6. Reference Documents

Hardware Manual

R8C/25 Group Hardware Manual

The latest version can be downloaded from the Renesas Technology website.

Technical Update/Technical News

The latest information can be downloaded from the Renesas Technology website.

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REVISION HISTORY	R8C/25 Group Timer RE in Output Compare Mode
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Rev.	Date	Description	
		Page	Summary
1.00	Dec 01, 2006	–	First Edition issued
1.10	Feb 29, 2008	11	Flow chart (program) partly revised

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